IBM Power Systems

POWER10 Processor
for Regular Techies

Nigel Griffiths POWER Technical Staff Member, IBM, UK   [v10]
IBM email: nag@uk.ibm.com   @mr_nmon twitter
http://tinyurl.com/njmon - njmon sourceforge project
http://tinyurl.com/AIXpert - My Blogs
https://www.youtube.com/user/nigelargriffiths - My 215 Videos

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POWER10 Processor for Regular Techies

Abstract:

Nigel will cover the POWER10 processor for big commercial server specialists such as Systems Administrator, Performance Guru, DevOps, Solution Designer, Systems Architects, and similar. Not for Processor Architects/Designers or kernel coders.

We will work through the publicly available information, followed by a little speculation - how the POWER9 generation servers might look, if they were running POWER10 processors a glimpse into the future.

No IBM Confidential information nor making Announcements in this session.

We will not be covering dates, prices or
                   performance rPerf/CPW ratings, GHz or model names.

Relevant for AIX / IBM i / Linux on POWER environments.

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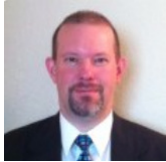
2

IBM's POWER10 Processor   IBM

32nd Hot Chips Conference - August 2020

William Starke
- Distinguished Engineer
- POWER10 Processor Architect

Brian Thompto
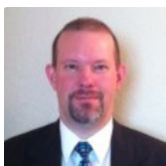- Distinguished Engineer
- POWER10 Processor Core Architect

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IBM's POWER10 Processor   IBM
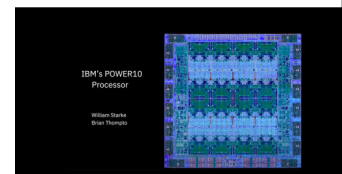
In September + October ➜ YouTube

William Starke

IBM POWER10 Processor
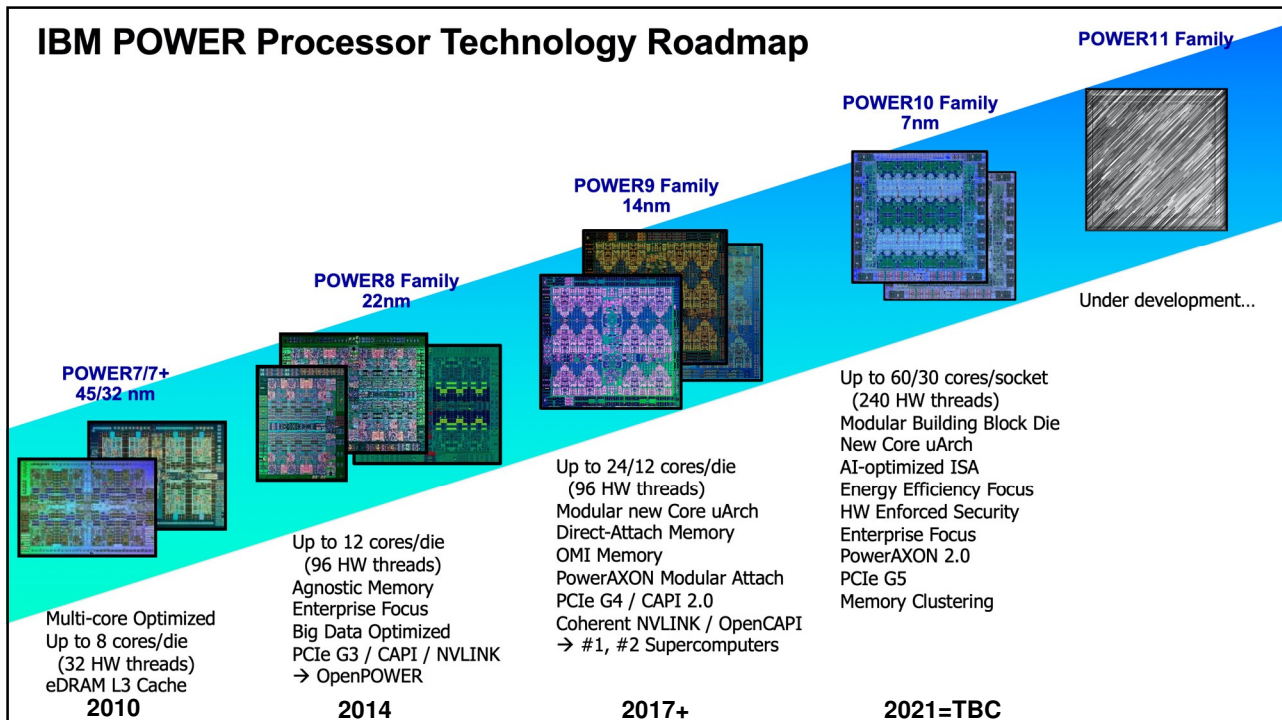OpenPOWER Summit
25 minute version with 1100+ Views
https://www.youtube.com/watch?v=27VRdl2BGWg

Brian Thompto

IBM POWER10 Processor: chip capabilities
90 minute version with 180+ Views
https://www.youtube.com/watch?v=FMvret3p7qE

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IBM POWER Processor Technology Roadmap

POWER11 Family

POWER10 Family
7nm

POWER9 Family
14nm

POWER8 Family
22nm

POWER7/7+
45/32 nm

Under development...

Up to 60/30 cores/socket
  (240 HW threads)
Modular Building Block Die
New Core uArch
AI-optimized ISA
Energy Efficiency Focus
HW Enforced Security
Enterprise Focus
PowerAXON 2.0
PCIe G5
Memory Clustering

Up to 24/12 cores/die
  (96 HW threads)
Modular new Core uArch
Direct-Attach Memory
OMI Memory
PowerAXON Modular Attach
PCIe G4 / CAPI 2.0
Coherent NVLINK / OpenCAPI
→ #1, #2 Supercomputers

Up to 12 cores/die
  (96 HW threads)
Agnostic Memory
Enterprise Focus
Big Data Optimized
PCIe G3 / CAPI / NVLINK
→ OpenPOWER

Multi-core Optimized
Up to 8 cores/die
  (32 HW threads)
eDRAM L3 Cache

2010   **2014**   **2017+**   **2021=TBC**

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POWER10 Design Focus

Data Plane Bandwidth, Capacity, Composability, Scale
Terabyte/second sockets, Petabyte system memory capacities, 16-socket SMP → Clusters

Powerful Enterprise Core
New Core Architecture, Flexibility, Larger caches, Reduced Latencies

End-to-end Security
Hardware enabled and co-optimized with PowerVM hypervisor

Energy Efficiency
3x improvement over POWER9

AI-Infused Core
10-20x matrix-math performance / socket compared to POWER9

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POWER10 Processor Chip

Technology and Packaging: ⭐ ⭐
- 602mm² 7nm Samsung (18B devices)
- 18 layer metal stack, enhanced device
- Single-chip or Dual-chip sockets

Computational Capabilities:
- Up to 15 SMT8 Cores (2 MB L2 Cache / core)
  (Up to 120 simultaneous hardware threads)
- Up to 120 MB L3 cache (low latency NUCA mgmt)
- 3x energy efficiency relative to POWER9
- Enterprise thread strength optimizations
- AI and security focused ISA additions
- 2x general, 4x matrix SIMD relative to POWER9
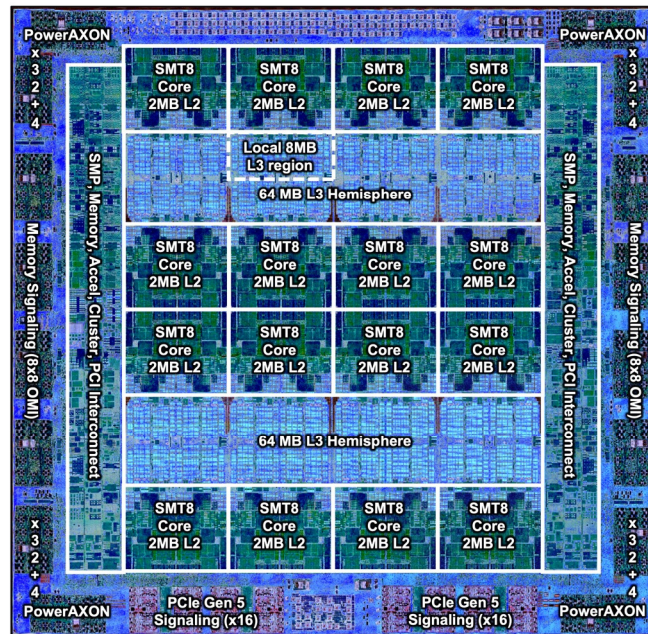- EA-tagged L1 cache, 4x MMU relative to POWER9

Open Memory Interface:
- 16 x8 at up to 32 GT/s (1 TB/s)
- Technology agnostic support: near/main/storage tiers
- Minimal (< 10ns latency) add vs DDR direct attach

PowerAXON Interface:
- 16 x8 at up to 32 GT/s (1 TB/s)
- SMP interconnect for up to 16 sockets
- OpenCAPI attach for memory, accelerators, I/O
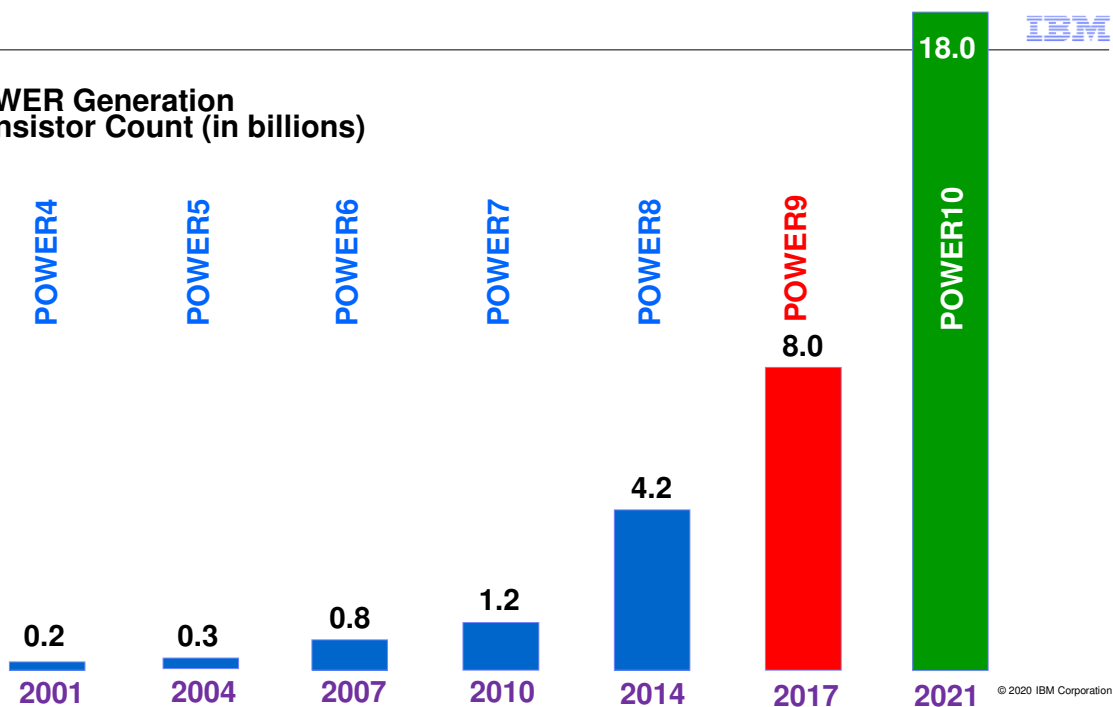- Integrated clustering (memory semantics)

PCIe Gen 5 Interface:
- x64 / DCM at up to 32 GT/s

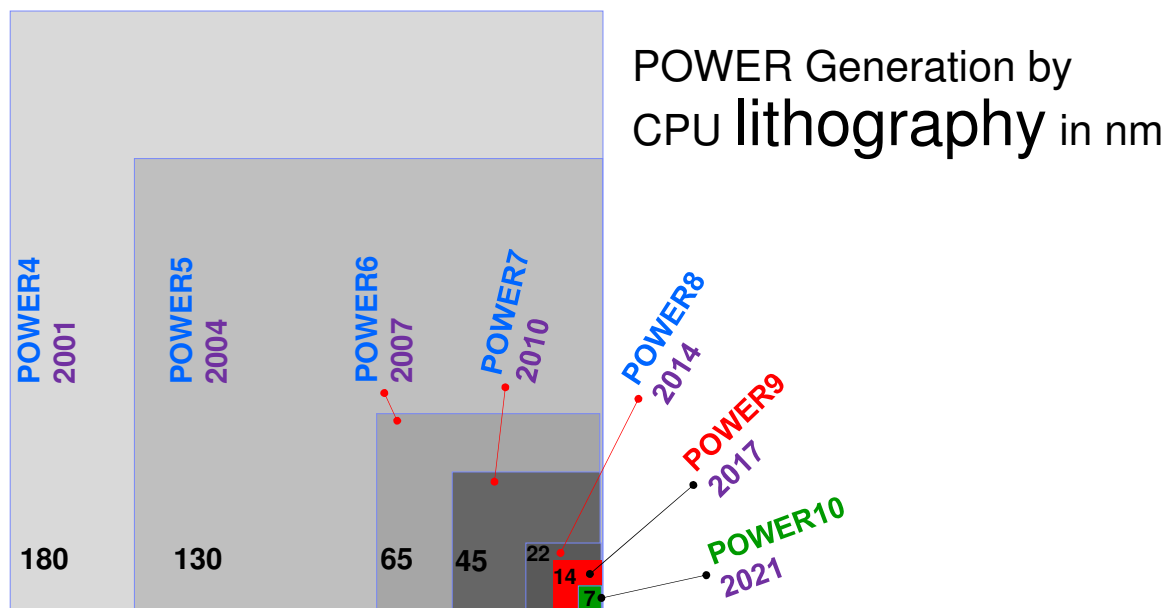Die Photo courtesy of Samsung Foundry

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POWER Generation
Transistor Count (in billions)

POWER4	POWER5	POWER6	POWER7	POWER8	POWER9	POWER10
0.2	0.3	0.8	1.2	4.2	8.0	18.0
2001	2004	2007	2010	2014	2017	2021

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POWER Generation by CPU lithography in nm

POWER4 2001 — 180
POWER5 2004 — 130
POWER6 2007 — 65
POWER7 2010 — 45
POWER8 2014 — 22
POWER9 2017 — 14
POWER10 2021 — 7

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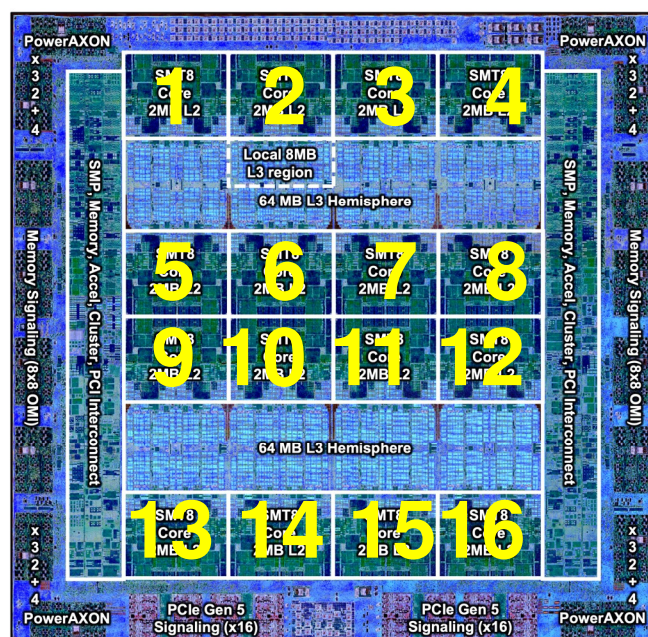- EA-tagged L1 cache, 4x MMU relative to POWER9

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PCIe Gen 5 Interface:
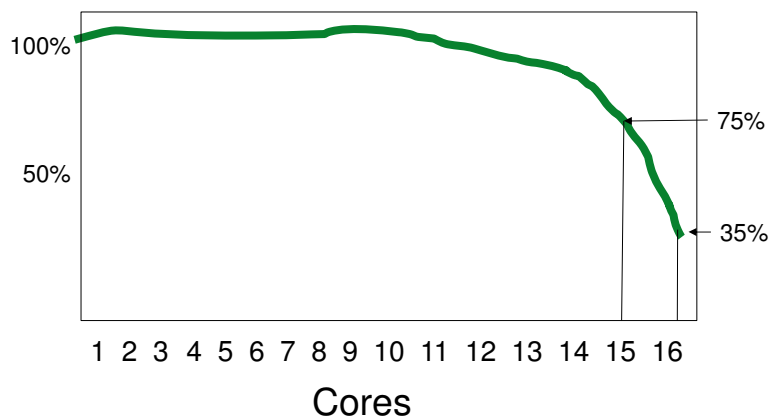- x64 / DCM at up to 32 GT/s

Die Photo courtesy of Samsung Foundry

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Core Yield = not to scale = for illustration purposes only   IBM

POWER chips with the highest numbers of cores are the most popular

By not offering the 16 cores, option, there are a lot more chips available (with the 15 cores)

Over the years of manufacturing yield of the top core chips slowly improve!

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POWER10 Processor Chip

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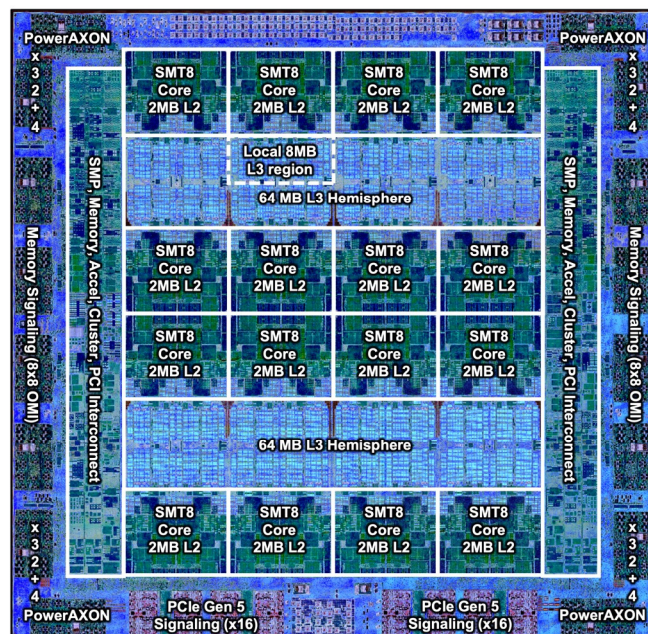- 16 x8 at up to 32 GT/s (1 TB/s)
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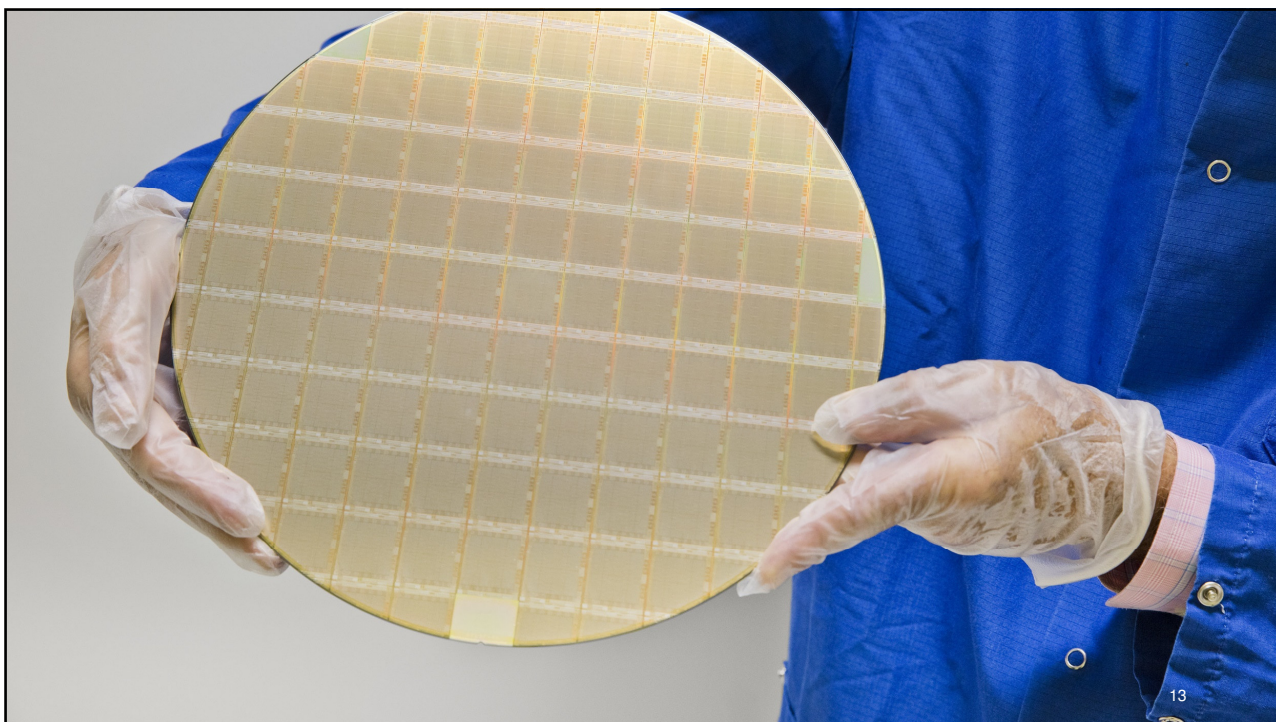- Integrated clustering (memory semantics)

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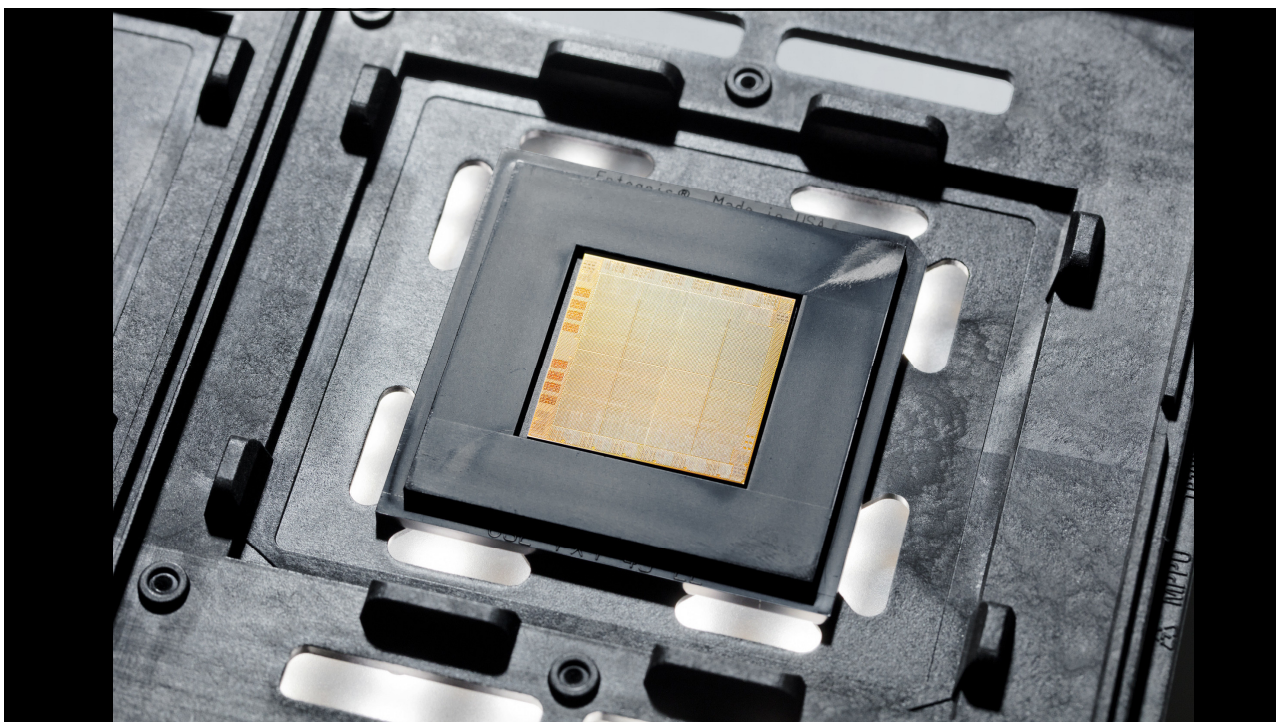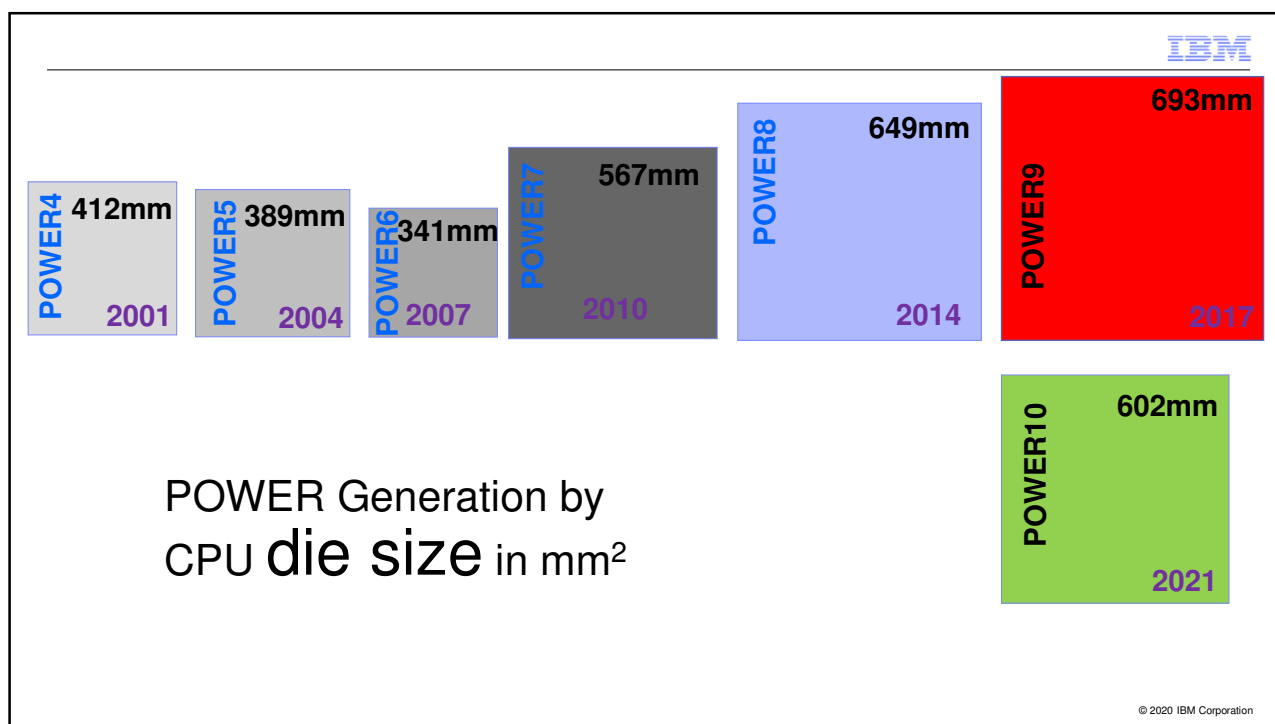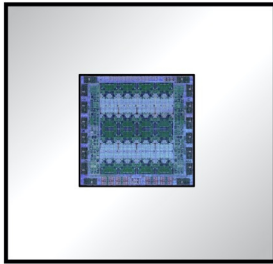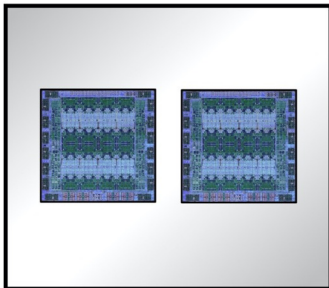Die Photo courtesy of Samsung Foundry

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POWER Generation by
CPU die size in mm²

16

Socket Composability: SCM & DCM
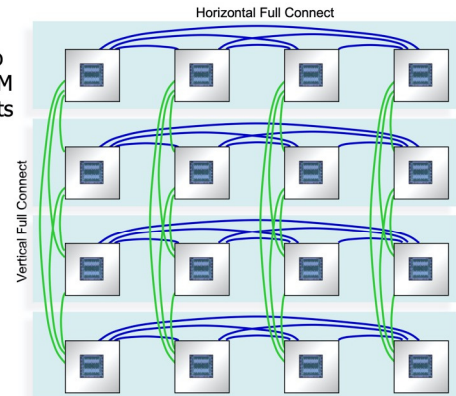

Single-Chip Module Focus:
- 602mm^2 7nm (18B devices)
- **Core/thread Strength**
  - Up to 15 SMT8 Cores (4+ GHz)
- **Capacity & Bandwidth / Compute**
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x128 @ 32 GT/s
  - I/O: x32 PCIe G5
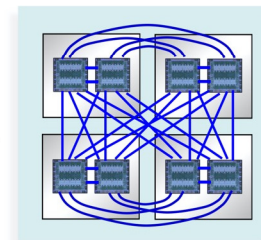- **System Scale (Broad Range)**
  - 1 to 16 sockets

Dual-Chip Module Focus:
- 1204mm^2 7nm (36B devices)
- **Throughput / Socket**
  - Up to 30 SMT8 Cores (3.5+ GHz)
- **Compute & I/O Density**
  - Memory: x128 @ 32 GT/s
  - SMP/Cluster/Accel: x192 @ 32 GT/s
  - I/O: x64 PCIe G5
  - 1 to 4 sockets

(Multi-socket configurations show processor capability only, and do not imply system product offerings)

Horizontal Full Connect

Vertical Full Connect

Up to 16 SCM Sockets

Up to 4 DCM Sockets

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System Composability: PowerAXON & Open Memory Interfaces

Multi-protocol "Swiss-army-knife" Flexible / Modular Interfaces
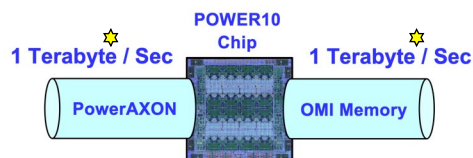
POWER10 Chip

1 Terabyte / Sec — PowerAXON | OMI Memory — 1 Terabyte / Sec

PowerAXON corner 4x8 @ 32 GT/s

OMI edge 8x8 @ 32 GT/s

Built on best-of-breed Low Power, Low Latency, High Bandwidth Signaling Technology
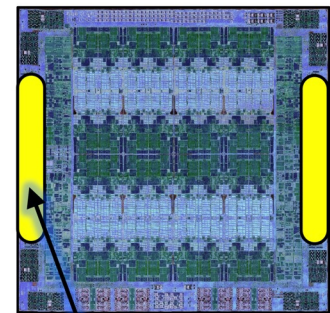
6x bandwidth / mm^2 compared to DDR4 signaling

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System Enterprise Scale and Bandwidth: SMP & Main Memory

Multi-protocol
"Swiss-army-knife"
Flexible / Modular Interfaces

Initial Offering:
Up to 4 TB / socket
OMI DRAM memory
410 GB/s peak bandwidth
(MicroChip DDR4 buffer)
< 10ns latency adder

Build up to 16 SCM socket
Robustly Scalable
High Bisection Bandwidth
"Glueless" SMP

Allocate the bandwidth
however you need to use it

POWER10
Chip

1 Terabyte / Sec   **1 Terabyte / Sec**

PowerAXON   **OMI Memory**

SMP Interconnect   Main tier DRAM

Built on best-of-breed
Low Power, Low Latency,
High Bandwidth
Signaling Technology

DIMM swap upgradeable:
DDR5 OMI DRAM memory
with higher bandwidth
and higher capacity

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)

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Future Memory 101

DIMM DDR4
- Parallel
- Clunky protocol
- Available for a few year

OMI
- Open Memory Interface
- MicroChip DDR4 buffer
- Serial interface (fewer pins)
- Smaller = less space
- Just became available

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System Composability: PCIe Gen 5 Industry I/O Attach

Memory Cluster

3D Memory(HBM)   Silicon die
Base die   PKG Substrate
Interposer

GDDR fast memory
~ 800 MB/s

Integrated Memory Clustering

POWER10 Chip

1 Terabyte / Sec   **1 Terabyte / Sec**

High bandwidth GDDR DIMM

Accelerated App
ASIC or FPGA

SCM

OpenCAPI Attach

PowerAXON   **OMI Memory**

Main tier DRAM

OMI Buffered RAM ~410 MB/s DDR4→DDR5 4 TB per socket

SMP Interconnect

Storage class

SCM

PCIe G5

Storage Class Memory (SCM) Larger & persistent

Adapters mix of Gen5, Gen4, Gen3

(PowerAXON and OMI Memory configurations show processor capability only, and do not imply system product offerings)
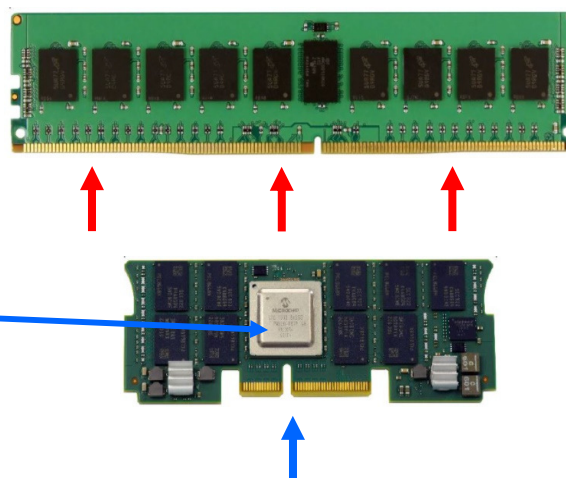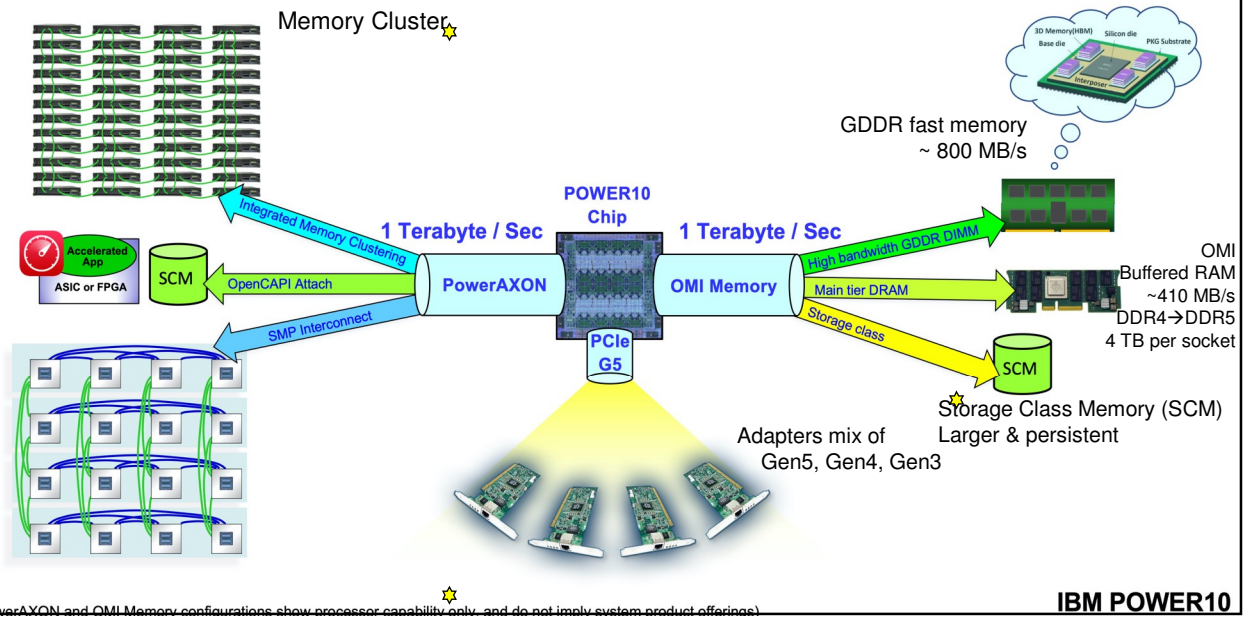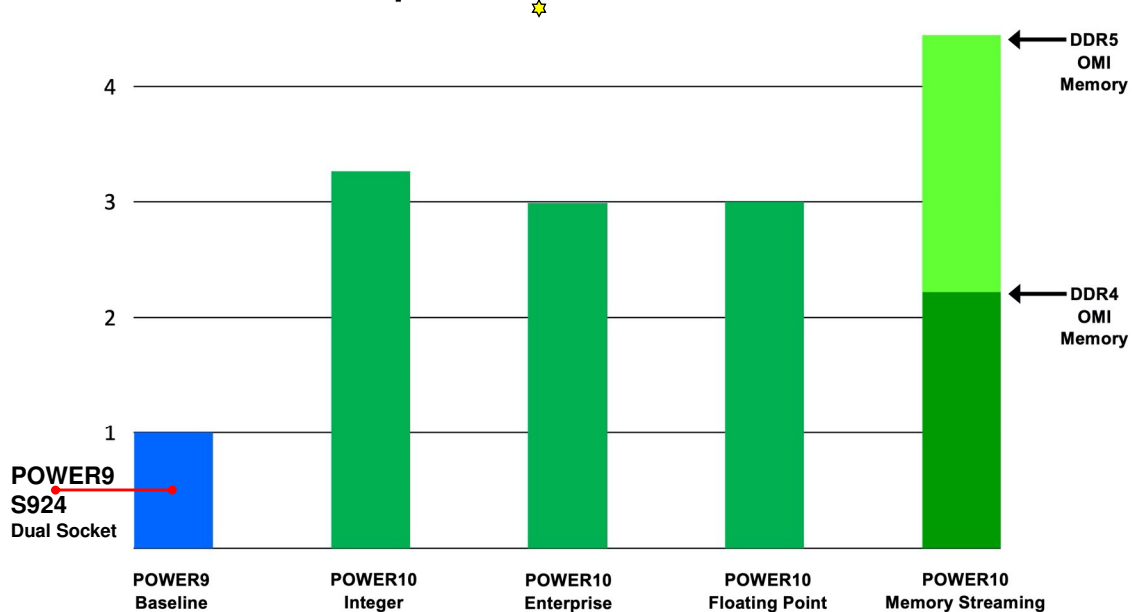
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POWER10 General Purpose Socket Performance Gains

	DDR5 OMI Memory
	DDR4 OMI Memory

POWER9 S924 Dual Socket

4

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1

POWER9 Baseline | POWER10 Integer | POWER10 Enterprise | POWER10 Floating Point | POWER10 Memory Streaming

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)

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More Details

▪ May be more details than you really want!

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Powerful Core : Enterprise Flexibility

Multiple World-class Software Stacks

Resilience and full stack integrity
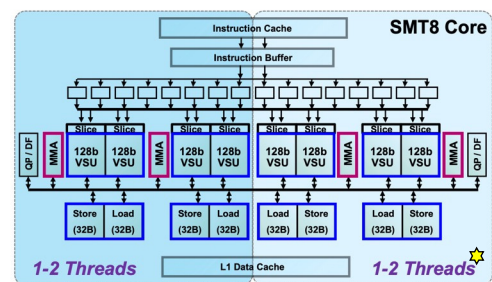- PowerVM, KVM
- AIX, IBMi, Linux on Power, OpenShift
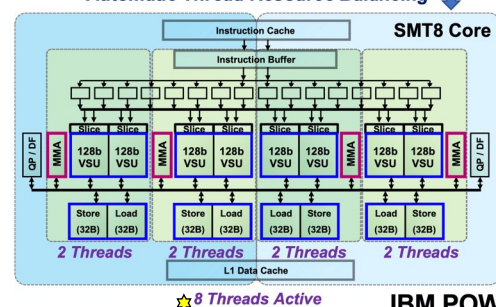
Partition flexibility and security
- Full-core level LPAR
- Thread-based LPAR scheduling
- *NEW*: With PowerVM Hypervisor
  - Nested KVM + PowerVM
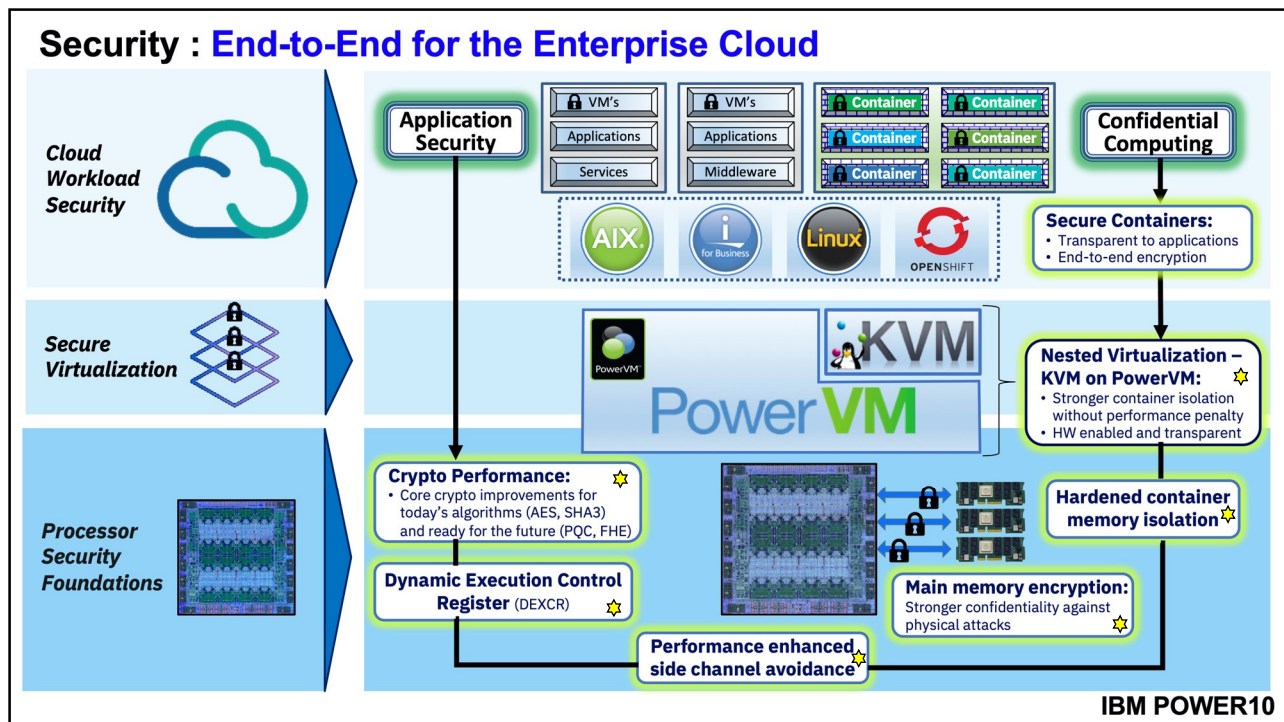 - Hardware assisted container/VM isolation

Hardware Based Workload Balance

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Security : End-to-End for the Enterprise Cloud

Cloud Workload Security

Application Security

VM's — Applications — Services

VM's — Applications — Middleware

Container — Container — Container — Container — Container — Container

Confidential Computing

AIX — i for Business — Linux — OPENSHIFT

Secure Containers:
- Transparent to applications
- End-to-end encryption

Secure Virtualization

PowerVM — KVM — PowerVM

Nested Virtualization – KVM on PowerVM:
- Stronger container isolation without performance penalty
- HW enabled and transparent

Processor Security Foundations

Crypto Performance:
- Core crypto improvements for today's algorithms (AES, SHA3) and ready for the future (PQC, FHE)

Dynamic Execution Control Register (DEXCR)

Hardened container memory isolation

Main memory encryption: Stronger confidentiality against physical attacks

Performance enhanced side channel avoidance

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POWER10 Servers

- Assumes some familiarity with the POWER9 servers

- Public POWER10 presentations make references to POWER10 servers with two, four and sixteen sockets

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POWER9 Servers

Enterprise

2U or 4U
1 or 2 socket
SCM 12 cores SMT=8
4 to 24 cores
4TB RAM

4U
2 or 4 socket
SCM 12 cores SMT=8
16 to 48 cores
16TB RAM

7U to 22U
4 to 16 socket
SCM 12 core
SMT=8
8 to 192 cores
64TB RAM

Scale-Out

S924

S922

Midrange

E950

E980

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POWER9 Servers

Enterprise

2U or 4U
1 or 2 socket
SCM 12 cores SMT=8
4 to 24 cores
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8 to 192 cores
64TB RAM

Scale-Out

S924

S922

Midrange

E950

E980

POWER8 and **POWER9** had a similar set of servers
Well understood and popular with clients
Let us **assume** that this continues . . . for **POWER10**
This is NOT an IBM statement but Nigel guesswork

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POWER9 Servers

Enterprise

2U or 4U
1 or 2 socket
SCM 12 cores SMT=8
4 to 24 cores
4TB RAM

4U
2 or 4 socket
SCM 12 cores SMT=8
16 to 48 cores
16TB RAM

7U to 22U
4 to 16 socket
SCM 12 core
SMT=8
8 to 192 cores
64TB RAM

Scale-Out

S924

S922

Midrange

E950

E980

2U or 4U with 1 or 2 sockets
DCM 15 cores SMT=8
Up to 60 cores
OMI RAM
PCIe Gen5 + Gen4

Two Dual Chip Module Sockets holding four POWER10 processors with up to 15 cores each = **60** POWER10 cores

POWER10 Servers

This can be deduced from POWER10 chip details via the Hot Chips conference
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POWER9 Servers

Enterprise

2U or 4U
1 or 2 socket
SCM 12 cores SMT=8
4 to 24 cores
4TB RAM

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16 to 48 cores
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8 to 192 cores
64TB RAM

Scale-Out

S924

S922

Midrange

E950

E980
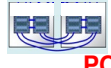
2U or 4U with 1 or 2 sockets
DCM 15 cores SMT=8
Up to 60 cores
OMI RAM
PCIe Gen5 + Gen4

4U with 4 sockets
DCM 15 cores SMT=8
Up to 120 cores
OMI RAM
PCIe Gen5

4 DCM Sockets 8 POWER10's
15 cores = **120** POWER10 cores

POWER10 Servers

This can be deduced from POWER10 chip details via the Hot Chips conference
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POWER9 Servers

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POWER9

Enterprise

2U or 4U
1 or 2 socket
SCM 12 cores SMT=8
4 to 24 cores
4TB RAM

4U
2 or 4 socket
SCM 12 cores SMT=8
16 to 48 cores
16TB RAM

7U to 22U
4 to 16 socket
SCM 12 core
SMT=8
8 to 192 cores
64TB RAM

Scale-Out

S924

Midrange

E950

**240
POWER10
cores**

S922

E980

2U or 4U with 1 or 2 sockets
DCM 15 cores SMT=8
Up to 60 cores
OMI RAM
PCIe Gen5 + Gen4

4U with 4 sockets
DCM 15 cores SMT=8
Up to 120 cores
OMI RAM
PCIe Gen5

22U with 4 to 16 sockets
SCM 15 cores SMT=8
Up to 240 cores
OMI RAM
PCIe Gen5

**This can be deduced from POWER10 chip
details via the Hot Chips conference**

POWER10 Servers

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Reminder – this is not an announcement

From public facts on the POWER10 processor chips
+ some assumptions
+ some guesswork

POWER8 and **POWER9** had a similar set of servers
Well understood and popular with clients
Let us assume that this continues . . . for POWER10
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Powerful Core = Enterprise Strength + AI Infused

Slim cores
OpenPOWER only

New Enterprise Micro-architecture

- Flexibility
  - Up to 8 threads per core / 240 per socket
- Optimized for performance and efficiency
  - +30% avg. core performance*
  - +20% avg. single thread performance*
  - 2.6x core performance efficiency* (3x @ socket)

1-2 POWER10 chips per socket
- Up to **30 SMT8 Cores**
- Up to **60 SMT4 Cores**

AI Infused

- 4x matrix SIMD acceleration*
- 2x bandwidth & general SIMD*
- 4x L2 cache capacity with improved thread isolation*
- New ISA with AI data-types

SMT8 Core

New ISA Prefix Fusion | 4x Matrix SIMD | Enhanced Control & Branch
2x General SIMD
2x Load, 2x Store 4x MMU
4x L2 Cache

* versus POWER9

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)

IBM POWER10

Powerful Architecture : AI Infused and Future Ready

Instruction Set Architecture ISA
→ 200+ more instructions

POWER10 implements Power ISA v3.1

- v3.1 was the latest open Power ISA contributed to the OpenPOWER Foundation: Royalty free and inclusive of patents for compliant designs

OpenPOWER

POWER10 Architecture – Feature Highlights		
Prefix Architecture	Greatly expanded opcode space, pc-relative addressing, MMA masking, etc.	RISC friendly 8B instructions including modified and new opcode forms. PO=1 M Prefix PO Suffix
New Instructions and Datatypes	New Scalar instructions for control flow, and operation symmetry	Set Boolean extensions; quad-precision extensions; 128b integer extensions; test LSB by byte; byte reverse GPR; int mul/div modulo; string isolate/clear; pause, wait-reserve.
	New SIMD instructions for AI, throughput and data manipulation	32-byte load/store vector-pair; MMA (matrix math assist) with reduced precision; bfloat-16 converts; permute variations: extract, insert, splat, blend; compress/expand assist; mask generation; bit manipulation.
Advanced System Features and Ease of Use	Storage management	Persistent memory barrier / flush; store sync; translation extensions.
	Debug	PMU sampling, filtering; debug watchpoints; tracing.
	Hot/Cold page tracking	Recording for memory management.
	Copy/Paste extensions	Memory movement; continued on-chip acceleration: Gzip, 842 compression, AES/SHA.
Advanced EnergyScale	Adaptive power management	Additional performance boost across the operating range.
Security for Cloud	Transparent isolation and security for enterprise cloud workloads	Nested virtualization with KVM on PowerVM; secure containers; main memory encryption; dynamic execution control; secure PMU.

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POWER10 SIMD / AI Socket Performance Gains

	1	5	10	15	20
POWER9 Baseline	▮				
POWER10 Linpack					
POWER10 Inference (Resnet-50) FP32					
POWER10 Inference (Resnet-50) BFloat16					
POWER10 Inference (Resnet-50) INT8					

(Performance assessments based upon pre-silicon engineering analysis of POWER10 dual-socket server offering vs POWER9 dual-socket server offering)

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Summary for Regular Techies

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POWER10 Speeds and Feeds Summary

Performance Gains
  POWER10 with 15 cores = 25% Jump
   + Dual Chip Modules with 30 CPU cores = 100% Jump
   + CPU core thread strength (SMT=8) improvement = 20% Jump
  = POWER10 servers are going to be

~3 times faster

With PowerAXON, OMI, PCIe Gen5 scaling and NVMe disks
  - No internal bandwidth limitations to slow down the processor

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POWER10 Speeds and Feeds Summary

Given:
    same size servers &
    expected similar electricity use &
    higher performance
  = **Superb Green Credentials** (transactions per Watt)

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POWER10 Client Practical Benefits

Stronger (faster) Cores and Threads
- Reduce core counts = reduced Software Licence costs

Larger Virtual Machines per server
- Scale-out: two 10 core VM plus VIOSs ➜ two 28 core VMs plus VIOSs
- Mid-range: two 20 core VM plus VIOSs ➜ two 58 core VMs plus VIOSs
  - Larger VM = faster Apps = less performance issues = reduced SysAdmin

More Virtual Machines per server
- Scale-out: two 10 core VM plus VIOSs ➜ seven 8 core VMs plus VIOSs
- Mid-range: two 20 core VM plus VIOSs ➜ seven 16 core VMs plus VIOSs plus spare 4 cores
  - More VM per server = consolidation of servers = less SysAdmin time
  - Reduced rack space/floor space, electricity, network connections

Other arguments require prices and rPerf/CPW for comparisons

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Questions?

No questions on
- Dates
- Prices
- Performance
- rPerf or CPW ratings
- GHz
- Model names
- Future Lotto
    winning numbers!

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