IBM Deep Computing Team

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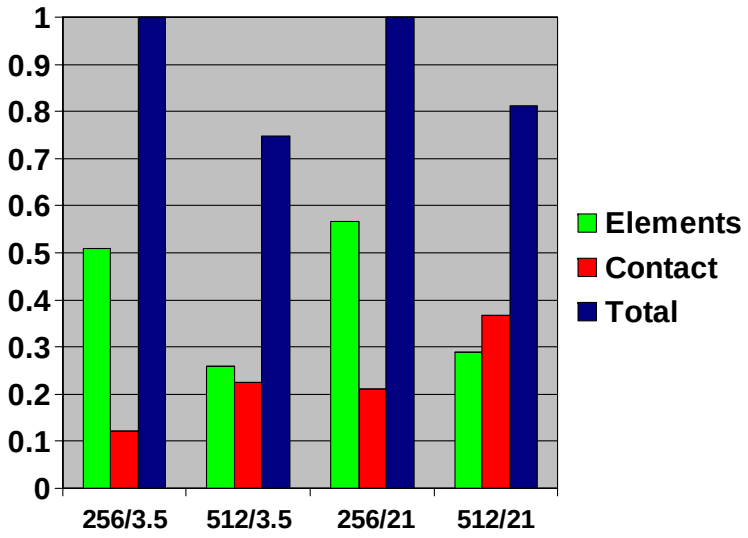
Why Push Parallelism?

- **Model size and complexity continues to grow about 25% a year**
  - **Processor (core) performance is not longer keeping pace**
- **Economic of manufacturing is requiring shorter product development cycles**
- **Increased parallelism is simplest solution**
  - **Apart from increased application complexity**

10M Benchmark: *Simulation Length & Processor Count*

- **Benchmark**
  - PAM-CRASH 2006.0
  - System P p575+ (1.9GHz|16-way) High Speed Switch
  - 256-way, 512-way parallel

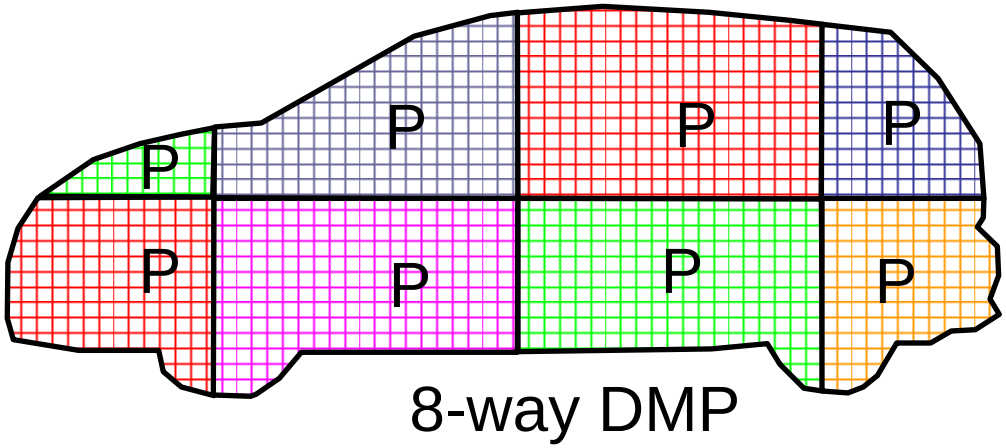


	256-way 3.5msec	256-way 21msec	512-way 3.5msec	512-way 21msec
Cycles	37,669	231,468	37,678	231,483
Int. Forces	2,586	15,935	1,318	8,130
Nodal ops	713	2,915	395	1,933
Output	90	280	50	277
Contact	622	5,886	1,136	10,323
Constraints	396	2,486	217	1,350
Total	5,072	28,125	3,797	22,850

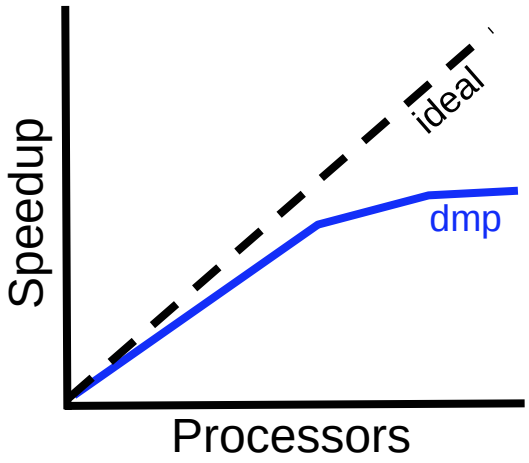
- **Observations**
  - Time step stable first 21 msec
  - Amount of contact work increases as simulation progresses
  - 70 msec guess: ~30 hours (256-way), ~25 hours(512-way)

Why DMP Parallelism Breaks Down

- **Serial portion limits effective speedup (Amdahl's law)**
- **Load imbalance affects performance**
- **Communication can grow with number of data partitions**

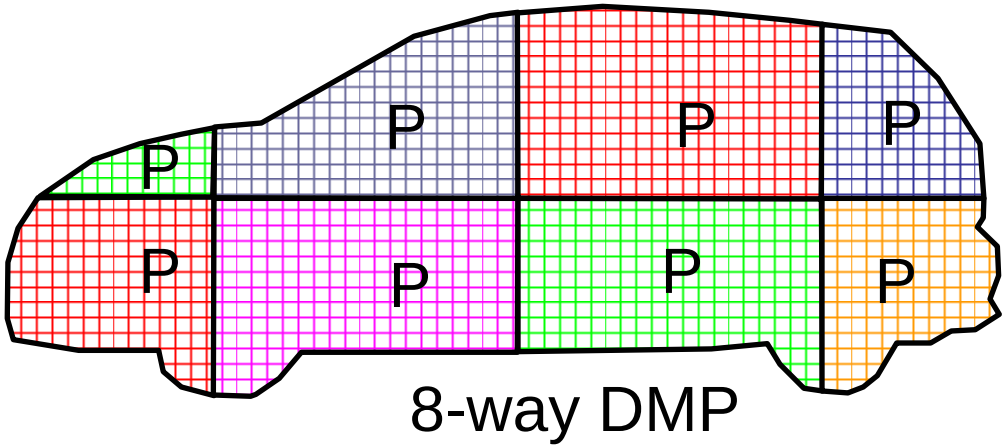


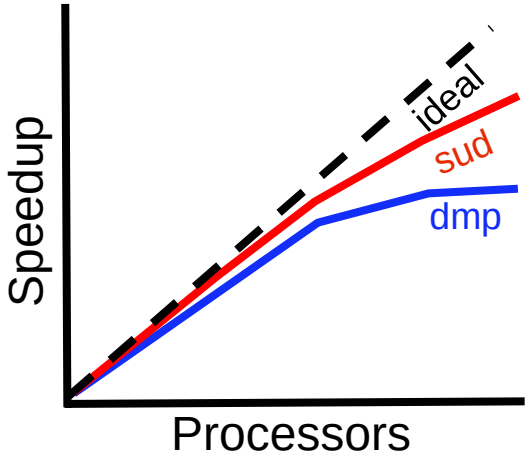
8-way DMP

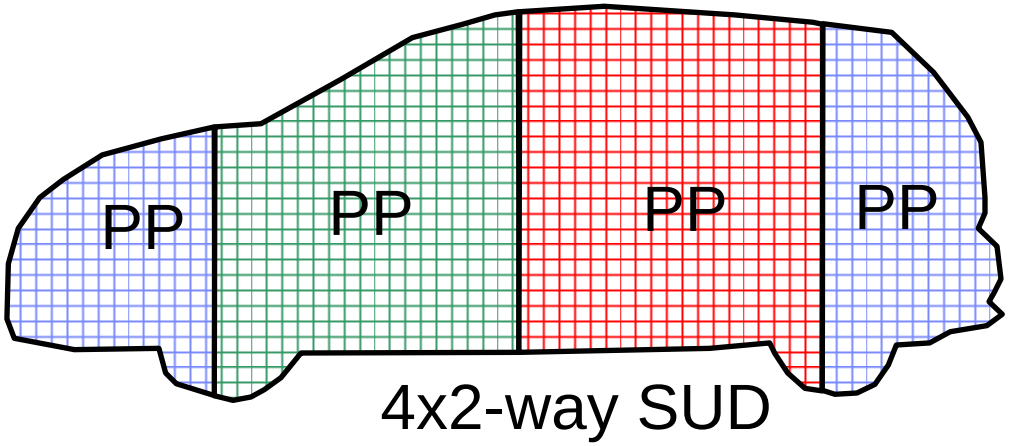


Why Hybrid Parallelism(SUD) Can Help

- **Serial portion limits effective speedup (Amdahl's law)**
  - **Easier to parallelize more of code**
- **Load imbalance affects performance**
  - **SMP can help decrease load imbalance**
- **Communication can grow with number of data partitions**
  - **Number of DMP partitions is decreased**

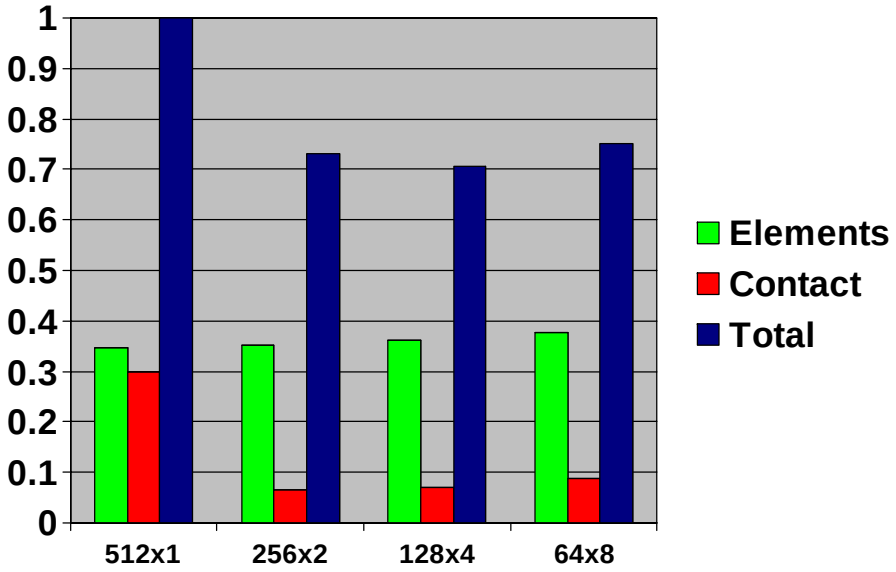






10M Benchmark: *SUD study*

- **Benchmark**
  - PAM-CRASH 2006.0
  - System P p575+ (1.9GHz|16-way) High Speed Switch
  - 512 cores, 3.5 msec simulation

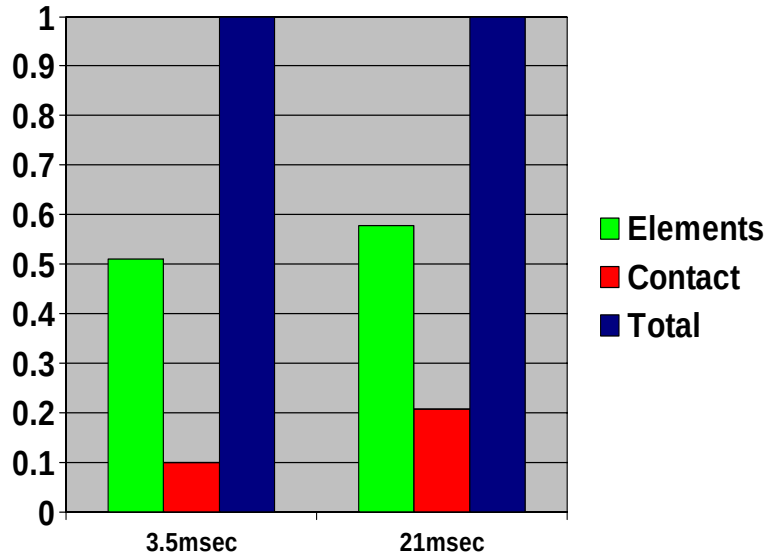


	512x1	256x2	128x4	64x8
Cycles	37,678	37,669	37,668	37,668
Int. Forces	1,318	1,337	1,369	1,430
Nodal ops	395	341	213	244
Output	50	52	74	107
Contact	1,136	250	265	336
Constraints	217	203	222	224
Total	3,797	2,771	2,679	2,840

- **Observations**
  - SUD has minor effect on Internal Force time
  - SUD significantly reduces contact time

10M Benchmark: *Complete run*

- **Benchmark**
  - PAM-CRASH 2006.0
  - System P p575+ (1.9GHz|16-way) High Speed Switch
  - 512 cores (128x4)



	128x4 3.5msec	128x4 70msec
Cycles	37,668	769,236
Int. Forces	1,369	28,014
Nodal ops	213	4,460
Output	74	1,557
Contact	265	9,965
Constraints	222	3,785
Total	2,679	48,420

- **Observations**
  - Complete run possible in < 13 hours
  - SUD about 2X faster than expected DMP time

Discussion

