John Cohn Ph.D.

WORK EXPERIENCE:

2012- Present	IBM Fellow IBM Corporate Technical Strategy
2006- 2012	IBM Fellow IBM Systems and Technology Group. Chief Scientist for Smarter Silicon
2002- 2009	Chief Scientist for Design Automation. Distinguished Engineer IBM Systems and Technology Group Chief Electronic Design Automation Scientist for IBM's Hardware Development
2001- 2002	Electronic Design Automation Group. IBM Microelectronics. Essex Jct. VT Distinguished Engineer, Technical leader of IBM's 400 person internal CAD development team
1991 - 2001	Electronic Design Automation Group. IBM Microelectronics. Essex Jct. VT Senior Technical Staff Member Led the development of a suite of custom design tools used on high performance microprocessors
1981 - 1988	Analog Specials Development IBM Microelectronics. Essex Jct. VT and IBM Hursley Labs UK Advisory Engineer Led CAD development for Analog / Mixed Signal development group

EDUCATION:

1988-1991 Carnegie Mellon University
Ph.D. Computer Engineering
Thesis work in Layout Automation for Analog VLSI
Thesis Published as "Analog Device-Level Layout Automation" Kluwer Press 1991
This work is the basis for the NeoCell product of Neolinear

1977-1981 Massachusetts Institute of Technology
BSEE Electrical Engineering
Thesis work in Device Fabrication
(Includes 1979-1980 at Institut fur Europaische Studiem, Vienna Austria)

ACHIEVEMENTS

- Elected Vermont Academy of Science and Engineering Jan 2011
- Co-starring in "The Colony" technical reality TV show on Discovery Channel beginning 7/21/09, consultant for Colony Season II 2010.
- Elected VP Americas for IBM Academy of Technology 2007
- Appointed IBM Fellow (1 of 63 in the IBM Company)
- Named IBM Burlington Master Inventor
- IEEE Division 1 Award for Service to the Field and Community
- Lead "Pathfinder's Guide to IBM Technical Community project. Coordinated 40 volunteers to create informal guide for recent technical hires. Elected to IBM Academy Technology Council. (12 member leadership of IBM 192,000 member technical community)
- Elected Fellow of the IEEE for contributions to custom circuit design automation
- Appointed Distinguished Engineer - Technical Executive
- Elected IBM Academy of Technology - 300 person technical advisory council to IBM Corporate Technology Council
- IBM Patent supplemental value award
- Appointed State Science Testing Content Committee by VT Sec'y of

Education

- Awarded 3 year IBM Resident Study Ph.D. Graduate Fellowship
- Outstanding Technical Achievement Award for SPAM: sub circuit recognition system
- VT Chamber of Commerce grant for science education
- IEEE grant for robotics in schools program
- Green Scholarship to MIT
- Invited Plenary speaker IEEE International Solid State Circuits Conference (ISSCC) "Kids Today, Engineers Tomorrow ? ", San Francisco, Feb 2009
- Keynote speaker IEEE International Symposium on Circuits and Systems (ISCAS) "Kids Today", Seattle, May 2008

PUBLICATIONS / PRESENTATIONS

- 2 chapters for '**Handbook on Electronic Design Automation for Integrated Circuits'** CRC Press, editors L. Lavaginio, G. Martin
- Tutorial at DAC 2004 "Getting your cool ASIC up to Speed: 2004
- Wrote Chapter in 'Winning the SoC Revolution." Editors G, Martin, E. Liu, Kluwer Press 2003, well reviewed in external press
- Participated in Panel at DAC 2003 "Place Your Bets"… Won audience choice on my positions 2003
- Co-authored: invited paper at ISPD 2003: "There's life left in ASICS"
- Co-authored: invited paper at DAC 2003: getting your cool ASIC up to Speed 2003
- Ran panel at ICCAD – Cad For Cad's Sake" 2002
- Co-authored invited tutorial at ICCAD : AtoZ's of SoC's 2002
- Authored paper at CANDE: Brickwalls and Breakthroughs for SoC's" 2001
- 2001 Invited Panelist Design Automation Conference (DAC2001) "Deep Submicron - Who has nanometer design under control "
- 2001 National Engineers Week Annual Meeting, Smithsonian Museum Washington DC. "Jolts and Volts" Science presentation for 600 kids
- 2000 Invited Panel Moderator Design Automation Conference (DAC2000) "Design on the Bleeding Edge"
- 1999 "Layout Automation for Analog VLSI" with Rob Rutenbar ISPD
- "Computer-Aided Design of VLSI Interconnect", Invited Tutorial International Conf on Computer Aided Design (ICCAD97) (Highest rated tutorial of the conference)
- "Computer-Aided Design of VLSI Interconnect", Invited Tutorial

International Conf on Computer Aided Design (ICCAD96) (Highest rated tutorial of the conference)

- "Layout Automation for Analog Circuits" with R. Rutenbar chapter from upcoming IEEE collection on Analog CAD. Editor B. Antao.
- "Computer-Aided Design of VLSI Interconnect", Invited Tutorial International Conf on Computer Aided Design (ICCAD94)
- "Computer-Aided Design of VLSI Interconnect", Invited Tutorial International Conf on Computer Aided Design (ICCAD93)
- "Analog Device-Level Layout Automation", with D. Garrod, R. Rutenbar, and L. Carley. Published by Kluwer Academic Press.
- "KOAN/ANAGRAM II: New tools for device-level analog layout", IEEE Journal of Solid State Circuits, March 91 (with D.J. Garrod, R. A. Rutenbar, and L. R. Carley)
- "Techniques for simultaneous placement and routing in KOAN/ANAGRAM II", Proceedings of ICCAD 91, Santa Clara CA. (with D.J. Garrod, R. A. Rutenbar, and L. R. Carley)
- "Placement of Analog Circuits in KOAN," Ph.D. dissertation, Carnegie Mellon University. Available as an SRC Tech. Doc.
- "KOAN/ANAGRAM II: New algorithms for device-level analog layout", Proceedings of CICC 1990, Boston, MA. (with D.J. Garrod, R. A. Rutenbar, and L. R. Carley)
- "KOAN/ANAGRAM II: algorithms for custom analog layout", Proceedings of TECHON90, San Jose Ca. (with D.J. Garrod, R. A. Rutenbar, and L. R. Carley)
- "EDIF in IBM", Proceedings of EDIF World, Portland ME.

RECENT ISSUED PATENTS

Approximately 50 patents issued or pending including:

US6832361 System and method for analyzing power distribution using static timing analysis
US6825711 Power reduction by stage in integrated circuit
US6792582 Concurrent logical and physical construction of voltage islands for mixed supply voltage designs

US6751744 Method of integrated circuit design checking using progressive individual network analysis

US6711719 Method and apparatus for reducing power consumption in VLSI circuit

US6687883 System and method for inserting leakage reduction control in logic circuits US6651230 Method for reducing design effect of wearout mechanisms on signal skew in integrated circuit design

US6574779 Hierarchical layout method for integrated circuits

US6523159 Method for adding decoupling capacitance during integrated circuit

US6523154 Method for supply voltage drop analysis during placement phase of chip

US6490708 Method of integrated circuit design by selection of noise tolerant

US6479974 Stacked voltage rails for low-voltage DC

US6473881 Pattern-matching for transistor level netlists

US6430733 Contextual based groundrule compensation method of mask data set

US6429469 Optical Proximity Correction Structures Having Decoupling Capacitors

US6189132 Design rule correction system and method

US5757657 Adaptive incremental placement of circuits on VLSI chip

US5745735 Localized simulated annealing

US5535134 Object placement aid

PROFESSIONAL ACTIVITIES

- Keynote speaker Silicon Seabelt Summit 2011, Fukaoka Japan Feb 2011
- Keynote speaker International Test Conference 2010 , Austin Nov 2010
- Keynote speaker International SEMATECH Manufacturing Initiative Conf , Austin Nov 2010
- Speaker IEEE Region 8 Student Conference, Lueven Belgium Aug 2010
- Invited Plenary Speaker IEEE ISSCC, San Francisco Feb 2009
- Keynote speaker at IEEE ISCAS, Seattle May 2008
- Keynote speaker at ACM World Programming Finals April 2005 Shanghai
- Appointed executive committee of International Conference on Computer Aided Design (ICCAD)

- Adjunct Professor at University of Vermont. Teach Advanced VLSI Systems Design class (EE224)
- Appointed technical committee of International Conference on Computer Aided Design (ICCAD)
- Frequent session chair ICCAD, DAC
- Frequent reviewer IEEE Journal on CAD, IEEE Journal on VLSI
- Multiple Ph.D. committees at University of Vermont, Carnegie Mellon University, Ecole Polytechnique Quebec
- Member Semiconductor Research Corp (SRC) Design Technical Advisory Board
- Contributor to 2001, 2002 International Technology Roadmap for Semiconductors (ITRS)
- Education Officer of Vermont Chapter of IEEE
- Education Officer of VarMIT (VT's own MIT Club)

TEACHING

- University of Vermont School of Engineering
- Instructor of Computer Science, Essex High School (6 week course) Hardware/software co-design project in speech capture.
- Teaching Assistant Carnegie Mellon University (while on Resident Study PhD Fellowship)
- Student English Teacher, Grades 8-12, Waltergasse Gymnasium IV, Vienna, Austria

EDUCATION OUTREACH

- Co-starring in "The Colony" technical reality TV show on Discovery Channel beginning 7/21/09. Show is geared to raise interest in science and technology in general audiences.
- "Inventors Like You" : Kid oriented multimedia presentation/demo in University of NY, New Palz, Yorktown Heights NY, NY Hall of Science NYC (300-800 kids)
- Annual science presentation at Disney Epcot Center
- Traveling jolts and volts science show to kids cross the N.E. (50-200 kids)

- Estimate that I have reached 40,000 kids from 1992-2006
- Shows in more than 50 schools in VT, NY, MA, schools and community groups, museums, etc.
- IBM Kid Days : Burlington, Fishkill, Poughkeepsie, Yorktown, Somers, Armonk, Boston
- Universities: Union, UVM, Columbia, CMU. Boston U. NJIT, MIT
- Museums: National Building Museum, Washington DC. NY Hall of Science

- "High Tension: The Life and Times of Nikola Tesla" multimedia talk/demo for ICCD Conference, Columbia University, Boston University, University of Vermont, VT IEEE, MIT Club of VT,
- 2000-2004 Vermont Governors Institute. Math and Science Lectures
- Science Enrichment Teaching at Williston Elementary School (2 4 week sessions)
- 1992- 2003Vermont Gifted Network science lectures
- Science Enrichment Teaching at Richmond Elementary School (4 7 week sessions)
- Adjunct Professor - University of Vermont. Teaching
  - EE295 "Principles of VLSI System Design" graduate class (I have taught this class for 3 semesters)
  - Guest Lecturer, EE221 Graduate Analog Design Course, Layout Unit

- Elected to the SACC science content testing board in VT. I sit on the group that drafts standardized science tests for the students of VT. Reports to the under-sec'y of education

SKILLS

- Basic inventing. > 40 US patents issued or pending
- Programming in C++,C, Java, PERL,TCL, SCHEME/LISP, TCL, Fortran, PLI
- Electronics fabrication
- Mechanical fabrication
- Basic demonstration chemistry, pyrotechnics

`INTERESTS

Science promotion for K-12
'Weird Science'
CAD for high speed circuit design
CAD algorithm development
Analog, mixed signal design

REFERENCES

Prof. Rob Rutenbar Dept. Of Electrical Engineering Carnegie Mellon University, , Pittsburgh, PA
Prof. Larry Pillegi Dept. Of Electrical Engineering Carnegie Mellon University, Pittsburgh, PA
Dean Domenico Grasso, Department of Engineering, University of Vermont, Burlington Vermont.
Marian Lawlor, IBM State External Programs Coordinator, IBM Essex Junction, Vermont
Nick Donofrio, Senior Vice President of Technology and CTO, IBM Corporation, Somers NY
Linda Reda, IBM/Epcott Center, Orlando, FL
Dr. Bernard Meyerson, Vice President and IBM Fellow, Yorktown Heights, NY