

## IBM System z10™ Mainframe, HP Integrity, No Contest!

## About this White Paper

Since Q4 2008, Hewlett-Packard (*HP*) renewed and sharply increased the volume of its attacks upon IBM's System z10™ mainframe, issuing press releases, critical Web page claims, and new comparisons, all seeking to show that its HP Integrity servers, based on Intel® Itanium® processors, were superior enterprise platforms that were winning away many customers from IBM mainframes.

- Was this the same HP that cast adrift tens of thousands of its loyal server customers when it killed off four longstanding HP business-enterprise server/Microprocessor Unit (*MPU*) architecture families already this decade?
- Were HP talking about the same IBM System z10™ mainframe that has actually gone from market strength to market strength, doubling its high-end server market share to 37% from 2000-2008, and further extending its technology leadership over all enterprise server comers? For the year 2008, System z was 17 points ahead of HP, and also reached a 39% share in Q4 2008. (Gartner Server Market Data Q4 2008, over \$250K servers.)
- Is that the same Intel® Itanium® MPU powering these HP Integrity enterprise servers that was recently described by one leading IT commentator in the words: ***“This continues to be one of the great fiascos of the last 50 years.”***

HP has been successful over recent years in other markets, holding share leadership in PCs and notebooks, printers and imaging, and Industry Standard Servers (*ISS*); three major, high-volume, standard products-focused, price-driven IT segments. So what is going on here? Why so much HP noise about HP Integrity enterprise servers? Why such disrespect for, and denigration of, IBM's resurgent and burgeoning System z10™ mainframe?

Expert mainframe and enterprise system analyst Software Strategies untangles what has been going on here, assesses HP's claims, and shows why IBM's System z10™ mainframes have been winning extra market share, new customer sites, new workloads, and more installed capacity, to HP's considerable detriment.

### Notes:

The < symbol is used throughout this Paper to concisely denote “up to”.

The ~ symbol is also used throughout to denote “about” or “approximately”.

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# White Paper

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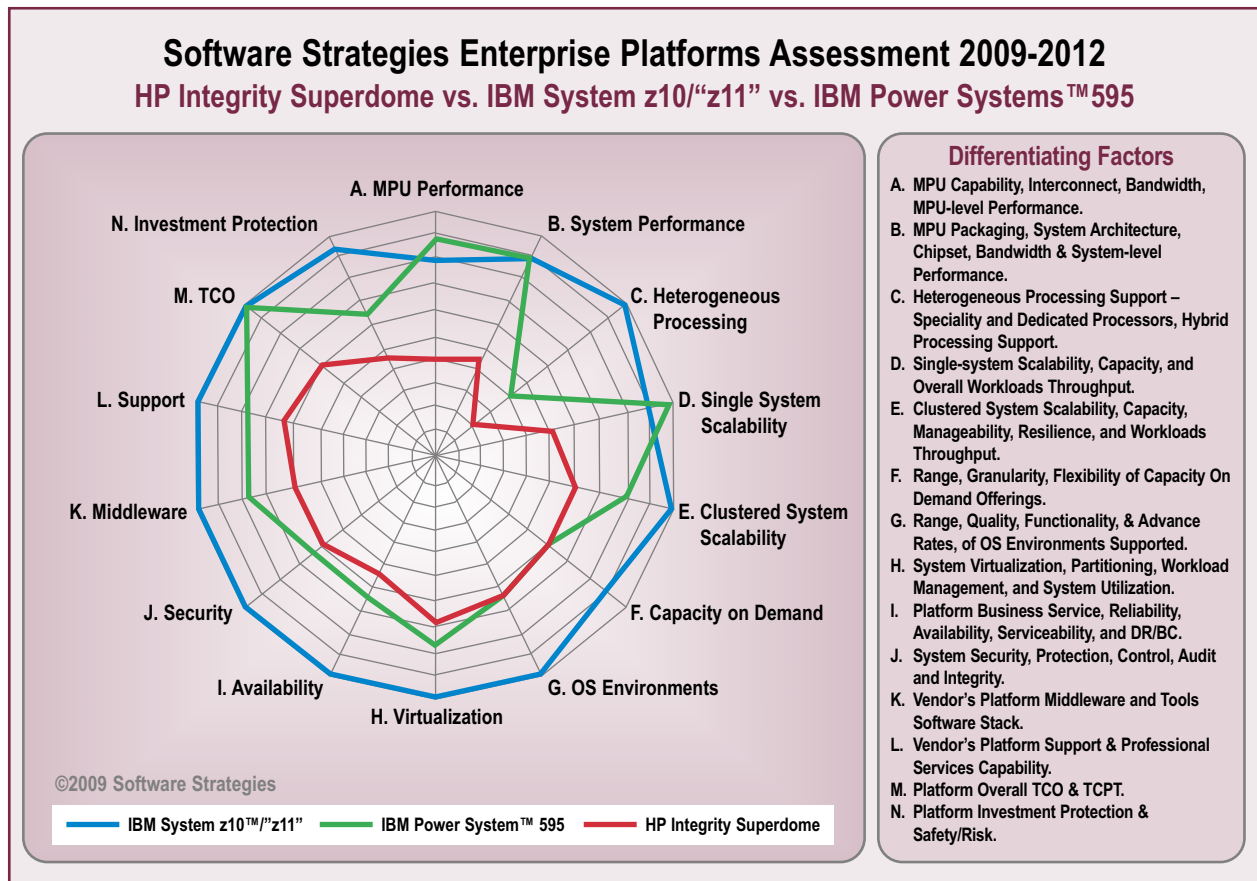
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## 0. White Paper Findings at a Glance

This new White Paper deeply compares and contrasts the resurgent, booming IBM System z mainframe with the HP Integrity server family (powered by much-troubled Intel® Itanium® microprocessors) which HP have, once again, been aggressively promoting as an alternative/replacement. From over 70 pages of in-depth analysis, in which we compared these major enterprise server platforms across the fourteen most important differentiating selection factors for systems of this class, Figure 0 below provides our “at-a-glance” summary of our findings on their high-end systems. The details behind how our ratings were determined are given in this White Paper’s main sections following: especially in Sections 5 and 6.

Our in-depth analysis covered not only the current generation high-end systems, today’s System z10 EC mainframe and HP Integrity Superdome (Intel® Itanium® 9100 Series – Montvale – powered), but also the next-generation System “z11” EC mainframe (expected ~end-Q3 2010) and the next-generation HP Integrity Superdome (Intel® Itanium® Tukwila MC-powered) systems (now delayed again to ~Q2 2010). This means that our analysis and comparisons span over, and are valid for, the 2009 to 2012, next four year time-period, an appropriate time horizon for strategic enterprise platform selection decisions.



**Figure 0: Software Strategies Enterprise Platform Assessment 2009-2012**

To provide a broader comparative view and perspective, our Figure 0 chart analysis also includes our ratings of the market’s performance and price/performance-leading UNIX market enterprise server, the IBM Power Systems™ 595 high-end system, the current generation using IBM’s POWER6 MPUs, and their next generation to soon use IBM’s blockbuster new POWER7 octa-core RISC MPU behemoth.

As Figure 0 shows, the System z EC high-end mainframe remains so far ahead, or so well ahead, of the HP Integrity Superdome high-end servers, on all major comparison factors, as to fully justify our White paper’s main title, **IBM System z10™ Mainframe, HP Integrity, No Contest!** This confirms why the mainframe continues to far lead HP Integrity in enterprise server revenue market share, a lead the mainframe keeps extending.

The IBM Power Systems™ 595 also far outscores the HP Integrity Superdome on most factors, again reflecting IBM’s UNIX revenue market-share-leading position since 2005, and comes much closer to the System z mainframe than the HP Integrity Superdome platform.

# 1. Aggressive HP Attacks IBM Mainframes, Promotes Integrity Servers

## War of Words Heats Up

Hewlett-Packard (HP) attacked IBM's **successful System z mainframe** again from late 2008, promoting its **HP Integrity**, and niche **HP Integrity NonStop**, enterprise server systems. HP's **Business Critical Systems (BCS)** sells/supports these systems. Both HP lines use "lagging-edge" **Intel® Itanium® Microprocessor Units (MPUs)**. (See Section 2.)

This White Paper explains HP's attacks (Section 1), assesses Intel® Itanium® MPU's evolution/roadmap (in Section 2), and reviews today's mainstream HP Integrity family (in Section 3). We recap IBM's latest System z10™ mainframe (Section 4), and review main current and next-generation enterprise server MPUs (Section 5) that power both vendors' enterprise servers. We highlight major differences between these unlike platforms, and give our conclusions (in Section 6).

From late-2008, HP stepped-up attacks on IBM's mainframes again with two provocative press releases (Sources 1 & 2, page 76). These claimed many users had migrated from mainframes onto HP Integrity, both in EMEA and elsewhere worldwide. HP also posted several "The Real Story on..." HP Web pages (Source 3, page 76), also promoting HP Integrity against IBM System z10™ mainframes, touting HP programs/resources soliciting further migrations.

IBM strongly challenged HP's aggressive attacks (Sources 4, 6, and 7, page 76) as did other analysts (for example, Source 8, page 76) for citing old **mainframe myths, drawing doubtful comparisons**, making unjustified assertions, **using partial data**, and skating over deep differences between the IBM and HP platforms. HP was accused of using Fear, Uncertainty and Doubt (**FUD**) **marketing** to promote HP Integrity against IBM's successful System z10™ mainframe.

Mainframe attacks, from HP and other UNIX vendors, have been frequent since the late-1990s. Then, IBM chose dignified silence, but redoubled its intense, \$10B-level innovation/development effort that dramatically advanced mainframe hardware and software through five new generations of 64-bit System z mainframes this decade, far outrunning competing HP and other UNIX vendor advances. IBM added many new, high-value, differentiated enterprise capabilities much faster than competitors added fewer "mainframe-like" features onto their enterprise servers. These intense IBM developments **kept IBM System z mainframes several generations, and c. 5-6 years ahead** of competitors in their capabilities, Qualities-of-Service (QoS), efficiency, automation, and latterly now also in their economics and Total Cost of Ownership (TCO) too.

In 2001, IBM also launched its ultra-high-powered, POWER4-based p Series (p690) top-end UNIX servers, "taking off the gloves" to begin a bare-knuckle fight for the UNIX server market it has since resoundingly won. This big success in UNIX servers, with its resurgent System z mainframes, gave IBM dominant market shares in both these key segments, and thus also in large enterprise servers as a whole (over 50%).

IBM also recently announced (Source 5, page 76) that over 5,000 customers had moved over to IBM Systems and Storage platforms, from HP, Sun, and EMC systems combined, since 2004, striking evidence of IBM systems/storage strengths, these large migration to IBM numbers swamping HP's claims.

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*...over 5,000 customers had moved over to IBM Systems and Storage platforms, from HP, Sun, and EMC systems combined, since 2004...*

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Roused by HP's jabs, IBM also unusually issued public point-by-point refutations (Sources 6 and 7, page 76) of most such HP claims, and powerfully extended its compelling IBM migration offerings. These **Migrate to IBM programs aim to win hundreds more HP (and other vendor) customers** onto IBM platforms. The famous **IBM Migration Factory** now also provides managed migrations from HP UNIX servers to IBM System z10™ mainframes, using well-proven, standardized processes honed by the 1,600+ to IBM Power™ UNIX systems migrations it has completed since 2004.

In this new White Paper, experienced system analysts Software Strategies, authors of many respected IBM System z mainframe hardware and software studies in recent years, (see page 77 for examples), take a broad-ranging look at HP's attacks on the IBM mainframe, and at HP's enterprise systems business. Our review of the MPU foundations of both HP and IBM enterprise platforms is central to this Paper. We also look at the relative strengths of the HP Integrity servers and IBM System z10™ mainframes in a number of key areas, where wide capability differences remain evident.

## Why the Renewed HP Integrity vs. IBM Mainframe Hostilities?

What lies behind this renewed battle of words between HP and IBM? Why is HP now pitching HP Integrity servers into head-on battle with IBM System z10™ mainframes? Server analysts long classed these platforms as falling in different enterprise server segments. Why is HP's Integrity focus straying away from the UNIX server market, the natural category in which it long competed?

We address these questions, and some powerful server market dynamics behind HP's moves, below:

- **HP Integrity – Best Categorized as UNIX Systems:** If it looks like a duck, quacks like a duck, and swims like a duck, it is a duck! HP Integrity servers use the same design, architecture, and build as the HP 9000s before them, with Intel® Itanium® MPUs replacing HP PA-RISC MPUs. HP 9000s were always classed as, and competed with, other UNIX servers. A majority of HP Integrity servers run HP-UX UNIX (*rewritten for Intel® Itanium® Architecture*): others run Linux, a minority OpenVMS, and a handful Microsoft Windows. HP Integrity systems are clearly UNIX servers!! So why is HP now pitching large HP Integrity systems against IBM System z10™ mainframes, rather than against natural UNIX competitors from IBM, Sun, and Fujitsu? **Because HP so badly lost UNIX (and all high-end server) revenue share to IBM! When beaten in your main segment, try another!**
- **UNIX Server and Mainframe Design Points Still Different:** Why do such server categorizations matter? Because design points, priorities, and trade-offs remain different for UNIX servers from those of IBM System z10™ mainframes. Each was optimized for different tasks and workloads, delivers different QoS, with different economic trade-offs, running different software/solution stacks, with different levels of virtualization, Reliability, Availability and Serviceability (RAS), automation, productivity, efficiency, and security, etc. This is why IBM still invests heavily in separate System z10™ mainframes and IBM Power Systems™ RISC-UNIX lines. Together, this IBM duo are today's dominant enterprise server revenue share leaders (*see below for further information*). With these renewed mainframe attacks, HP positions Integrity as single design-point enterprise servers able to fulfill both widely-divergent needs. If top UNIX server attributes could be melded with real System z10™ capabilities in one unified, “do-it-all” enterprise server, IBM would surely have built it by now. Big Blue strove all decade to share server technologies across, and simplify its Systems portfolio with unified MPU and system development teams, to “raise all boasts” and to cut costs. It would have eagerly seized such unification cost savings were they feasible. **IBM's striking high-end server successes refutes the HP Integrity “one-type-fits-all-needs” claims, as do HP's modest market results. But Integrity is now HP's sole mainstream enterprise platform; so this stance is its only choice.**

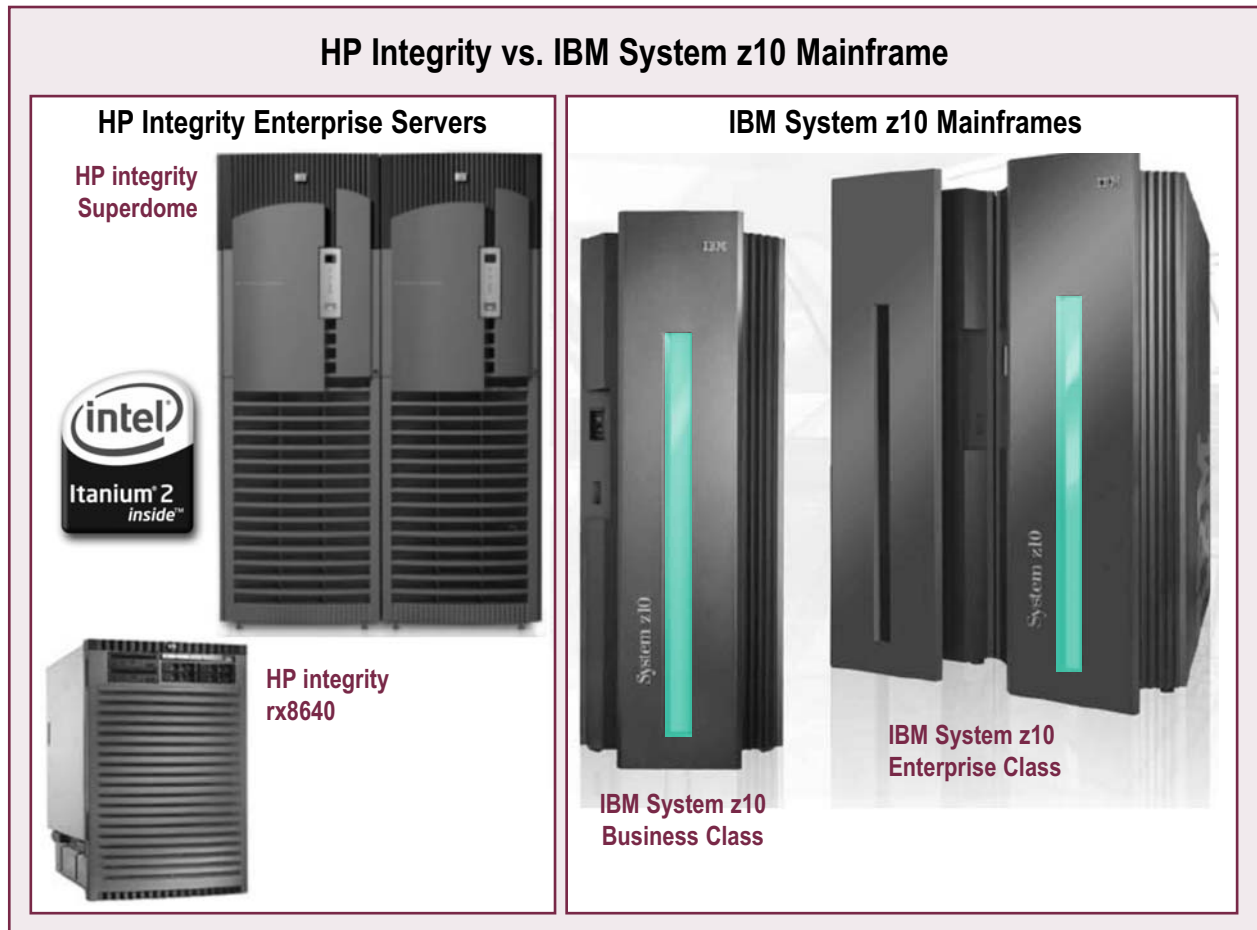


Figure 1: HP Integrity vs. IBM System z10™ Mainframe

- **But HP Integrity NonStop Line Contradicts Its Case:** HP's "one-type-fits-all-needs" Integrity case is also demolished by the continuance of its own esoteric, niche **HP Integrity NonStop** server line. Why is this still needed if mainstream HP Integrity systems really do address all mainframe and RISC-UNIX needs combined – as HP's mainframe attacks argue? HP even created a new Itanium®-MPU-based generation of these closed, proprietary, fault-tolerant enterprise servers from 2005. Why did it bother? They have a completely different architecture, and a different operating system, to those of mainstream HP Integrity, offering only a tiny software stack. Different design points offer different attributes, here to suit the niche Tandem-legacy market, yielding fading revenues to HP as that base decays away. **If HP Integrity were a real IBM System z10™ alternative, why does HP still offer Integrity NonStop? That it does so confirms that different design points are indeed needed!**

*IBM held 37.2% of UNIX server revenue in 2008, versus third placed HP's 26.5%...*

- **HP Lost UNIX Server Market Battle to IBM:** IBM resoundingly won a fierce competitive battle with HP & Sun by seizing and holding revenue share leadership in the still-large UNIX server market since 2005, with top-performing IBM Power Systems™ RISC-UNIX servers. Today, these use **performance-leader IBM POWER6+ RISC MPUs**. IBM held 37.2% of UNIX server revenue in 2008, versus third placed HP's 26.5%, who also lagged behind even struggling, second-placed Sun Microsystems on 28.1%, per IDC. HP's 26.5% share was spread over newer HP Integrity, and (*fast-declining*) legacy HP 9000 and HP AlphaServer sales in an 80/20% split that year. Only IBM grew UNIX revenue share over the last five years, adding a striking 11.2% share points, whilst HP lost 5.7%, and Sun lost 1.9% (*per IDC, August 2008*). **HP 9000/HP Integrity thus lost out to IBM Power Systems™ RISC servers from 2001 to 2009. After Integrity also failed in other segments, mainframes are HP Integrity's last target. Some hope, we found, see below!**

- **Resurgent IBM Mainframe Doubles High-end Server Share This Decade:** IBM enjoyed real success with resurgent 64-bit System z mainframe growth. It invested c. \$10B in five new System z generations between 2000's first z900, and 2008's stunning System z10™, all packed with leadership innovations. It also made major mainframe middleware/tools software investments, including many Independent Software Vendor (*ISV*) acquisitions, creating an unrivalled, leadership software portfolio on System z. This software now better fits System z10™ mainframes to run many crucial enterprise workloads today

*...17% to a 37% enterprise server market revenue share this decade...*

than any other platform. The decade's level and pace of IBM research-driven System z hardware, OS, and especially software, innovations was far higher than in the 1990s. It successfully delivered unique new mainframe capabilities faster than competing UNIX system like HP Integrity, widening System z functional leadership in many areas. Large System z market share gains reflect this, more than doubling from a 17% to a 37% enterprise server market revenue share this decade (*over \$250K servers, between Q2 2000 and Q4 2008, per Gartner Q4 2008 Server Market data*). Installed IBM System z mainframe capacity has also exploded ~8-fold, soaring from 1,800,000 Million Instructions Per Second (*MIPS*) (*Q1 1997*) to 14,300,000+ MIPS (*end 2008 – IBM data*). **Every IBM System z sale, or capacity upgrade, lost a large system opportunity to HP Integrity**, doubtless one driver of HP's renewed mainframe attacks.

- **IBM Dominant in Enterprise Servers Overall:** IBM's victory in UNIX servers (*strongest in mid- to high-end IBM Power Systems™ RISC-UNIX servers*) and the dramatic System z resurgence above, combined to **give IBM dominant 50%+ revenue share leadership in enterprise servers (>\$250K servers)**. For Q3 2008, IBM's share of this crucial segment even reached 57.5% (*Gartner end-2008*). In contrast, HP lost significant high-end enterprise server share to IBM this decade. **HP must now also fight the new Sun/Oracle titan, and all other high-end server vendors, for a shrinking minority share of this high-value market.** When Oracle's acquisition of Sun Microsystems completes as expected, a stronger, and more combative, Sun/Oracle server/software combined competitor's impact will be felt most directly by HP Integrity.

*For Q3 2008, IBM's share of this crucial segment even reached 57.5% (Gartner)...*

- **Cloud Computing Will Increase IBM High-end Server Share:** As the market adopts the cloud computing model over the coming years, centralized, highly-virtualized, efficient resource sharing, highly-secure, and completely reliable cloud host platforms will be needed. IBM's System z10™ mainframes and high-end IBM Power™ UNIX servers are already superbly well-placed, with superior attributes over all competitors, to host most scale-up-friendly cloud computing workloads, as IBM's emerging, new cloud-supportive firmware, virtualization, and systems/services management middleware, are rolled out under its Dynamic Infrastructure and Cloud Computing initiatives.

HP's weaker market share positions, in both UNIX and in the broader overall high-end server segments above, explain its recent attacks on IBM's System z mainframe. **But how important are enterprise servers to HP today? What are HP's real business focuses now?**

## HP Business Critical Systems – Not Critical to HP Business!

HP talks of serving enterprise customers with higher-end systems for mission-critical applications, but how important are Business Critical Systems – the firm's enterprise server business – now mainly HP Integrity and HP Integrity NonStop systems – really to HP? And how did this HP unit perform in recent years business-wise?

HP became world-largest IT company in 2008. It posted an impressive \$118.4B revenue, up a healthy 13.5%, and earned a strong net income of \$8.329B, for the last 2008 Financial Year (FY) ending 31.10.2008. (*Just missing recession impact*). As a company, HP performed impressively over the last six years. Revenues grew from \$73.1B (2003) to \$118.4B (2008) at a strong 10.2% Compound Annual Growth Rate (CAGR), and net earnings soared from \$2.539B to \$8.339B, at a quite splendid 26.9% CAGR over the same period. So what IT markets provided HP's main revenues? For the last 2008 HP FY, the firm's reported segments were ranked:

- # 1: **“Personal Systems Group” (PSG)** – \$42.295B or 35.7% of HP revenue, up 16.1% Year-On-Year (YOY).
- # 2: **“Imaging and Printing Systems” (IPS)** – \$29.385B or 24.8% of HP revenue, up 3.2% YOY.
- # 3: **“HP Services”** – \$22.397B or 18.9% of HP revenue, up 35.2% YOY (*incorporating EDS for one quarter*).
- # 4: **“Industry Standard Systems” (ISS)** unit of Enterprise Storage and Servers (ESS) – \$11.657B or 9.85% of HP revenue, up 2.4% YOY.
- # 5: **“Storage”** unit of ESS – \$4.205B or 3.6% of HP revenue, up 13.5% YOY.
- # 6: **“Business Critical Systems” (BCS)** unit of ESS – \$ 3.538B or 2.99% of HP revenue, down 0.4% YOY.
- # 7: **“HP Software”** – \$3.039B or 2.56% of HP revenue, up 19.7% YOY.
- # 8: **“HP Financial Services” (HPFS)** – \$2.698B, 2.28% of HP revenue, up 15.2% YOY.

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*“Business Critical Systems” ranks far down HP’s size/importance order in a lowly sixth place, with under 3% 2008 FY revenue.*

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HP wisely focused management attention, resources, and investments, on its largest, strongest, and highest-growth, business segments. “Business Critical Systems” ranks far down HP’s size/importance order in a lowly sixth place, with under 3% of the firm’s last 2008 FY revenue. BCS alone also saw a revenue decline in that strong HP results year, barely above

sales of the also relatively small, but strongly growing, HP Software segment.

HP is unquestionably # 1 revenue share leader in PCs today (*with PSG*), is also # 1 in printers/imaging (*with IPG*), and in industry-standard servers, including blade servers (*with its ISS unit*). In these segments, HP competes with fellow volume-product-centered player Dell Computer. IBM plays in neither of those first two high-volume/commodity sectors, but battles fiercely with HP in ISS (x64) and blade servers, both sold only to businesses.

HP will gain # 2 share position in IT services for its 2009 FY, when its full-year EDS acquisition revenue is consolidated, clearly emulating IBM’s successful Global Services, Big Blue’s largest revenue source. The four HP strongholds above, plus an improving storage segment, accounted for \$110.94B, or 93%, of HP 2008 FY revenue; so deserved, and got, most of HP’s Research and Development (R&D), investment, and management attention.

**“Poor relation” BCS is thus far from central nor critical to HP business success** by comparison with far stronger HP segments discussed above. So why does HP persist with it? Why not focus on its leadership strength segments (*PSG, IPG, ISS*), or better margin (*IPG, HP Services*) businesses?

## HP Business Critical Systems Results Easy to Criticize, Going Down

The recent year’s revenue, revenue growth, and share of total company sales, are the best gauges of any business segment’s health. The data in Figure 2 (*on page 9*) thus shows why HP BCS is of low (*and declining*) importance to HP’s leaders and investors for these last six years. Unlike other HP segments, and HP as a whole, all of which grew well, BCS revenue declined over this healthy economic period. It fell sharply from 26.3% of HP ESS revenue in 2003, to just 18.2% in 2008. As a percentage of total HP revenue, BCS almost halved, from 5.25% in 2003, to only 2.99% in 2008. Latest total BCS Q2 2009 FY revenue fell sharply by 29% YTY, with combined HP Integrity revenues down by 18% YTY, far worse than their 5% Q1 2009 FY YTY drop, which first reversed prior years of Integrity growth.

For HP BCS enterprise system customers, these falling revenues and HP revenue shares raise real concerns, and set alarm bells ringing. How much new HP investment, product innovation, and support can users expect from a declining BCS unit shrinking within a growing HP? Rational observers must expect more BCS cost-cutting, lower investment, price rises, and reduced support, opposite to BCS customer wants/needs. In this decade, HP already severely downsized or divested multiple BCS MPU design and server development teams, chip fabrication plants, and trimmed BCS operating system commitments – now cost-cutting is once again a central HP focus in 2009. More of the same ahead for BCS seems highly-likely.



HP FY (to 31.10.0X)	2008	2007	2006	2005	2004	2003
HP BCS revenue \$B	\$3.538	\$3.553	\$3.654	\$3.812	\$3.759	\$3.835
HP BCS % revenue growth/fall YOY	-0.42%	-2.76%	-4.14%	1.41%	-1.99%	–
HP BCS revenue as % ESS	18.2%	19.1%	21.2%	22.8%	24.9%	26.3%
HP BCS revenue as % of HP total	3.0%	3.4%	4.0%	4.4%	4.7%	5.3%
HP ISS revenue \$B	\$11.657	\$11.380	\$9.982	\$9.389	\$8.128	\$7.260
HP ISS % YOY revenue growth	2.4%	14.0%	6.3%	15.5%	12.0%	–

Sources: HP Annual Reports & 10Ks 2003-2008 FY. Segment revenues for HP's Business Critical Systems (BCS) & Industry Standard Systems (ISS) units.

Figure 2: HP's Faltering BCS Revenue

By contrast, HP's ISS server (*much higher-volume, faster advancing Intel/AMD x64 MPU-based, standard servers*) revenues grew by 60.6% over the same six-year period, reaching 3.3 times BCS revenue in 2008 FY, whilst continuing HP's long-standing (*Compaq-inherited*) ISS market leadership in this now-largest server segment.

If HP's Integrity servers were really as great as it claims, surely BCS revenue and revenue share growth (*and not decline*) would have been posted by this HP enterprise system unit over the last 6 years of strong economic growth? **Enterprise systems are a small HP niche, not a central focus, as they undoubtedly remain at IBM, we conclude.**

## Judge System Innovation/Differentiation – Divergent HP & IBM R&D Strategies, \$B Spends

In enterprise systems, innovation, differentiation, capability advances, strong QoS, increased customer value, and best end-to-end TCO, are created by effective, focused, and timely MPU, system, firmware, and software R&D well-combined and tightly integrated together. All these must advance in parallel, and be rapidly deployed in each new wave of enterprise systems that vendors deliver to business customers, on a timely drumbeat. IT markets today expect strong rates of advance, and falling system hardware prices; in this toughly-competitive industry, expectations that pose huge challenges to system vendors. Enterprise system vendor R&D spend rates (*including R&D as a % of revenue*), are important indicators of how much innovation that a vendor's customers can expect, providing R&D and technology strategies are sound, and research results well-implemented. Figure 3 shows HP and IBM \$ R&D investment in each of the last six years – 2003-2008.

Powering System Innovation – IBM & HP R&D Expenditure Compared						
Financial Years	2008	2007	2006	2005	2004	2003
HP R&D \$M	\$3,543	\$3,611	\$3,591	\$3,490	\$3,563	\$3,651
HP R&D % of Revenue	2.99%	3.46%	3.92%	4.03%	4.46%	5.00%
IBM R&D \$M	\$6,337	\$6,153	\$6,107	\$5,842	\$5,874	\$5,314
IBM R&D % of Revenue	6.12%	6.23%	6.68%	6.41%	6.10%	5.96%
IBM R&D \$/HP R&D \$	1.79	1.7	1.7	1.67	1.65	1.46
IBM R&D %/HP R&D %	2.04	1.8	1.7	1.59	1.37	1.19

Sources: IBM Annual Reports 2003-2008, FYs ending 31.12. HP Annual Reports & 10Ks 2003 to 2008, FYs ending 31.10

Figure 3: Powering System Innovation – IBM & HP R&D Expenditure Compared

IBM's R&D quality and effectiveness are legendary. IBM spent from 46% to 79% more than HP yearly between 2003 and 2008, averaging a consistently high 6.0% of IBM revenue over the period. IBM long recorded the most US patents granted to any firm, 3,148 in 2008, more than double 10<sup>th</sup> placed HP's 1,470. Breadth and pace of chip, system, and software innovation from IBM's Systems and Technology Group (STG) and Software Group (SWG) into new IBM systems and software has been quite outstanding this decade, with System z mainframes and IBM Power Systems™ RISC servers major beneficiaries. The market leadership and large share gains both platforms achieved since 2000 clearly highlights how IBM's deep MPU and system innovation R&D drove and enabled these enterprise system's strong successes.

*IBM spent from 46% to 79% more than HP yearly between 2003 and 2008...*

HP has a sound R&D reputation, R&D spend ran flat at (*a still-substantial*) \$3.5B p.a. over the same years, but fell sharply (*by 40%*), from 5.0% of HP revenue in 2003 to just 2.99% of revenue in 2008. This sharp R&D % fall was in line with the consistent “get costs down” and “raise operational efficiency” themes of Mark Hurd’s HP leadership over recent years.

HP’s R&D spend must first support its three largest units, PCS (*PCs*), IPG (*imaging and printers*), and now EDS buy-expanded HP Services, before fourth-ranked ESS, of which BCS is now just a small part, gets a look in. HP BCS’s technology strategy was to divest its MPU design teams, trim server design teams, sell off chip fabrication facilities, and reduce multiple operating systems efforts. Instead came total reliance on Intel (*and AMD*) for MPUs for all HP systems from PCs upwards. BCS suffered years of downsizing as HP sold off, slimmed down, or disbanded multiple MPU, system, and OS development teams (*ex-HP, Compaq, DEC, and Tandem origins*), including transferring its Itanium®/PA-RISC MPU development team across to Intel in 2005.

HP’s falling enterprise server market share, and BCS revenue declines this decade (*discussed above*), suggest this new HP Way – the “consolidation/downsizing/cost-cutting” approach to the enterprise systems business – is yet to achieve resounding success. We doubt it ever will.

## Judge Them by Their Own Words – HP’s Focus & Forte High-volume & Consumer IT Markets

As our above data shows, HP achieved real successes in high-volume, consumer-focused markets for PCs and imaging/printing systems. These, plus major acquisitions (*Compaq, EDS, and Mercury Interactive, etc.*), made HP 2008’s largest technology company. HP’s volume products and consumer market focuses are clearly reflected in the order and emphasis of its “elevator speech”, included on 2009 HP news releases:

***“HP, the world’s largest technology company, provides printing and personal computing products and IT services, software, and solutions that simplify the technology experience for consumers and businesses. HP completed its acquisition of EDS on August 26<sup>th</sup> 2008.”***

“Printing” and “personal computer” products are named first, followed by “IT services”, “software”, and “solutions”. None of the three parts of HP’s ESS business are mentioned at all in this company positioning paragraph. No mention of “enterprise storage”, “business-critical (*enterprise*) systems”, or “industry-standard systems”, a deeply-revealing omission. “Consumers” are mentioned first as HP’s target market, before “businesses”, again confirming HP’s self-perceived consumer market priority. Enterprises should conclude they are not HP’s foremost priority, except when they buy high-volume, standard products like HP’s PCs, printers, and ISS servers. HP clearly chooses to focus on such volume product and consumer markets foremost in its strategy, an entirely valid choice that has proved successful for the firm. However, this renders its avowed commitments to enterprise system markets highly-questionable (*see also below*). Relatively low-technology printer ink cartridges still provide a significant part of HP’s profits!

## No Doubting IBM’s Exclusive Business/Government Customer, Enterprise Systems Focus

In contrast to HP’s split consumer-business personality, all IBM segments today **focus solely on business/government customers**, with legendary enterprise IT customer strength now complemented by 7 years of Small and Medium Business (*SMB*) focus, with no consumer market, or commodity product, distractions. IBM systematically divested high-volume, standard products in commoditizing segments with low margins. These were PCs/laptops (*sold to Lenovo*), standard disk drives (*sold to Hitachi*), printers (*into Lexmark*), and printing services (*to Ricoh*), etc. IBM thus applies 100% of its massive R&D-based innovation output and capital investments exclusively to benefit business customers. Its innovation torrent focuses on higher-margin, high-growth IT services, middleware and tools software, as well as on sharply-differentiated, technologically-advanced, IBM Systems and Storage solutions, optimized for large and small enterprises. All IBM offerings are also highly complementary and synergistic, providing extensive single-stop-shopping for business customers, as well as strong leverage and good integration across business segments.

## Four HP Enterprise Platform User Bases Betrayed – HP BCS’s Proud 2000 Decade!

Behind HP BCS’s declining revenue is how it treated scores of thousands of business/enterprise system customers this decade. Foremost obligation, and wisest business strategy for enterprise system vendors, is to retain customer trust/confidence by carefully preserving enterprise platform investments long-term. The user’s cumulative investments in a system architecture’s hardware, operating systems, vendor middleware software, storage, etc., are just the smaller if more visible parts. Much larger are their decade(s)-long user investments in business applications, databases, and staff skills/knowledge, built up on/around their enterprise platform. Enterprise users rightly expect their deep trust in/reliance on their vendor to be respected, and their major investments to be preserved over decades without disruptive discontinuities.

However, since 2001, HP BCS betrayed such trust/faith at scores of thousands of business/enterprise system customers, inflicting mass destruction of their platform investments in hundreds of thousands of HP servers, and on those users' far larger, associated applications, etc., investments. Since 2001, HP phased out all four of its older, proprietary business IT system/MPU architectures, each now past End Of Sale (EOS) and now past or nearing End-Of-Life (EOL) stages when HP support ceases. These are:

- **HP e3000 – PA-RISC-MPE/XL:** Popular, widely-used, HP integrated mid-range proprietary minicomputer line, built from 1971-2006, with last HP support ceasing at end-2010. HP PA-RISC MPUs powered these minis for the last decade of their life, over 300,000 were sold, and the HP e3000 was the main IBM AS/400/System i competitor. HP e3000 customers were abandoned with no software-compatible HP migration path offered. HP roadmaps suggested moves to incompatible HP 9000/HP Integrity HP-UX systems (*themselves in transition*), or to also incompatible HP ProLiant x64 MPU servers running Windows/Linux!
- **HP 9000-PA-RISC-HP-UX:** HP's main enterprise server brand, built from 1984-2008. Successful, sometime UNIX server market leader, HP PA-RISC MPU-powered, proprietary enterprise servers (*and originally workstations*) spanning entry-level to top-end enterprise Symmetric Multiprocessing (SMP) servers. HP 9000s all ran HP-UX proprietary UNIX, are now all past EOS, with HP End-of-Support at end-2013. Similar HP Integrity (*Itanium/EPIC*) systems, launched in 2003 (*and reviewed fully in Section 3*), were the cross-MPU architecture migration path HP offered to HP 9000 users.
- **HP AlphaServer-Alpha RISC-Tru64 UNIX & OpenVMS:** High-performance Alpha RISC-MPU-powered server line inherited by HP via the 2002 Compaq buy, originally DEC-developed. Alpha RISC chips were often the highest-performing RISC MPUs in the 1990s. AlphaServers were shipped from 1994 to 2007 (*April*), and HP support finishes at end-2012. HP Integrity was again the proposed HP migration path for these users. However, HP cancelled its promised port of major Tru64 UNIX features into HP-UX for HP Integrity, forcing Tru64 UNIX AlphaServer users into unwelcomed cross-MPU/systems architecture/OS transitions. However, the other AlphaServer OS, OpenVMS, was ported to HP Integrity by 2005, and is still supported today by HP for the firm's "VAX-legacy" customers.
- **HP NonStop-MIPS RISC-NonStop OS Systems:** Specialized, HP proprietary, fault-tolerant, MPP (*Massively Parallel Processing*) enterprise platform long powered by MIPS RISC MPUs. Also inherited by HP from the 2002 Compaq acquisition, and originally Tandem-developed. Their Tandem MIPS NonStop forerunners were built from 1986, and the last HP NonStop (MIPS) units were shipped in 2008. HP Integrity NonStop (*Itanium®-powered*) systems were the proposed migration routes, the first of these were launched from 2005, and now cover that platform's full range.

Little surprise thousands of HP BCS customers, deeply invested in these platforms, were unhappy at HP's plans. Many found HP migration roadmaps involved disruptive discontinuities and complex, costly migrations, resulting in the destruction of customer platform investments. Their negative feelings were compounded by the under-performing, belated delivery HP Integrity replacements that HP offered. Many customers voted with their feet (*see below*). In fairness, HP arguably had little choice but to rationalize the overlapping legacy enterprise platforms it inherited, and has provided lengthy transition processes and support in a professional manner over many years.

## Our Analysis – Thousands of HP BCS System Users Flee

HP BCS abandonment of these four proprietary system platforms angered thousands of its own customers. Intel's repeated delays in delivering each Itanium® MPU generation (*see Section 2*) delayed each HP Integrity server generation pro rata, and resulted in relatively uncompetitive system performances when each finally shipped. (*See Section 3.*)

*HP BCS users deeply reluctant, and far slower than expected, to migrate to HP Integrity systems.*

These factors, plus a paucity of Itanium® re-written software for years, and the often costly, complex migrations involved, made many HP BCS users deeply reluctant, and far slower than expected, to migrate to HP Integrity systems. HP's PA-RISC-MPU-powered HP 9000 systems remained popular longer than expected up until their EOS, because of these HP Integrity weaknesses.

The large **HP e3000 PA-RISC population was cut adrift** with no software-compatible HP upgrade path (*except for nightmare cross-MPU/cross-system-architecture/cross-operating-system migrations suggested*). HP AlphaServer **Tru64 UNIX users were similarly abandoned** when HP broke earlier promises to port major Tru64 UNIX capabilities and features into the Itanium® code-fork of HP-UX on the new HP Integrity platform. This forced these users into cross-system-architecture/cross-operating systems conversions of their AlphaServer workloads to either HP-UX or Linux, if they chose HP's Integrity path.

Many **customers instead rejected HP roadmap** recommendations, most flocking to IBM systems, especially to the ultra-competitive IBM Power Systems™ UNIX, but also to System z mainframes and System x servers, depending on workloads. IBM's strong server market share gains in UNIX, with System z10™, and all high-end servers (*discussed above*), show that much of IBM's gain was from HP BCS losses.

Many other BCS customers migrated workloads/applications down to standard x64 servers, often choosing HP's always-competitive, good value, and increasingly-capable, x64-powered ProLiant, and BladeSystem scale-out volume servers, rather than move to the scale-up HP Integrity systems the vendor proposed. This is clearly shown in the strong revenue growth HP's ISS unit has posted, whilst BCS dipped, over the last six years. (*See Figure 2, page 9.*)

## 2. The Itanium® Story – Intel & HP's EPIC Bid for the Enterprise Computing Lead

### Twenty Years of Big Promises, Repeated Delays, and Performance Under-delivery

**HP's Integrity** enterprise servers (*See Section 3*), and HP's currently weak enterprise systems position (*see Section 1*) is best understood from the dramatic story of the **Intel® Itanium® MPUs** powering all HP enterprise systems today. MPU architecture underpins every server family, determining system capabilities, performance, strengths, weaknesses, and thus relative competitive market position. 2009 is the **20<sup>th</sup> anniversary of what later became Intel® Itanium® Architecture**. This saga began in 1989, when HP began researching Explicitly Parallel Instruction Computing (**EPIC**). EPIC sought to execute more than one instruction per clock cycle, using special compilers to determine when each instruction in the stream ahead should execute, in a Very Long Instruction Word (**VLW**)-influenced MPU architecture approach.

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*The partners expressed boundless ambitions for their planned new HP-Intel IA-64 wonder-chip family...*

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From 1994, HP partnered with Intel in a shared grand vision to jointly design, develop, manufacture, and launch, a new full-64-bit MPU architecture based on EPIC, originally named "IA-64". The partners expressed boundless ambitions for their planned new HP-Intel IA-64 wonder-chip family which, the duo promised, would smash the constraints of CISC MPUs (*including Intel's own IA-32 32-bit MPUs*), and would overcome the limitations of the newly-emergent RISC MPUs then powering fast-growing UNIX workstation and server segments. With IA-64's full 64-bit headroom and expansibility, EPIC's claimed Instruction Level Parallelism (**ILP**) performance advantages, and with "Intel-economics" high-volume, low-cost chip manufacturing, IA-64's future seemed star-bright to HP & Intel back in 1994.

With **unbridled marketing hype**, the duo claimed IA-64 MPUs would displace both CISC and RISC MPUs, would soon power most workstations, all levels of servers/mid-range systems, would drive mainframes, and would power top supercomputer systems. This MPU world conquest was to begin in 1998, when the first IA-64 Merced chips were due to ship. With Intel's vast chip-making prowess, muscle, and money, and HP's decades-long chip and system design expertise, **how could these partners' grand vision possibly fail?**

Riding high on Intel's mass success with x86 (**IA-32**) MPUs for the prior decade, then dominant in the PC and ISS segments, the duo were confident that IA-64 MPUs would soon capture all the system segments above. Intel named the new MPU family Itanium® in 1999, and much later the architecture was last renamed "Intel® Itanium® Architecture". But a dog is still a dog, even if you change its name.

Until 2005, HP and Intel jointly developed the first four Itanium® MPU generations, but that year HP completed its final exit from MPU design/development by transferring its Itanium® MPU development team (*who had earlier developed HP PA-RISC MPUs*) based in Fort Collins, Colorado, across to Intel (*who opened a Design Center there for them*).

From 2005 on, Intel developed Itanium® alone, with 1,000+ staff now on the MPU's development. (*Source 9, Paul Ortellini, CEO of Intel, page 76*). The other Itanium® development team, including ex-Dec Alpha RISC MPU developers (*Intel acquired these from Compaq in 2001*), are based at Intel's Massachusetts Microprocessor Design Center (**MMDC**) in Hudson, Massachusetts. Alternate Itanium® generations were engineered by the two teams. The next, Tukwila MC, comes from the Hudson team. Pat Gelsinger, top Intel executive guiding Itanium® developments since 2005, later admitted the prior joint development with HP had been too complex, had caused missteps, and had added to Itanium® delivery delays, pledging big improvements under sole Intel control. Four years on, an eager world still waits. (*Source 10, page 76.*)

## EPIC Voyage for the Good Ship Itanium

What really happened with Itanium® is amongst the most dramatic, roller-coaster technology rides in IT industry history. Itanium® became an IT industry legend for the two promoters' way-overblown promises, for fantastic IDC market forecasts, and for unfilled expectations of rapid market dominance, for repeated years-long MPU generation delays, and for consistent under-delivery of performance/functionality compared to MPU competitors.

Many hundreds of articles, stories, critiques, and jokes, were published about Itanium® over this now-twenty-year saga, many in strong terms, and sparking much passion both for and against. Just four of the more striking assessments are cited below, to give our readers a flavor:

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*Itanium® became an IT industry legend for the two promoters' way-overblown promises, for fantastic IDC market forecasts, and for unfilled expectations...*

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- ***“This continues to be one of the great fiascos of the last 50 years.”*** January 2009 comment on Itanium® history from leading IT industry commentator, John C. Dvorak. (Source 11, page 76.)
- ***“...delays turned the product into a joke in the chip industry.”*** Top New York Times technology writer Ashlee Vance, in a February 2009 article on the last but one of ten years of Itanium® delays. Vance had previously chronicled many earlier twists of the Itanium® saga whilst writing for the respected “The Register” Web site. (Source 12, page 76.) Almost unbelievably and beyond parody, on May 21 2009, Intel announced yet another delay to the next Itanium® chip by a further six months, with OEM deliveries now slated for Q1 2010.
- Soon after Intel named Itanium® in 1999, **industry humorists renamed the chip “Itanic”**, an ironic wordplay comparing it with the supposedly unsinkable White Star Liner Titanic, which promptly sank after hitting an iceberg on its maiden voyage. The tag stuck, and has been widely used ever since.
- ***“The Itanium® approach ... was supposed to be so terrific – until it turned out that the wished-for compilers were basically impossible to write.”*** Famous computer scientist and software guru Donald Knuth, criticizing the extremely demanding compiler requirements for EPIC architecture MPUs. (Source 13, page 76.)

Looking back today in 2009 to the mid-late 1990s when the Intel-HP partnership began, it is amazing how most of the IT industry were swept up into the wave of IA-64 near-hysteria this duo's powerful hype had generated, including:

- **System Vendors Piling Aboard IA-64:** Most IT vendors then (*or later*) pledged to build IA-64 workstations, servers, mainframes, or HPC systems, in varied combinations. In addition to development partner HP, these vendors included Compaq, IBM, Dell, SGI, NEC, Hitachi, Groupe Bull, Unisys, and Fujitsu – but see our assessment in Appendix A: poor souls!
- **Multiple IA-64 Operating Systems Efforts Begun:** HP pledged to port its mainstream HP-UX, Compaq pledged to move Tru64-UNIX, Sun planned to port Solaris, Microsoft planned IA-64 Windows, the IBM/SCO/Sequent Monterey/64 effort was launched, and Project Trillian (*Linux on IA-64*) was begun. The Solaris, Tru64 UNIX, and Monterey IA-64 efforts were all cancelled before reaching market. The Linux efforts succeeded, and HP later added OpenVMS and NonStop OS for IA-64 pledges after its 2002 Compaq acquisition added those platforms to its portfolio.
- **Market Researcher IDC's Fantastic Forecasts:** Long-time “Itanium® booster” IDC produced a now-notorious series of wildly over-optimistic forecasts of Itanium® server revenues, issued yearly from 1997 through 2006. The first, issued in mid-1997, for example, projected a market-sweeping \$38B in Itanium® server sales for 2001, whereas the actual was far below \$100M, even

the latter on far-optimistic Intel data, a quite fantastic forecasting error. Later lower, but still sky-high, IDC Itanium® revenue forecasts became an annual IT industry joke, remaining way too high each year over that period, even damaging that forecaster's credibility.

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*Many of these industry actors suffered repeated later disappointments, many losing large IA-64 investments...*

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Many of these industry actors above swallowed HP/Intel's extraordinary hype, but suffered repeated later disappointments, many losing large IA-64 investments in what followed.

## Cautious ISVs Waited Years Before Adding IA-64 Versions

**One important IT industry community resisted this IA-64 hype**, cautiously waiting to see if these new IA-64 architecture MPUs would take off in the market, as their promoter duo were forecasting. This was the ISV community. Always deeply cautious before committing large effort/costs to port to, and to support their software on, a new MPU platform until market success/failure is clear, most chose a “wait and see” attitude.

After the first IA-64 chip finally shipped in 2001, it emerged that **Itanium® IA-32 hardware compatibility gave poor performance** on the myriad existing IA-32 applications. Almost every software application required major rewriting, re-optimizing, and

*In retrospect, it is deeply surprising that Intel and HP so misjudged how damaging these software incompatibility, poor performance levels, and poor software range availability, issues would prove...*

recompiling, to perform acceptably on Itanium® IA-64/EPIC architecture. This effort/cost was impossible for ISVs to justify whilst Itanium® server sales remained pitifully low over the platform's first 4-5 years. It took massive arm-twisting, and large infusions of Intel and HP money from 2001 to 2007, before the platform boasted an ISV software portfolio remotely comparable with leading UNIX platforms. The size of this software portfolio remains much-disputed, and hard to verify, today. Why would

customers buy servers for which little software was available, and/or where the largest group of existing software (IA-32) ran far slower than on lower-cost x86 native hardware? The answer was that, for many years, they didn't. In retrospect, it is deeply surprising that Intel and HP so misjudged how damaging these software incompatibility, poor performance levels, and poor software range availability, issues would prove to platform uptake. These issues gravely handicapped Itanium® system sales from 2001 through to 2007, when efforts to extend a software portfolio had finally gained traction.

## Six Itanium® Microprocessor Generations to Date Reviewed

The Itanium® MPU generations shipped from 2001 to our end-Q1 2009 writing date, plus three future roadmap generations ahead Intel has disclosed to date, are shown on our Figure 4 summary chart. The third to the sixth of these MPU generations powered all HP Integrity-branded servers shipped to date. (See Section 3.)

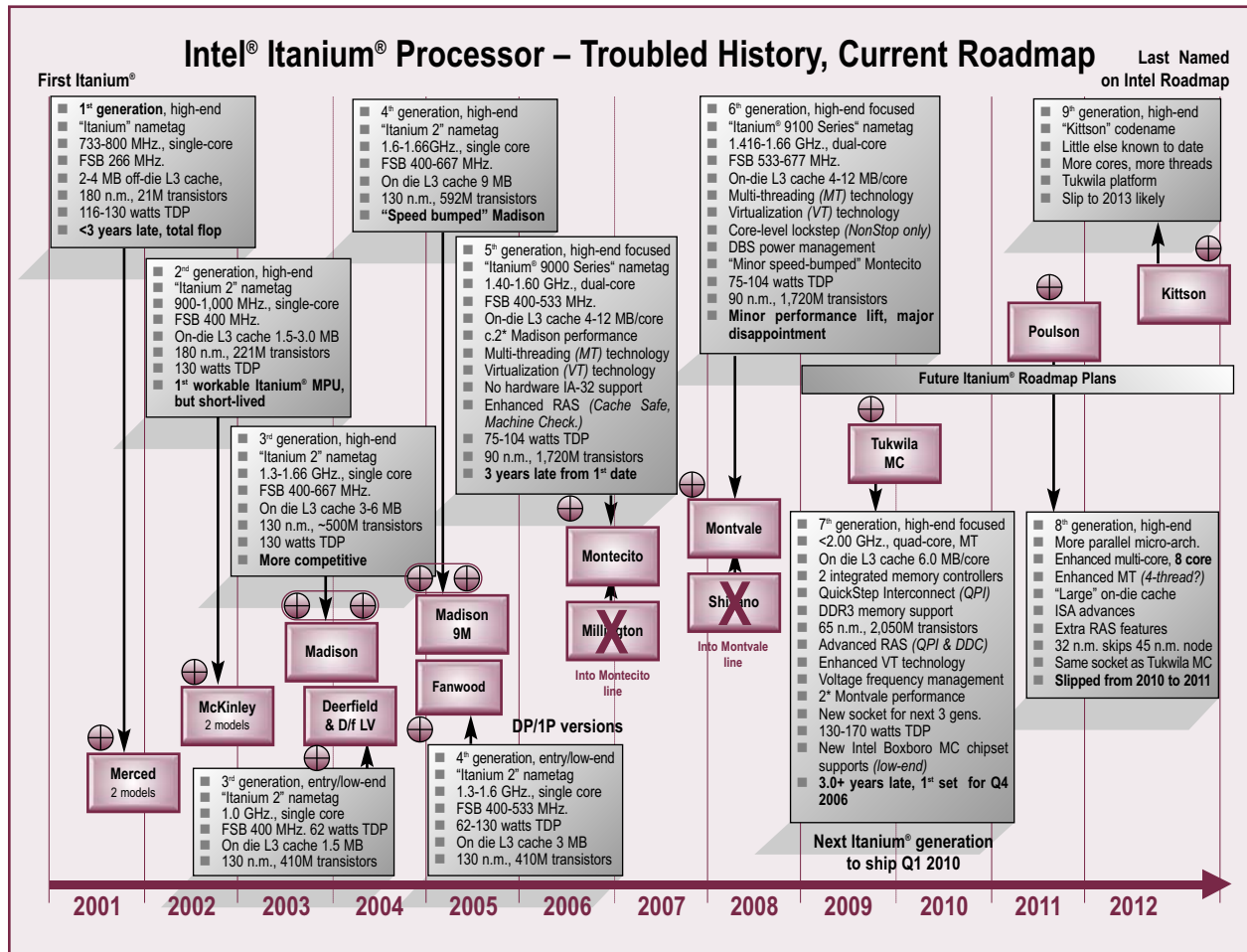


Figure 4: Intel® Itanium® Processors – Troubled History, Current Roadmap

Our chart shows when each generation shipped, the major features/technologies each offered, and our brief comment, to give a quick perspective.

The six Itanium® generations shipped to date were:

- **Merced:** Troubled first generation, 180 n.m. process, Merced single-core Itanium® chips finally arrived over 3 years late, in mid-2001, to near-universal rejection. **Completely uncompetitive** with IBM's storming new POWER4 launched the same year, even with Sun UltraSPARC, and often with Intel's own Xeon® MP MPUs as these scaled-up for enterprise use. Merced IA-32 hardware support gave really poor performance on IA-32 applications and was "buggy"; and little IA-64 optimized software was ready. **Just a few thousand low-end Merced systems were sold and/or given away** by Intel to ISVs, a tiny fraction of early expectations. Mercifully Merced's misery was short-lived, and it was superseded just 13 months later by:
- **McKinley:** The second generation, also 180 n.m. McKinley Itanium® 2 single-core parts debuted in mid-2002, also 3 years later than first-quoted date. Much-improved, these MPUs doubled Merced's performance with faster clock and Front-Side Bus (FSB) frequencies, and by adding <3MB of on-die L3 cache. But McKinley was also short-lived, and system sales using the chip generation remained low. Sales remained crippled by still-low IA-64 software availability, and the still-poor IA-32 software performance. McKinley was itself quickly superseded just 11 months later by:
- **Madison & Madison 9M:** The third generation, 130 n.m. process-based Madison mid- to high-end, single-core Itanium® 2 MPUs first debuted from end-2003 to mid-2004, bringing faster <1.5GHz. clock speeds, and doubling L3 cache to <3-6 MB, but with no FSB frequency increases. These were more competitive. A low-end, low-cost Deerfield part followed in late-2003. **These Itanium® 2 MPUs powered the first generation HP Integrity family from mid-2003.**

Because Intel's next-generation, dual-core Montecito MPU was also so badly delayed (*eventually shipping 3 years later than first planned*), HP created an exclusive MX2 dual-chip module (*Hondo*) using two slowed-down (*to cut heat and power draw*) Madison chips with a large L4 cache that plugged into a single PAC611 Itanium® 2 socket. This HP effort was made to keep up with by-then-already true dual-core MPU competitors IBM, Sun, and Fujitsu. The MX2 provided larger core-count HP Integrity servers, and in-chassis chip/core doubling upgrades, from mid-2004 on.

Fourth Itanium® generation, "speed-bumped" Madison 9M mid to high-end MPU versions shipped from end-2004 to mid-2006, with higher clock speeds of <1.66GHz, and top FSB frequencies lifted to <667MHz. on the top-end parts.

- **Montecito:** The fifth Itanium® generation, some 3 years late, were the 130 n.m. mid-to-high end Itanium® 9000 Series MPUs that first debuted from mid-2006, with top clock frequencies much lower than expected at <1.60GHz. These were the **first dual-core Itanium® chips**, providing <12MB of L3 cache/core, adding coarse multi-threading (*2 threads*), Intel Virtualization Technology (VT) virtualization hardware support, dropping the IA-32 hardware support (*replaced by IA-32 Execution Layer (EL) software emulation*), and with added RAS features. Planned "Foxton" (*power management*) capability was dropped until the next Itanium® generation – Montvale. A substantial step forward, but desperately late to market, Montecito roughly doubled Itanium® MPU performance over the predecessor Madison chips.
- **Montvale:** The current, sixth Itanium® generation shipped from end-2007 to time of writing, but was deemed a major disappointment by reviewers. Essentially a small Montecito "speed-bump" shrink to Intel's 90 n.m. process, with a few extra features, Montvale offered only slight performance gains from a small clock frequency increase from 1.60GHz. to 1.66GHz., and a top FSB frequency increase to 667MHz. Demand Based Switching (DBS) power management (*Foxton*) was added, and core-level lockstep supported (*not used in HP Integrity servers*). The Montvale MPU shares just 10.6GB/s of FSB bandwidth over its two cores and four threads, drastically throttling MPU performance. IBM noted, for example, that its contemporary, top-end POWER6 RISC MPU offered over three times the performance of the highest Montvale MPU, aided by POWER6's over 300GB/s of total chip bandwidth. Unsurprisingly, HP and Intel Montvale marketing was extremely low-key.

Performance of all six Itanium® MPU generations to date was handicapped by their antiquated, severely bottlenecked, low-bandwidth Itanium® Bus/FSB interconnect design. **Other leading, high-end server MPU/system designs used far superior, higher-bandwidth interconnect architectures** for many years now, a major source of their performance advantages. For example, IBM's POWER4 from 2001, and all subsequent POWER MPU generations, used IBM's sophisticated distributed switch architecture (*"Elastic I/O"*) that scales up directly with core clock speeds, and gives far higher bandwidths. AMD's Opteron x64 server MPUs since 2003 have successfully used AMD's HyperTransport Interconnect, a major source of Opteron performance advantage over Intel® Itanium® and x64 Xeon® competitors until recently. Only with the next Tukwila MC generation (*see below*) will Itanium® finally add Intel's new QuickPath Interconnect (QPI) equivalent, and belatedly solve this killer constraint.

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*Performance of all six Itanium® MPU generations to date was handicapped by their antiquated, severely bottlenecked, low-bandwidth Itanium® Bus/FSB interconnect...*

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Intel/HP suffered as Itanium® MPU generations came years later to market than first planned, most with several delays. Clock frequencies sometimes arrived lower than planned, announced new features slipped generations, and generations even slipped process technology nodes, etc. This was hard on all Itanium® system vendors, each change disrupting new system plans/schedules at high cost. HP (and other vendor) servers using Itanium® were usually heavily outperformed by IBM's winning POWER4 to POWER6 RISC MPUs (see below), by some Fujitsu SPARC64 MPU systems, and sometimes even by Sun UltraSPARC MPU systems, in most periods from 2001-2009 to date. Itanium® MPUs were also relatively uncompetitive on price/performance against increasingly powerful x64-MPU server systems now also offering 64-bit headroom. We discuss how superior designs and faster evolution of other leading server MPUs so confounded Intel/HP's Itanium® hopes in a following subsection below.

## Next Three Itanium® Roadmap Generations

On Intel's current Itanium® roadmap, the next generation due to arrive is Tukwila MC, previously due in Q3-2009, but in May 2009 just again delayed by another six months to Q1 2010. Tukwila MC is to be followed by Poulson in (late) 2011, and Kittson around 2013. Most Tukwila MC specifications are now known, but only broad outlines were disclosed for Poulson. Just the codename, and the 22 n.m. node planned, are known for the shadowy Kittson cat.

- **Tukwila MC:** After such prior travails, the next and seventh generation Itanium® MPU is now crucial for Intel® Itanium® Architecture's future and for HP. **Built on Intel's ageing 65 n.m. process**, the monster 2,050M transistor (*largest MPU ever*), 700 m.m.2 die area, Tukwila MC is the first Itanium® quad-core MPU. The fastest part is expected to run at <2.0GHz. clock frequency in a hot 170W Thermal Design Power (TDP) power footprint, but lower-end parts will run from 1.2GHz. within a 130W TDP. With Intel® MT multi-threading, 8 coarse threads per chip/socket are supported. Tukwila MC is the first Itanium® MPU with Intel® QPI links, finally eliminating ancient Front Side (Itanium®) Bus bottlenecks. With QPI, Intel promises peak inter-processor-core link bandwidth of <96GBps, and memory

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...the monster 2,050M transistor (*largest MPU ever*),  
700 m.m.2 die area, Tukwila MC is the first Itanium®  
quad-core MPU.

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bandwidth of <34GBps on Tukwila MC, a long-overdue and major improvement. A 12-port on-die crossbar switch connects the four MPU cores, the two integrated memory controllers, the 4 full-width QPI ports and the 2 half-width QPI ports. Intel stated lower-end Tukwila MC MPU parts will deliver "twice the performance" of top-end Montvale 1.66GHz parts, in an only 25% higher power footprint. What performance increase high-end Tukwila MC parts will deliver has not been disclosed. Given the MPU's higher specifications, these Intel performance claims were disappointing, implying some further unexplained MPU bottleneck, see below.

Originally seen on Intel roadmaps from 2003, Tukwila MC (*first called Tanglewood*) was first expected at end-2006, but slipped several times. Earlier this year, another six-month delay was announced in February 2009, putting Tukwila MC deliveries back to Q3 2009. That delay was to change the dual on-chip memory controllers to support scalable, buffered DDR3 memory, and to support a new Intel socket Tukwila MC shares with the next two Itanium® MPU generations below. (*Reducing Itanium® system vendor development costs for three server generations.*) But then on May 21 2009, Intel announced yet another six month delay, with Tukwila MC (*and platform below*) deliveries to OEMs now set for Q1 2010.

Intel's Q2 2009 public roadmap showed its new **Boxboro Mission Critical (MC) Server Platform**, comprising the **new Itanium® Tukwila MC MPU**, and an associated **new Intel Boxboro MC I/O chipset** supporting it. The Intel Boxboro MC chipset will provide further development cost savings for Itanium® server vendors using it.

The most recent Intel announcement said that late testing of the chip had revealed an opportunity to make "applications scalability enhancements" to the MPU! Original Equipment Manufacturer (OEM) systems built with the chips will therefore probably ship slightly later, within Q2 2010, after these OEMs have re-engineered and re-validated their new servers and chipsets with these yet again revised Intel® Itanium® MPUs.

- **Poulson:** This eighth Itanium® generation MPU will be built on Intel's 32 n.m. process, skipping the 45 n.m. node completely as Intel seeks to finally catch up with competitors' enterprise server MPU performance levels. More parallelism in the micro-architecture is promised, with enhanced multi-core (*we expect 8-core*), and increased multi-threading (*probably 4-threads*), instruction set enhancements, large on-die cache, extra RAS features, plus the Tukwila MC socket/platform compatibility features above, are expected to be supported. Latest indications are that Intel now plans Poulson to ship in late 2011. Whilst we expect Poulson will provide a strong performance advance over Tukwila MC, on that schedule it will arrive too late, a year or more behind its main competitors. It also looks unlikely to best the IBM POWER7, or the next IBM "z11" mainframe MPUs. (*See Section 5 for our analysis on this.*)



- **Kittson:** Almost nothing (*except this codename*) is yet known of this ninth generation Itanium® except Intel plans to built it on the 22 n.m. process node, and we now expect it to debut in 2013. Lack of detail raises suspicions this Itanium® MPU generation may later be cancelled, to enable Intel to finally draw the Itanium® saga to closure before mid-decade.

Intel named and described these three next Itanium® generations to counter the rampant industry rumor/speculation (*widespread in recent years*) that it would cancel Itanium® to stem its large losses on the MPU family at some point. Naturally, both Intel and HP leaders still swear undying public commitment to the MPU architecture. (*Source 9, page 76.*) What else could they possibly say, until that day dawns?

## Itanium® Loses Performance Workstations and HPC/Supercomputer Markets Completely

Critical to Intel's and HP's 1994 IA-64 plans from 1994 were to win dominance in the then-booming **Performance Workstation**, and in the fast-expanding **High-Performance-Computing (HPC)**, market segments.

- **Performance workstation** sales were soaring, and RISC-UNIX MPUs dominated this large segment back then. IA-64's strong EPIC performance, the duo thought, would allow rapid victory and complete segment conquest. The high workstation volumes from this would push up IA-64 chip volumes, and also win more ISV software to IA-64 faster. After Itanium® arrived in 2001, Itanium® performance workstations were launched by all Itanium® system vendors. These proved a complete fiasco, every vendor dropped out of this segment within a year or two, and no Itanium® trace remains in workstations today. See Appendix A for details on this vendor-costly Itanium® market failure.

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*...Itanium® performance workstations proved a complete fiasco...*

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- **HPC** also offered Intel and HP high potential, because the HPC segment was then expanding fast to encompass a much broader customer base, and was migrating away from highly-specialized supercomputer designs and toward more standard (*RISC-UNIX and ISS*) clustered SMP systems able to provide high performance at lower costs. With Itanium® EPIC architecture's high-performance claims, IA-64's top floating point performance, and the platform's full 64-bit headroom, HPC

segment dominance seemed assured for the new MPU. This was important, both for the MPU volumes it would add to IA-64 sales, and for the performance prestige it would bring. After the 2001 Itanium® first ship, the MPU did gain some HPC success, peaking with 16.8% of the systems in the TOP500

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*...Itanium® MPUs have plummeted to a minimal 1.8% share on the latest TOP500 Supercomputers list...*

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Supercomputers list of 11/2004. But today, Itanium® MPUs have plummeted to a minimal 1.8% share on the latest TOP500 Supercomputers list of 11/2008, an almost complete defeat. See Appendix A for our analysis, and supporting data, about this damaging HPC segment share collapse.

These blows drove Itanium® completely out of both vital market segments, the clear causes for which we discuss below.

## What Crushed Sky-high Early Itanium® Hopes?

Behind these market segment failures above were the unexpected resurgence and success of two CISC MPU architectures, and of the dominance attained in the RISC MPU market by one UNIX vendor new leader. These MPUs were:

- **Intel/AMD x86/x64 64-bit extended CISC MPUs:** Far from being replaced by Itanium® as the Intel/HP duo counted on in 1994, x86 morphed into x64 from 2003, and went from strength to strength as the dominant, high-volume processor for ISS servers, performance workstations, and HPC clusters. Today, high-end x64 MPUs also now increasingly outrun Itanium® in high-end enterprise servers too. (*See subsection below.*)
- **IBM System z 64-bit CISC:** Since 2000, IBM's 64-bit z/Architecture System z mainframes enjoyed resurgent growth, doubling their high-end server market share. Five new System z generations, built on sophisticated IBM System z CISC MPUs, industry-leading advanced packaging and systems architecture, powered their success.
- **IBM POWER 64-bit RISC:** From 2001, IBM's POWER RISC MPUs in IBM p Series, System p, and IBM Power Systems™ UNIX servers seized dominant performance, price/performance, and technology leadership in the UNIX market, to gain the market revenue lead from 2005 on.

These successes were not foreseen in Intel and HP's mid-late 1990s IA-64 world view, but happen they did, confounding and crushing the duo's high hopes in most market segments this 2000 decade. We analyze more deeply how these contenders so heavily impacted the Itanium® dream in Appendix A, and below.

## x64 Dominates Server Volumes, Scales up Faster, Undercuts Itanium®

What most wrecked Intel and HP's sky-high early hopes for Itanium® world domination was AMD's 2003 64-bit extended (*AMD64*) architecture Opteron server MPU, followed in late-2004 by Intel® Xeon® server MPUs (*from Nocona on*) using the chip giant's Intel 64 architecture (*EM64T*) copy. Unlike Itanium®, these 64-bit extended x64 MPUs were fully software compatible with x86/IA-32, and so directly ran the huge wealth of x86 software without change. This software all ran with excellent, native performance on x64 hardware systems, without the extensive rewriting Itanium® required, whilst benefiting from extended 64-bit headroom for larger memory. x64 MPUs rapidly swept the ISS market, now the largest server segment. They also quickly dominated in the mid- to high-end PC/workstation market, achieving huge x64 sales for Intel/AMD from these two prime ISS segments. These ultra-high x64 MPU volumes enabled the true "Intel-economics" that Itanium® has long failed to achieve, bringing highly-competitive x64 server MPU prices, along with excellent price/performance. Not only that, x64 MPUs advanced faster than Itanium®, from the first single-core x64s (2003/2004), to dual-core (2006), to quad core (2007), and now in 2009 to the current six-core) Xeon® 7400 MPU (*Dunnington*).

The next high-end x64 step is the deeply impressive, new Nehalem micro-architecture-based, high-end, eight core Xeon® EX (*code-named Nehalem-EX*) MPU, with Intel Hyper-threading support (*dual threads*) that is now due to ship end-2009. Nehalem-EX will thus now arrive a quarter earlier than Tukwila MC, and looks likely to blow away that new Itanium® MPU on price/performance for sure, and probably on performance also. (See Section 5.)

With multiple cores and threads now the x64 norm (*e.g. on the Intel® Xeon® Processor 5500 Series MPUs*), even standard volume x64 ISS servers have scaled-up greatly in power and capacity, and now today (*in Q2 2009*) can offer ISS server capacities of:

- 2 sockets – up to 8 cores, up to 16 threads.
- 4 sockets – up to 16 cores, up to 32 threads.
- 8 sockets – up to 32 cores, up to 64 threads.

These Xeon® MPU-based ISS server capacities now reach up to what, just a few years ago, were classed as mid-range, or even upper-mid-range, server segments long targeted by HP Integrity Itanium® servers.

Above these standard ISS x64 systems, high-end, scale-up x64 Xeon® EX-based SMP enterprise servers (*of up to 32 sockets*) from IBM (*X4 Architecture System x*), Unisys (*ES7000*), and NEC, running Windows or Linux, also provide formidable competition on these OS workloads to the mid- to top-end HP Integrity (*Itanium®*) rx and Superdome systems of similar capacity.

### Itanium® Chipsets Crucial Barrier

To build an Itanium® MPU-based system, a suitable system/server chipset is needed. To design, develop and test a new chipset/generation costs several \$10M+. Deep system architecture and chip design skills are needed. Chipsets heavily determine system features and capabilities. Unlike in x64 and x86 server segments, where numbers of chipset designs have long been offered, no real open Itanium® chipsets market developed. Early, low-end Intel® Itanium® chipsets fell obsolete and went un-replaced. This meant each Itanium® system vendor had to invest deeply in their own chipset to be able to build Itanium® systems. HP, alone amongst Itanium® system vendors, invested fully in both low-end and high-end system chipsets, over two generations, shared by its HP Integrity (*Itanium®*) and HP 9000 (*PA-RISC*) server families (see Section 3).

Chipsets have therefore been another barrier, and a large development expense, impeding Itanium® adoption. Intel seeks to address this by introducing its new Boxboro MC I/O chipset for the next Itanium® Tukwila MC, now slipped again to Q1 2010. See Appendix A for further chipset analysis.

### Itanium® Solutions Alliance (ISA)

To rally allies to the tattered Itanium® banner, Intel established the ISA in January 2006, as a cheerleading and propaganda front organization that was to proselytize the disbelieving multitudes as yet unconverted to the Itanium® faith, its sponsors **pledging a collective \$10B in Itanium®-related spend by 2010** to the cause. (*Source 14, page 76.*) It is hard to see where (*or indeed if*) such a massive sum has actually been spent, other than on all normal Itanium®-related costs members were already committed too, or to adjudge whether the results merited this sum. Active in its early years, less has been heard from the ISA of late, reflecting diminishing hopes for the platform from these Club Itanium members. A notably slow-performing Web site is an ironic ISA feature – Itanium® in action we presume!

### Software Incompatibility the Itanium® “Achilles Heel”

Perhaps the gravest error Intel and HP made with Itanium® was failure to design/build-in 100% software compatibility for the huge wealth of IA-32 software with native x86/x64 performance. This meant all IA-32 software could never run on Itanium® MPU systems with acceptable, native-level performance comparable to that of x64 hardware of the same period. This was true both with the Itanium® original IA-32 hardware support (*up to 2005*), but also with the IA-32 EL software emulation layer support provided since Montecito, and remains the case today. So it clearly makes far more sense for enterprises to run their x64 software workloads at native speed on more economical x64 native hardware, not on more costly, lower-performing Itanium®, which is what the market has done en masse throughout.

This meant every software solution ported to Itanium® needed to be heavily rewritten, re-optimized, and recompiled, to run well on Itanium®-MPU-based systems. With far lower Itanium® systems sales than early predictions promised, ISVs were slow to see sufficient market size, many waiting years before creating Itanium® versions of their software. This is why it took HP and Intel over six years (2001-2006) from the Itanium® first ship until a reasonable critical mass of Itanium® software solutions had been built.

Even normally strong HP and Intel supporter Microsoft is brutally frank about these Itanium® system characteristics in the current customer guidance regarding Itanium®-based systems that it offers on its Web site, which reads:

*“Itanium® processors utilize Intel’s EPIC architecture. Unlike x64 MPUs, Itanium® processors are not backwards compatible with traditional 32-bit x86 software. Itanium® processors do allow certain 32-bit x86 software to run in emulation, but the performance of the software will be reduced. (Lack of) Backward compatibility is a key point differentiating Itanium® from x86 and x64 architectures.” (Source 15, page 76.)*

Wow, that’s pretty clear then. With friends like this, do HP and Intel need enemies?

## Itanium® – Our Analysis

The Itanium® saga inflicted market share loss, and reputation damage, to HP’s enterprise systems business, and dented Intel’s microprocessor credibility, for years. The twisting path, narrowing niche targets, and delay-plagued deliveries of this MPU story were embarrassing to these two powerful technology majors. Itanium® fell far short of the duo’s stratospheric 1994 ambitions of world domination. Executives at both firms have ruefully (*if quietly*) admitted as much several times. (*Example: Pat Gelsinger, VP Intel DEG, source 10, page 76.*) But both remain deeply locked in mutual interdependence around Itanium®, at least for the next several years. Our conclusions on the Itanium® MPU line today are:

- **An HP Proprietary MPU:** For all practical purposes, with 95% of all 2008 Itanium® servers sold by HP, Itanium® is now an HP-proprietary MPU, custom-made near-exclusively for HP by Intel. Most Itanium® servers sold replaced HP’s legacy RISC MPU/server platforms (*see Section 1*); a process HP will complete in year or two. HP Itanium® server sales recently fell YOY, and will likely to dip further as this replacement process ends.
- **Very Low-volume MPU:** Itanium® is a low-volume MPU. Other analysts put Itanium® MPU units shipped at c. 200,000 for 2007. We estimate <275,000 units were shipped in 2008, with c. 825,000 units total shipped from 2001-2008 over all Itanium® generations. “Shipped” were also surely rather higher than “sold” units. These volumes are magnitudes below the 10Ms of Intel/AMD x64 MPUs that power the <8M ISS servers sold yearly, plus the 10Ms more used in PCs/workstations. By contrast, IBM sells many 10Ms of Power Architecture™ MPUs to power all three games consoles, and many more 10Ms for embedded systems, supporting its low-volume, high-price IBM POWER6 and z10 mainframe MPU manufacturing.
- **Itanium® Market Niches Lost or Shrinking:** Itanium® lost crucial market segments originally targeted. Performance workstations (*completely lost to x64*), HPC (*nearly all lost to x64/Power*), high-volume, industry-standard servers (*lost to x64*), were near-total market failures. HP also lost substantial share in RISC-UNIX, and in all high-end enterprise servers (*to IBM POWER RISC and System z10™ mainframes*). Mid- to high-end RISC-UNIX and mainframe replacement are now the only remaining target niches for Itanium®, with IBM the dominant competitor in both areas. So HP must now defeat IBM in these segments for Itanium® to thrive. This looks most unlikely, and further erosion of HP enterprise systems share more probable, from our analysis here.
- **Abandoned by Leading System Builders:** Experienced system vendors IBM, Dell, and now Unisys, each abandoned Itanium®, writing-off serious investments and determined sales efforts, decisions none made lightly. Their moves showed terminal disillusion on future Itanium® prospects by three important system vendors, two Tier 1s. The handful of other system vendors still offering Itanium® systems sell tiny server numbers, most with more server business on their other MPU platforms. With the latest, May 2009 announced, further six-month delay on Tukwila MC, further vendor departures are now likely.
- **Far From an Industry Standard:** Intel and HP long portrayed Itanium® as an “industry-standard MPU”. These claims are ludicrous. A near-HP-proprietary, very low-volume MPU, sold at relatively high prices, used by a dwindling few other second- or third-tier server vendors together selling just 5% of Itanium® systems sold in 2008, can in no way claim to be an industry-standard MPU. By using this phrase about Itanium®, Intel & HP debases this useful term.
- **Lateness to Market & Underperformance Record:** Itanium® MPU generations to date were all consistent – consistently years later to market than planned, and consistently lagging main competitors in performance, price/performance, performance/core, and performance/watt, crucial enterprise server metrics. Itanium® system vendors and users can thus easily predict their future, unless such a consistent record miraculously changes!

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*Intel and HP long portrayed Itanium® as an “industry-standard MPU”. These claims are ludicrous.*

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- **Heavy Itanium® Financial Losses for Intel:** We estimate Intel spent \$5B+ on its 15-year Itanium® design, development, fabrication, marketing, software ecosystem, and system vendor support efforts to date. Significant revenue returns only flowed from c. 2005 on. For 2008, we estimate Intel took in ~\$450M net Itanium® MPU revenue, certainly its best year to date. We assess Intel's Itanium® revenues for its 2001-2008 MPU shipping lifespan at ~\$1.35B. Intel's cumulative Itanium® losses (1994 to 2008) thus total ~\$3.65B (*our estimate*), a large sum even for the chip giant, and one unlikely to be fully recouped. With 1,000+ Intel staff working on Itanium® design, development, test, etc. (*Source 9, page 76*), plus Intel's heavy Itanium® marketing spend, and with chip manufacture costs, yearly costs remain high, but reportedly brought Intel current-year Itanium® revenue profitability in 2008.
- **Figures Hidden-truth Hurts:** Intel discloses no Itanium® MPU sales or cost data, no MPU units, MPU \$M revenues, nor \$M costs incurred, although similar data on its more successful Intel product lines is sometimes shared. Obviously, by Intel's lofty standards, Itanium® MPU unit sales and revenues remained embarrassingly low, and cumulative costs high, until the last year or two. To have provided data revealing that real picture would have given Itanium® critics a field day, indicated large Intel losses to date, and could have raised Intel shareholder ire, perhaps even sparking Board challenges! So hiding the truth won the day.
- **Itanium® Future Bleak – Outclassed Again:** Our assessment (*Section 5*) is that directly competing next generation IBM (*POWER7 and System z11*), Sun (*UltraSPARC-RK*), and next Intel Xeon® (*Nehalem-EX*) high-end server MPUs will each hugely trump the performance of Intel's so long-awaited, next-generation Itanium® Tukwila MC, which has just slipped back another six months to Q1 2010. The currently shipping generation of enhanced POWER6+, and System z10™ mainframe, MPUs seem likely to still match (*or outperform*) this next Itanium®. We discuss why this is the case in Sections 5 and 6. On our assessment, this will doom HP to further server market share losses through to 2012, without a major course change on HP's part.
- **IBM Exec Calls Itanium® End by Early 2013:** In a January 2008 interview, IBM STG VP Scott Handy said: *"The end of life for Itanium® will occur in the next five years. HP will have to announce some kind of transition."* citing the unsustainable basic economics of the MPU that internal IBM analyses had found. (*Source 16, page 76.*) Handy's prediction thus calls early 2013 as the latest date by which Itanium® abandonment will be declared. That timing is consistent with Intel's Itanium® roadmap pledges that covered three more generations, the last-named Kittson slated for the year before. But of course IBM would say that! However, we consider this became a more likely outcome after the latest, additional six-month delay. If the Poulson generation fails to finally attain fully-competitive performance relative to its main MPUs competitors, or is once again too long-delayed, that end is certain.
- **Itanium® Platform Investments High Customer Risk:** Based on the factors above, enterprises making further Itanium®-based HP Integrity investments are clearly taking high strategic risks of running on an uncompetitive, HP proprietary MPU architecture enterprise platform that is likely to reach the end of its evolutionary life in just a few more years.

Not a pretty MPU picture. We examine the HP Integrity server family built around these Itanium® MPUs in Section 3 following.

## 3. The HP Integrity Server Family In Review

### HP Integrity Family Introduction

The mainstream server family HP long pitched against IBM's Power™ System UNIX servers, but has now also thrown up against Big Blue's thriving System z10™ mainframes, **was announced as HP Integrity in June 2003**. This new server brand replaced the "HP 9000 Itanium®" tag used on HP's first 2001 (*Merced 1<sup>st</sup> Itanium® generation MPU-powered*) and 2002 (*Itanium® 2 McKinley 2<sup>nd</sup> Itanium® generation MPU-powered*) low-end servers, few of which were sold. (*Many were given away to ISVs, business partners, and universities, etc., to promote Itanium and to gain software support – the former also for use as boat anchors, and to provide space heating, etc.*)

### HP Integrity – Near-Indistinguishable from HP 9000 Server Equivalents

HP Integrity servers (*from-2003 on*) were near-indistinguishable (*model-for-model*) with their HP 9000 PA-RISC-powered equivalents, except for obvious MPU and software stack differences. Forerunner high-end systems first shipped as the HP 9000

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*HP Integrity servers (from-2003 on) were near-indistinguishable HP 9000 PA-RISC-powered equivalents...*

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Superdome, using PA-RISC MPUs only, in 2000 (*based upon HP and Convex technologies that HP had acquired in 1995*) and using HP's Yosemite chipset. To simplify its enterprise server line-up, to ease the PA-RISC to Itanium® MPU move, and to cut development costs, HP engineered common server hardware to support both PA-RISC MPU-based (*HP 9000 rp and HP 9000 Superdome*) and Intel Itanium® MPU-based (*HP*

*Integrity rx and Superdome*) systems. Both lines used the same low-end HP zx1 and high-end HP sx1000 chipsets initially, each line using different main-boards and cell-boards. The zx2 and sx2000 second-generation HP chipsets also supported both server lines. HP 9000 systems ran only under HP-UX UNIX, which HP had also ported and rewritten to Intel® Itanium® Architecture to also run on HP Integrity systems.

HP 9000 PA-RISC systems were offered in parallel with new HP Integrity systems through two more PA-RISC MPU generations over five more years. The first used last-but-one HP PA-8800 RISC dual-core MPUs, and the last used higher-frequency, final PA-8900 RISC dual-core MPUs from 2005 until the December 2008 HP 9000 EOS.

HP Integrity design, construction, broad capabilities, strengths, and weaknesses were thus familiar to HP 9000 customers, ISVs, and partners.

This common hardware approach allowed HP to reduce its enterprise systems R&D levels, slim operating software teams, and cut BCS costs this decade, as it phased out four legacy platforms in favor of the new Itanium®-based systems. The legacy HP e3000, HP AlphaServer, HP 9000 PA-RISC, and HP NonStop MIPS RISC, platforms have now all passed their EOS dates. Replacements were to be mainstream HP Integrity and the specialized, fault-tolerant HP Integrity NonStop, systems, but many unhappy HP BCS customers jumped ship to IBM and other system vendors. HP also saved operating system costs by not porting two of its operating systems to HP Integrity. These were HP MPE/IX (*HP e3000, v7.5 last release*) and HP (*Compaq/Digital*) Tru64 UNIX, the main features of which it had promised to port into HP-UX, a promise later broken. **No software-compatible migrations were offered to either large group of HP users.**

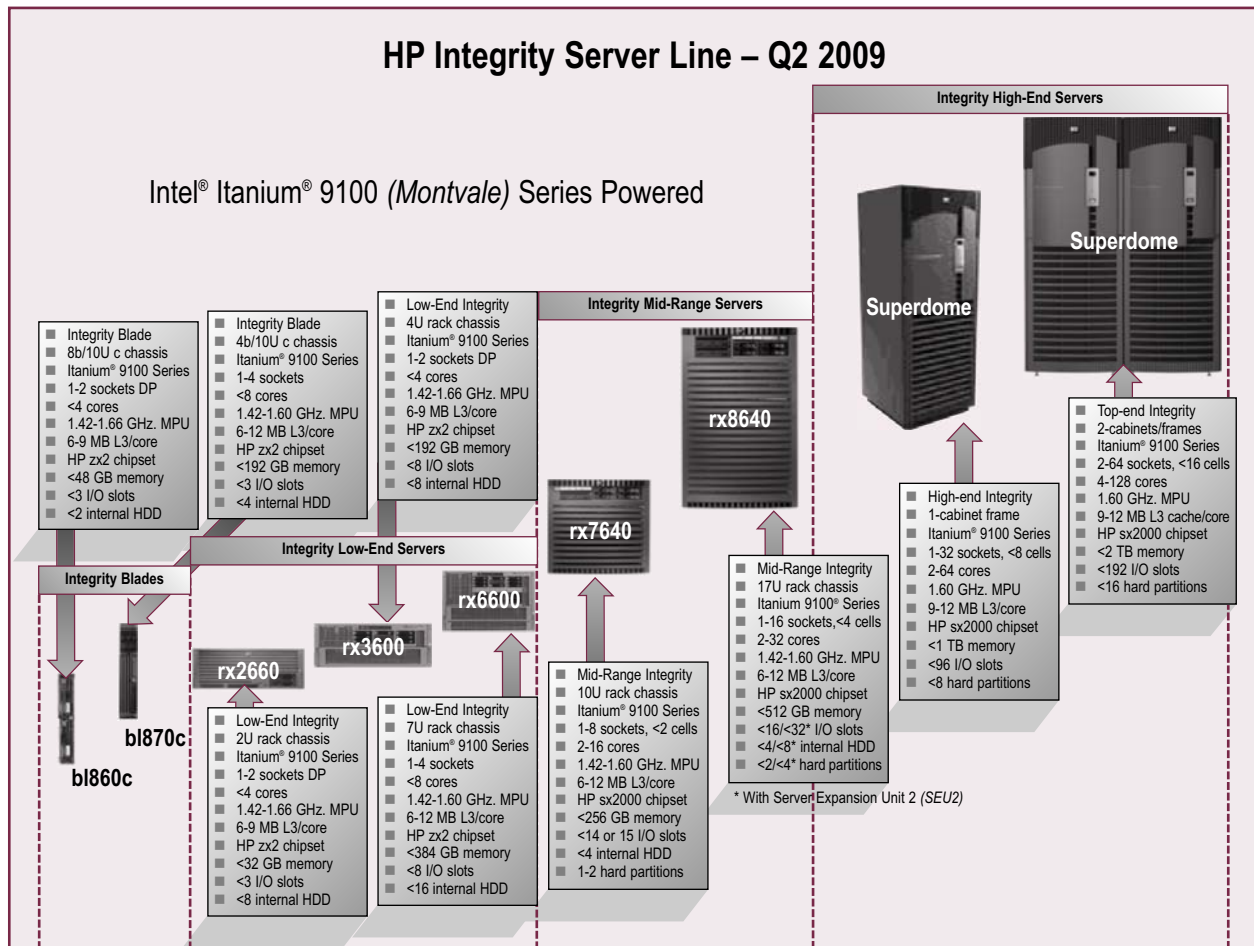
## HP Today Dominant Itanium® System Vendor – Other Majors Abandoned

HP today completely dominates Itanium® MPU powered system sales. **Gartner reported that HP Itanium®-based systems accounted for 95% of Itanium® server sales in 2008**, with NEC at 3%, and Fujitsu, SGI, and Hitachi each selling under 1% of total server units each. (*Source 12, page 76.*) Amongst other Tier 1 server vendors, Sun never committed to using Itanium®, whilst IBM and Dell (*who both did*) each abandoned the MPU in 2005, after each building first servers and workstations. Unisys followed suite in 2009, having tried for years to promote Itanium®. Abandonment by these three major, experienced system vendors, after each made significant investments in, and strong efforts to sell, Itanium®-based systems, now leave HP the only Tier 1 vendor still supporting Itanium® today. The handful of other system vendors still offering Itanium®-powered servers all do so non-exclusively, heavily hedging Itanium® bets with other MPU/system platforms. This is especially so for the largest, most important of these, Fujitsu. See Appendix A for our assessment of these other Itanium® system vendors.

## HP Integrity Server Family End-Q1 2009

The current HP Integrity server line-up at time of writing (*early Q2 2009*) is shown in our Figure 5 chart (*on page 22*), which gives the main specifications of each model. All these current HP Integrity systems are powered by Intel Itanium® 9100 Series (*Montvale*) generation MPUs, assessed fully in Section 2.

- **High-end HP Integrity Servers:** Heading the family are top-end **HP Integrity Superdome systems**, HP's long-running (*since 2000*) high-end UNIX server design. Superdome systems are cache-coherent (*c.c.*) Non-Uniform Memory Architecture (*NUMA*)-architecture, large-shared memory systems, built up from multiple (<4, <8, or <16) four-MPU-socket HP cell-boards, and currently use HP's high-end sx2000 server chipset. Superdome systems currently provide <16, <32, or <64 sockets, and <32, <64, or <128 cores, in the single cabinet/frame high-end, and the twin cabinet top-end versions respectively, using Itanium® 9100 Series (*dual-core*) MPUs running at 1.6GHz and sporting 9 or 12MB of on-die L3 cache/core. These HP Superdome systems can be hard-partitioned along their cell-board physical boundaries into <4, <8, and <16 HP nPar hard partitions respectively. HP Superdome systems compete with high-end IBM Power Systems™ 570 and 595 POWER6/6+ RISC-UNIX systems, with IBM System z10™ Enterprise Class high-end mainframes, with Sun and Fujitsu SPARC64 VII Enterprise 8000 and 9000 systems, as well as with HP's own Integrity NonStop, and with x64 scale-up enterprise servers from IBM, NEC, & Unisys.
- **Mid-range HP Integrity Servers:** The mid-range HP Integrity line-up comprises the rx7640 and the rx8640 rack-mounted servers (*10U and 17U formats*), which offer <8 and <16 sockets, supporting <16 or <32 cores respectively. These systems also use a similar *c.c.* NUMA design, 4-socket cell-board construction, and HP sx2000 server chipsets, as the Superdome systems above. These servers can also be hard-partitioned along their cell-board boundaries, with <2 and <4 HP nPar hard-partitions respectively. They use "performance/value" Itanium® 9100 Series MPUs running at 1.42-1.60GHz., with 6 or 12MB of on-die L3 cache/core. These servers compete against IBM's Power™ System 560 POWER6+-based mid-range systems, against IBM System z10™ Business Class mainframes, and against Sun/Fujitsu SPARC64 VII Enterprise 5000 and 8000 mid-range systems, as well as against large, scale-up Xeon® EX-powered SMP-like multiprocessor enterprise servers from IBM, Unisys, and NEC, with Fujitsu likely to join them.
- **Low-end HP Integrity Servers:** HP Integrity low-end, mostly rack-mount, servers are the rx2660, rx3600, and rx6600, models (*in 2U, 4U, and 7U formats*), with <2 sockets/<4 cores DP, <2 socket/<4 cores MP, and <4 sockets/<8 cores MP capacities respectively. These low-end servers use the HP zx2 server chipset, and HP main-board construction. These systems compete directly with volume RISC-UNIX servers, notably IBM Power Systems™ 520, and with Sun Microsystems volume UltraSPARC (*T1, T2, and T2 Plus*) servers. They also go head-to-head with Intel/AMD x64-MPU-powered volume servers of similar sizes, notably ISS server leader HP's own highly-competitive ProLiant x64 server systems, but also against IBM System x, and Dell PowerEdge, standard servers.



**Figure 5: Current HP Integrity Server Line – Q2 2009**

- **HP Integrity Blade Servers:** HP also now offers two Itanium®-MPU-powered blade servers. First was the bl860c, a <2 socket, <4 core, single-wide server blade, 8 of which can fit in a 10U HP BladeSystem “c”-class chassis. The second was the bl870c, a double-wide, <4 socket/<8 cores server blade, of which 4 can fit in a 10U HP BladeSystem “c”-class chassis. HP BladeSystem x64 blades, and IBM BladeCenter x64 and POWER blades, are their direct competition.

Lower-end HP Integrity servers and blades mostly provide Intel® Itanium® Architecture software-compatible, scale-out server options for development, testing, and small deployments, mostly under the HP-UX and OpenVMS OS. Most enterprise users today now deploy most of their low-end to mid-sized scale-out Microsoft Windows and Linux applications onto x64 servers or blades, which offer better choice, more software, and lower costs with better price/performance. HP’s 2009 positioning for the HP Integrity server family, and Intel’s pitch for Itanium®-based systems today, both emphasize mid-range to top-end roles strongly for that reason. So HP’s apparently wide, “one-family-fits-all-enterprise-needs” HP Integrity positioning actually now focuses on the mid-range to high-end segments only. A simplified HP Integrity entry-low-end and blades range is thus quite likely in HP’s next-generation server line-up, now delayed again until ~Q2 2010.

### HP Integrity Server Family Generations to Date

The HP Integrity server family was developed/delivered through three and a half generations between its mid-2003 launch and our early Q2 2009 time of writing, three driven by main Intel® Itanium® MPU generations to date, plus a “half generation” based on an HP Dual-Chip Module (DCM) packaging step:

- **1<sup>st</sup> HP Integrity server generation:** From June 2003, based on Intel® Itanium® 2 (Madison and later Madison 9M) MPUs, using the HP zx1 and sx1000 chipsets for low-end, and mid-high-end servers, respectively.
- **1.5<sup>th</sup> HP Integrity server generation:** From May 2004, based on the HP MX2 dual-chip module (Hondo) using Intel Itanium® 2 (Madison) MPUs, doubling chip/core count, but running the MPUs at cranked-down frequencies, using the same chipsets as above. Provided a needed HP Integrity per-socket performance boost, and cores capacity upgrade, during the long wait for Intel’s much-delayed Montecito Itanium® generation.

- **2<sup>nd</sup> HP Integrity server generation:** From July 2006, based on the Intel Itanium® 9000 Series (*Montecito*) dual-core MPUs, using second-generation HP zx2 and sx2000 chipsets for low-end, and mid-high-end, servers respectively.
- **3<sup>rd</sup> HP Integrity server generation:** From November 2007, based on Intel Itanium® 9100 Series (*Montvale*) using the same HP zx2 and sx2000 chipsets as above, for low-end, and mid-high-end, servers respectively

The fourth and next generation HP Integrity line awaits Intel volume production of the Itanium® Tukwila MC MPU generation, centerpiece of Intel's new Boxboro MC Server Platform. In February 2009, these new Intel Itanium® MPU and chipset parts were delayed by six months, with delivery then put back to Q3-2009. Most recently, in their May 21, 2009 announcement, Intel revealed a further six-month delay, putting OEM volume shipments back to Q1 2010. This now pushes the next HP Integrity server generation out to around Q2 2010, after HP's needed further system re-design and re-validation process has been completed. Tukwila MC uses a new Itanium® MPU socket and the Intel® QPI interconnect, and so needed a new server chipset generation (*see below*).

## Mixed PA-RISC and Itanium® MPU Servers, In-Chassis Upgrades

Cell-board-based HP Integrity Superdome systems could mix certain combinations of PA-RISC MPU-based cells and/or Itanium® 2-based cells in the high-end HP Integrity system chassis. (*All MPUs in each cell had to be of the same type/speed.*) This was helpful for HP 9000 Superdome customers, allowing them to incrementally transition capacity to Itanium® 2 cells alongside their PA-RISC cells, on one hard-partitioned HP server, and/or to run different operating systems on the one HP box for the first time.

Within limitations, customers could also upgrade HP 9000 and HP Integrity Superdome servers within the chassis, by swapping mainboards or cell-boards for replacements sporting newer MPUs, carrying some chassis infrastructure investments over several MPU generations, for partial, but still useful, cross-generation platform hardware investment protection.

## HP Integrity Server Chipsets

Functionality, specifications, capabilities, and technologies supported by HP Integrity servers were much dictated by the Itanium® MPU generations/models used (*assessed in Section 2*), but the other main server capability determinant was the architecture, capacities, and features of the server chipsets used. In recent years, Intel provided no up-to-date or high-end Itanium® chipsets, leaving system vendor OEMs to design/build their own to power their Itanium®-based systems.

Itanium® was always planned as a standard “merchant MPU”, intended to support a wide range of OEM system builders, and a wide diversity of systems, albeit now much-narrowed. Therefore, Intel always had to provide a simple, relatively easy-to-interface, standard Itanium® MPU design, using a relatively low number of signal Input/Outputs (*I/Os*) and pins and a standard socket. This was needed as the “lowest common denominator” MPU building-block that all OEMs (*of differing skills levels*) would be able to integrate into their designs. This precludes sophisticated MPU module packaging, and tight MPU-chipset-system architecture optimizations, that integrated MPU-system vendor IBM so extensively exploited in both its market leadership IBM Power Systems™ RISC-UNIX systems and System z10™ mainframe high-end enterprise systems.

Server chipsets thus provided Itanium® server vendors with their best opportunity to add value, by applying their system architecture know-how to improve server performance, and to add RAS features, beyond those that standard Itanium® MPUs provided. Designing/developing enterprise server chipsets is a challenging system/chip design/development/validate/fabricate process, each design/generation costing an OEM several \$10Ms to develop, prove, and to manufacture in the relatively small volumes needed.

For its HP Integrity family, HP has (*to date*) engineered two generations of low-end (*zx1 and zx2*) and two generations of mid-high-end scalable (*sx1000 and sx2000*) server chipsets. These chipsets powered all models of HP Integrity servers (*and workstations*), supporting all Intel® Itanium® and PA-RISC MPUs used, from 2003 to our Q2 2009 time of writing. Figure 6 on page 24 shows the capacities and characteristics of these four HP chipsets, the newer two enabling the HP Integrity server specifications we showed in Figure 5 on page 22.

The next Tukwila MC MPU generation will use a new Itanium® socket shared with the two next Itanium® MPU generations. New-generation chipsets to support Tukwila MC's new QuickPath Interconnect, this new socket, and other MPU and system features are thus needed. With the Tukwila MC MPU, substantial memory controller functions, previously performed in the chipset, have been moved onto the new MPU's die-resident dual memory controllers, simplifying chipset functionality and making I/O control and RAS functionality now the most central new chipset functions.

Intel's new Mission Critical Server Platform family was named the “Boxboro MC Server Platform”. For this, Intel is providing a new (*I/O*) chipset (*Boxboro MC*) to support Tukwila MC, now to ship on a six-month's further delayed, Q1 2010 delivery timescale. Specifications and capabilities of Boxboro MC have not been disclosed.

**We expect that HP has developed a third-generation, high-end HP chipset** superseding or updating the sx2000, to preserve and carry forward current, unique mid- to-high-end HP Integrity added value-features, and supporting the new Tukwila MC system's QPI interconnect, new socket, etc. No details have yet been disclosed.

HP Integrity Server Chipsets to Date				
HP Server Chipsets:	zx1	zx2	sx1000	sx2000
HP Code Name:	'Pluto'	'Titan'	'Pinnacle'	'Arches'
Role:	Entry-Low End	Entry-Low End	Mid-Range to High-End	Mid-Range to High-End
	Mainboard servers	Mainboard servers	Cellular enterprise servers	Cellular enterprise servers
Year debuted:	<b>Q1 2002</b>	<b>Q2 2006</b>	<b>Q1 2003</b>	<b>Q2 2006</b>
Itanium Generations:	McKinley	Montecito	McKinley	Montecito
	Madison	Montvale	Madison	Montvale
	Madison 9M		Madison 9M	
HP PA-RISC MPUs:	HP PA-8800 RISC	HP PA-8900 RISC	HP PA-8800 RISC	HP PA-8900 RISC
No. Of MPU Sockets:	<4	<4	<b>2-128</b>	<b>1-64</b>
No. Of Cores:	<4	<8	<b>2-128 (on MX2 only)</b>	<b>2-128</b>
No. Of Threads	<4	<16	<b>&lt;128 (on MX2)</b>	<b>&lt;256</b>
FSB Frequencies:	400-533 MHz.	400-667 MHz.	400-667 MHz.	400-667 MHz.
Maximum Memory:	<b>128 GB</b>	<b>192 GB</b>	<b>1 TB</b>	<b>2 TB</b>
Max. I/O Slots:	<8	<8	<192	<192
Front Side Bus Bandwidth:	<b>6.4-8.5 GBps</b> 2/4 socket	<b>8.5 GBps</b>	NA	NA
Crossbar Throughput/cell	NA	NA	<b>8.0 GBps</b>	<b>&lt;34.6 GBps</b>
Peak Memory Bandwidth:	<b>12.6 GBps</b>	<b>17.0 GBps</b>	<b>&lt;256 GBps</b>	<b>&lt;553 GBps</b>
Aggregate I/O Bandwidth:	<b>4 GBps</b>	<b>8 GBps</b>	<b>2.5 GBps</b> Cell to I/O subsystem	<b>11.4 GBps</b> Cell to I/O subsystem
Memory Type:	DDR1 2 200/266 MHz.	DDR2 400/533 MHz.	DDR1 2 200/266 MHz.	DDR2 400/533 MHz.
I/O Types:	PCI, PCI-X, ADP 8x	PCI-X, PCI-X 266, PCI-Expr	PCI, PCI-X, ADP 8x	PCI-X, PCI-X 266 PCI-Expr
Note: HP's high-end Yosemite chipset supported only PA-RISC 8600 in first-generation HP 9000 Superdome servers from late 2000.				

Figure 6: HP Integrity Server Chipsets to Date

However, we expect HP will use Intel's Boxboro MC I/O chipset (<8 socket) on next-generation, low-end and blade-format HP Integrity servers. Chipset performance should be good, Intel prices moderate, and doing so will save HP \$10M+ costs it would otherwise have incurred to develop a new low-end HP chipset generation to replace its zx2.

## HP Integrity Operating Systems Support

HP Integrity servers offer four operating system families, the supported version(s) of which are:

- HP-UX 11i v3:** The flagship HP-UX 11i v3 operating system for HP Integrity systems is now offered in four bundled Operating Environment (OE) packages. These are the **Data Center (DC-OE – most comprehensive, with all the following)**, **High Availability (HA-OE – adds HP Serviceguard clustering for HA, PA/PM software, etc., to Base OE)**, **Virtualization Server (VS-OE – Base OE plus)**, and **Base (BOE – Base HP-UX 11i, file system, partitioning, etc.)** First released in 2007, HP-UX 11i v3 supports all HP Integrity and HP 9000 PA-RISC servers. (On different code-bases, with all new developments on the Itanium® MPU fork.) The large majority of deployed HP Integrity servers (and partitions) run HP-UX, which provides HP's robust, comprehensive, general-purpose enterprise UNIX OE. HP-UX 11i v3 offered improved performance, increased availability, better package value, and simplified system management. Earlier releases were long-familiar to HP 9000 users. HP-UX's pace of development this decade is generally rated slow, considered as lagging behind faster and stronger advances of z/OS®, AIX, and Solaris, no doubt due to the large efforts needed by HP's Itanium® porting challenge, and subsequent HP-UX development staff cuts. It was recently announced that the minor release HP-UX 11i v3, Update 4, shipped in April 2009. The next major release, HP-UX 11i v4, is roadmap-slated for 2010.
- Linux: Red Hat Enterprise Linux 5 & Novell SUSE Linux Enterprise Server 10** distributions. These two enterprise distributions of the open-source Linux OS are the other mainstream HP Integrity (Itanium®) operating system options, providing access to a decent range of Linux Itanium® Architecture software applications, and to Linux open source economic benefits, on HP's main enterprise server platform. However, most enterprises today deploy Linux on x64 hardware by preference, because it provides equivalent or better performance at lower cost, and is now available in both scale-out cluster and scale-up enterprise server forms, each best for different workloads. Application performance of Linux on HP Integrity is said to often run below that of HP-UX, the latter more optimized to the hardware.



- **HP OpenVMS v8.3-1H:** In a choice of **Mission Critical (MC)**, **Enterprise**, and **Foundation OE** bundles. This DEC VAX/HP AlphaServer-heritage, cluster-strong operating system offers good availability, performance, security, and broad systems management capabilities, in the three levels of bundle strength above. OpenVMS v8.3-1H for HP Integrity is the current version, and v8.4 is expected late in 2009. Today's OpenVMS on HP Integrity hardware carries forward this software architecture, which has a 32-year track record that began with Digital's VMS 1.0 in 1977. Most OpenVMS support/development has recently been off-shored from Massachusetts, USA, to India.
- **Microsoft Windows: Windows Server 2003 for Itanium®-based Systems**, in **Enterprise** (up to 8-way) and **Datacenter** (up to 64-way) Editions, and **Windows Server 2008 for Itanium®-based Systems**. Microsoft developed the two full-function Windows Server 2003 for Itanium®-based Systems Editions above, but found limited uptake compared to mass usage of its Windows Server 2003 and 2008 x64 and x86 versions. It also found this limited usage restricted to just three specialized enterprise roles/workloads. The Redmond software giant therefore cut-down the current Windows Server 2008 for Itanium®-based Systems OS to support only these three roles: database serving, Line-Of-Business (LOB) packaged applications (like SAP), and custom applications, boosting its mission-critical features. This newest MS Itanium® OS is now a narrow niche, high-end-only, Windows Server 2008 subset, targeted to compete with RISC-UNIX systems only in those three roles. Microsoft also offered SQL Server 2005, and now ships SQL Server 2008, for the above Itanium®-based Windows OS for platform data-serving duties. Both the full-function Windows Server 2003 for Itanium®-based Systems Editions above passed their EOS dates at end-March 2009, and so are now no longer sold. Declining Microsoft interest in what must have been a costly Itanium®-based systems OS development/support effort that yielded only a modest Windows Server 2003 for Itanium®-based Systems installed base (most HP), is quite evident. It seems unlikely that this was a profitable Microsoft business, unless Intel and/or HP funded the Redmond giant's costs to keep this Itanium®-based system Windows Server OS code-base alive to date.

HP-UX remains the most widely-used, and most important, HP Integrity operating system, and is today a fairly strong enterprise UNIX, supporting the MPU hardware features of Intel® Itanium® MPUs (including VT virtualization support, MT multi-threading, dual-core, and RAS features, etc.), as well as features specific to HP Integrity hardware. Linux provides the main OS alternative, with a choice of two enterprise distributions from Red Hat and Novell SUSE opening up an extra HP Integrity Linux applications pool, as well as open source software world capabilities. HP is to be commended for porting, and for continuing support of, OpenVMS on the HP Integrity platform, enabling ex-AlphaServer OpenVMS users to carry forward their workloads onto more modern HP hardware. However, most enterprises needing scale-up Windows Server higher-end SMP platforms select the mainstream Windows Server 2008 Datacenter Edition OS, running on x64-MPU-based hardware, over HP Integrity. Ditto for scale up Linux workloads, where x64 platforms are also preferred. Interestingly, most HP Integrity customers run only one OS on each system, highlighting that single-purpose deployment remains common on this platform, unlike the mainframe.

## HP Integrity Server Performance – Mostly Outclassed for Most Time Periods

HP was badly handicapped in enterprise server markets by the usually off-the-pace **absolute performance** of HP 9000 Itanium® and HP Integrity servers, on most UNIX-type workloads and benchmarks, over most time periods from the first 2001 HP Itanium® server debut, to our early-Q2 2009 time of writing.

HP Integrity servers mostly performed below, or much below, IBM's POWER4 to POWER6 MPU-based RISC-UNIX servers, the market's absolute performance leaders over most of this period, and were also sometimes outrun by Fujitsu SPARC64, Sun UltraSPARC RISC, and by some high-end Intel® Xeon® processor MP systems (including IBM X Architecture System x, Unisys ES7000, NEC Express). Only for certain short MPU transition/overlap periods, did HP Integrity systems muster significant benchmark wins in this eight-year period. HP/Intel performance claims were most muted for the especially weak Itanium® 9100 Series (Montvale) MPU-based, current HP Integrity generation when these shipped at end-2007, and for good reasons given the paltry performance advances they provided.

Currently, IBM POWER6/6+-based Power™ System servers hold over 70 world-top absolute performance benchmarks for a wide spectrum of workloads and system sizes, most showing 2-

3 times the performance per core of current HP Integrity and Sun SPARC Enterprise competitors, as well as top absolute performances on many. (Source 17, page 76.) **These IBM systems also hold price/performance leadership firsts** on many of the same tests versus HP Integrity, and Sun SPARC RISC-based, systems. The IBM Power Systems™ 595 top-end server remains much the world's most powerful server. This pattern of IBM POWER-RISC MPU-based server benchmark leadership over HP Integrity has been so pronounced, is so widely documented, and has persisted for so many years, there is no point in our including the extensive server performance benchmark data here, as these are all on the record. (Source 23, page 76.)

**Performance per processor/core** is today the most important server/MPU performance metric. The fewer cores needed to run a given workload, the better. The software stacks that most RISC-UNIX enterprise servers deployed in commercial IT run (OS, database, middleware, enterprise applications, Business Intelligence (BI), etc.) cost (license and maintenance total) several-fold more than the server hardware they are deployed upon, under all proper 3- to 5-year TCO ratings.

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*...IBM POWER6/6+-based Power™ System servers hold over 70 world-top absolute performance benchmarks...*

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Servers with higher-performing MPU cores need many fewer costly software core licenses, providing major lifetime software cost savings versus equivalent capacity, but lower performance/higher core-count, systems. Current HP Integrity systems needed 2- to 3-times more cores to equal the performance of IBM POWER6/6+-based, or z10 mainframe systems, making their software license/maintenance costs far higher than for equivalent capacity IBM Power Systems™ or System z10™ servers.

We review, assess and compare MPU and system architecture differences that explain these wide system performance differences between IBM's Power high-end servers and System z10™, and HP's Integrity systems with Itanium® MPUs in Section 5.

## ISV Software Support on Itanium®-based Systems – Range Much-exaggerated

Enterprise users need a wide choice of modern, well-supported software from leading ISVs as well as from many specialist providers, that are current with, and well-optimized for, their chosen hardware/OS platform.

Lack of ISV software for Itanium®-based systems much-deterred sales in the platform's first five years. Competing RISC-UNIX server vendors Sun and IBM long touted figures around 15,000 and 12,000 for applications their server platforms supported by the mid-2000-decade, whilst the Itanium® applications count remained far lower then.

So how many ISV applications are actually now available for Itanium® MPU-powered platforms in early Q2 2009? We turned first to a recent Q1 2009 ISA presentation, where that number was claimed to be "14,000 applications". Then we consulted the ISA Web site, where the number was "more than 13,000 applications" (at 16.04.2009). HP's Integrity Web pages also quoted "13,000 applications", implying all these were available for HP Integrity systems. (Source 21, page 76.) Big, impressive-sounding numbers in each case, and 14,000 is certainly "more than 13,000". What's a thousand applications difference here or there in Club Itanium land, where the sun always shines and all is quite wonderful? But are these numbers actually true?

*The ISA, and HP and Intel quoting their number, thus all far exaggerate the size of the Itanium® applications portfolio, according to our sample by some 65% to 70%.*

We looked more closely, examining the source of these much-quoted numbers, the Itanium® Applications List – a huge Web table of ISVs, and products, etc. From a substantial sample of pages, it seems **the ISA has double- or triple-counted each real ISV application** just for different operating systems and/or releases, to reach their 13,000 or 14,000 application total. Eliminating this ludicrous double/triple counting suggested a more realistic figure nearer to 8,000 across all the operating systems. The ISA, and HP and Intel quoting their number, thus all far exaggerate the size of the Itanium® applications portfolio, according to our sample by some 65% to 70%. Plain English terms for this include **misleading, distortion, and deception**. See Appendix B for details.

## HP Integrity – Decent Systems Management Support

A broad family of modular, integrated server management tools are provided under the **HP Integrity Essentials** banner, supporting both HP 9000 and HP Integrity server hardware, and the latter's multiple operating systems (*HP-UX 11i, Linux, OpenVMS, and Windows Server 2008*). Management facilities offered vary across operating systems, with HP-UX offering the most extensive set. These support real and virtualized HP Integrity environments, with some limitations. (See Section 6 for our virtualization assessment.)

As foundation for system-level management of single or multiple HP Integrity servers, the firm now provides the unified **HP System Insight Manager (HP SIM) V5.3** software, also used to manage x64 HP ProLiant and HP BladeSystem servers, and HP StorageWorks disk arrays. HP SIM is a widely-used, generally well-regarded, integrated system-level management software tool, which operates in conjunction with the on-board **HP Integrity iLO 2** advanced remote management support built into each HP Integrity server's service management processor (*HP iLO 2 is also used on HP ProLiant and BladeSystem servers*). **HP Ignite-UX**, for example, provides faster deployment of HP-UX on multiple HP Integrity servers (*real or virtual*). **HP Operations Software for Unix** discovers, controls, and reports on availability and performance of large-scale IT environments, consolidating network, systems, storage, database, and application information.

These HP Integrity system-level management tools can also be integrated upwards to feed enterprise management software tools from the **HP Business Technology Optimization (BTO)** portfolio (*or into IBM Tivoli or CA Unicenter® enterprise management suite products*).

Overall, HP provides a comprehensive, integrated suite of modern, system-level management software for its HP Integrity platform, part used also to manage HP ProLiant and BladeSystem x64 platforms, and providing a decent set of management capabilities. Additional operating system-specific management tools are also included in/with the wider operating environments of some supported OSs.

*...HP provides a comprehensive, integrated suite of modern, system-level management software...*

## HP Software Stack – Some HP Integrity Value-add

HP remains a mid-range player in the global software industry, software comprising 2.6% (\$3.039B) of 2008 FY HP revenue, small beer compared to software majors Microsoft, IBM, Oracle, and SAP (*but growing fast at ~20.0% that year*). HP abandoned its own failed core middleware software efforts earlier this decade, to rely on third-party ISVs such as Oracle, IBM, and TIBCO, et al, for database systems, application servers, Service Oriented Architecture (SOA), integration software, and Application Development (AD) tools for use on its server platforms.

The value-add that HP's own software portfolio thus brings to the HP Integrity platform cannot thus approach the value-add that IBM Software Group's massive, leading-edge middleware and tools stacks – both today extremely strong on the System z mainframe and on the IBM Power Systems™ family platforms – bring to users of both IBM enterprise platforms, and for which they are most fully optimized and most-tightly integrated/coupled.

HP itself supports two in-house HP Integrity operating systems – HP-UX and OpenVMS – with their added layers of HP server/storage management, clustering, virtualization, and disaster recovery software that enable its enterprise platform solutions. HP's main software business remains centered on enterprise management, but the firm's Peregrine Systems (*helpdesk*), Mercury Interactive (*testing tools*), and OpsWare (*data center management*), etc., acquisitions extended that footprint somewhat. Now these are combined within HP's BTO portfolio. Many of these products, plus HP's platform-related middleware and server management software, are naturally offered for the HP Integrity platform, most under HP-UX, providing some value-add for HP Integrity server customers also selecting such HP software offerings.

## Next-generation HP Integrity Servers Q2 2010

The further six-months delayed, now promised Q1-2010 arrival of Intel's next-generation Tukwila MC MPU, new socket, and Boxboro MC chipset, means the next HP Integrity server generation will be announced/shipped from Q2 2010, after HP completes yet another system redesign and re-validation round needed for Intel's May 2009-announced, further Tukwila MC chip changes. Intel must now successfully complete and validate its chip (*and related platform*) design changes, sample revised MPUs and chipsets to all OEMs, then successfully ramp-up Tukwila MC MPU and chipset production and yields on its established 65 n.m. line, to the new time schedule above just announced. At least by using the long-established 65 n.m. process, Intel should achieve a faster production ramp-up and more respectable yields for Tukwila MC. But this process is now far behind the 45 n.m. technology Intel already ships its leading new x64 Nehalem Xeon® 5500 processors upon today.

As ever, HP remains dependent upon Intel. It can only complete its new server rework in synchronization with Intel's MPU delivery steps. HP volume shipments of new Integrity generation servers depend on all going to plan on both sides. HP's new servers are thus now likely to ship from Q2 2010, although the new range may arrive in more than one drop. It was amazing that Intel again had to announce yet another half-year delay in May 2009, and this new slippage further dented already-fragile Itanium® credibility.

HP will be eager to get these new HP Integrity systems out, for several reasons. Firstly, the significant Tukwila MC performance jump (*discussed in Section 2*) will make these new HP Integrity systems much better performers than all their predecessors to date. HP has endured a severe beating from RISC-UNIX competitors IBM, Fujitsu, and even Sun, as well as from x64 platforms, on performance, performance/core, and often on price/performance too, over recent years, and so desperately needs this performance boost. However, we assess this advance will not be enough to make new HP Integrity servers competitive with their 2010 opposition.

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*...whilst BCS's now-dominant (90%+) HP Integrity server revenues (both Integrity lines combined) fell 18% YTY...*

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Many would-be HP Integrity buyers wanting newest systems held back 2H 2008-on orders, intending to buy in early 2009 when new HP Integrity servers were then planned to ship. The first delay (*caused by Intel's February 2009 Tukwila MC schedule slip*) deferred many of these "on-hold" HP Integrity buys for another six months. Now, the latest, May 2009- announced six-month delay puts new server delivery back to Q2 2010. This, and recession impacts, already dented HP BCS revenues. These were sharply down 29% YTY for the latest Q2 2009 FY quarter, whilst BCS's now-dominant (90%+) HP Integrity server revenues (*both Integrity lines combined*) fell 18% YTY.

HP doubtless holds some pent-up order backlog for new HP Integrity servers awaiting volume availability, but the latest delay above will now force many of these patient HP customers to go elsewhere. The latest Itanium® delay also blew any HP hopes of booking significant amounts of new-generation Integrity server revenue before its 2009 FY-end (31.10.2009) date.

Enterprise customers previously considering HP Integrity purchases in 2009 should now reconsider their options and alternatives. They should certainly hold off all Integrity purchases until the new generation's details are disclosed, and the new systems ship, around Q2 2010. By then, HP will be more than eager for new business to recoup its delay-induced losses above, allowing savvy HP Integrity buyers to win increased discounts from the vendor during 2010.

## Claiming “Mainframe-like” – HP Integrity Plays Old RISC-UNIX Game

Since the late 1990s, distributed systems vendors sought to strengthen their larger UNIX enterprise servers in (*numerous*) areas of original enterprise platform weakness by gradually adding features/capabilities to their hardware and software copied from long-established IBM mainframe capabilities. Marketing terms like “mainframe-like”, “mainframe-class”, “mainframe-level”, and “mainframe-standard” were liberally applied by these UNIX vendors to almost every such advance, however minor, and however far behind IBM’s latest mainframes these remained. The reality this decade, however, was that:

- IBM System z mainframes advanced much faster than most competing UNIX systems.
- IBM’s \$10B+ of mainframe MPU, system hardware, and software R&D investment fuelled this new flood of mainframe innovation, with dramatic results.
- Functional and QoS gaps between the latest System z10™, and HP Integrity/other competitor UNIX systems, actually grew wider, not narrower as UNIX server vendors claimed.
- Extremely careful, detailed examination and comparison of each attribute/capability, not simple tick-box lists, are needed to show these wide differences, and what they mean in superior TCO, lower capacity/watt, and higher QoS, etc., fully.
- Amongst UNIX systems, IBM’s own IBM Power Systems™ servers incorporated more advanced, real mainframe-inspired MPU packaging, system architecture, virtualization, RAS, and software capabilities, than any other UNIX systems. These drew directly on IBM’s 45-year mainframe expertise, using the same team skills that actually built the System z10™ mainframe.
- At IBM, interchanges of technology also went both ways. The latest System z10™ mainframe, with its huge jump in performance and capacity and vast increases in bandwidth, made cost-effective use of very-high-performance, standard InfiniBand I/O interconnect technology, which far outperforms earlier proprietary IBM System z Self-Timed Interface (STI) interconnect links, yet costs less, for example. The z10 MPU also drew heavily on its close sibling, the market’s performance leadership IBM POWER6 MPU used in IBM Power Systems™ RISC-UNIX servers. For the first time ever, IBM mainframe compute-intensive performance climbed to near-UNIX best, complementing the mainframe’s already-leadership transaction processing, data-serving, and massive I/O handling, advantages.

*They simultaneously assault the IBM mainframe as an outmoded legacy platform, whilst recognizing and copying it as the enterprise platform gold standard in terms of features, functionality, QoS, and TCO...*

Both HP and Intel, with HP Integrity enterprise servers and Itanium® MPUs respectively, continued the disreputable old UNIX vendor pattern in recent years. They simultaneously assault the IBM mainframe as an outmoded legacy platform,

whilst recognizing and copying it as the enterprise platform gold standard in terms of features, functionality, QoS, and TCO, etc., rightly seeing it as their principal (*and winning*) competitor in high-end markets. Their systems/MPUs offer weak imitations that pack only small subsets of mainframe system and MPU capabilities, and actually remain as far, or even further behind, as ever.

## Other Important Enterprise System Capability Areas

A number of other major factors also need to be carefully considered and weighed, beyond those covered so far in this Section 3, when strategically evaluating and comparing enterprise server platforms. In our assessment, MPU technology and over a dozen other crucial enterprise server platform capabilities below sharply differentiate between what the latest real mainframe – the IBM System z10™ range – now offers, compared to the capabilities offered by challenger UNIX systems like high-end HP Integrity rx and Superdome systems. These differentiating capability areas are:

- **MPU Capability, Interconnect, Bandwidth, MPU-level Performance.**
- **MPU Packaging, System Architecture, Chipset, Bandwidth, & System-level Performance.**
- **Specialty Processors and Dedicated Processors, Hybrid Processing Support.**
- **Single-system Scalability, Capacity, and Overall Workloads Throughput.**
- **Clustered System Scalability, Capacity, Manageability, Resilience, and Workloads.**
- **Range, Granularity, and Flexibility of Capacity On Demand Offerings.**
- **Range, Quality, Functionality, and Advance Rates of OS Environments Supported.**
- **System Virtualization, Partitioning, Workload Management, and System Utilization.**

- **Platform Business Service Reliability, Availability, Serviceability, and Disaster Recovery/Business Continuity (DR/BC).**
- **System Security, Protection, Control, Audit, and Integrity.**
- **Vendor Platform Middleware and Tools Software Stack.**
- **Platform Overall TCO/ Total Cost Per Transaction (TCPT).**
- **Platform Investment Protection and Safety/Risk.**

Rather than review what HP Integrity systems offer for these capability areas in isolation here, we compare them against IBM System z10™ mainframes on each in Section 5 (MPUs) and Section 6 (all other factors).

## HP Integrity – Our Analysis

Our first-level HP Integrity platform assessment conclusions are summarized below.

- **HP's Prime Enterprise Server Platform for Now:** After a difficult 6-year haul, HP Integrity platforms now dominate HP's BCS revenue. For its last three full FYs of 2008, 2007, and 2006, HP reported total Integrity system revenues of \$2,795M, \$2,274M, and \$1,352M, which were 79%, 64%, and 37% of BCS total revenues those years. (Source: HP 10K Returns FY 2008, 2007, 2006.) For the latest Q2 2009 FY quarter (to 30.04.09), BCS total revenue fell dramatically by 29% YTY, with majority HP Integrity (both lines combined) revenue falling 18% YOY (after years of growth), and thus with HP legacy platform revenue (now thought to be <10% of BCS) falling off a cliff. HP has now transitioned the majority of its legacy user bases onto these newer HP systems, but lost a substantial minority to competitors (mainly to IBM, also to HP ISS systems) through base migration/erosion. New sales of all HP legacy systems have now ended. During this long transition, **HP's UNIX server and high-end server market shares both fell**, and BCS revenue dipped slightly.

- **Itanium® Delays/Problems Injured HP:** HP lost market share, saw its enterprise server reputation hurt, and incurred large costs, through the many Itanium® delays, course changes, under-performance, and software shortages (covered in Section 2). These often left HP Integrity systems off-the-pace as new HP server generations lagged competitors. Reworking HP server ranges for Itanium® roadmap changes also added large extra costs to HP's multi-\$B cumulative Itanium® investment (not publically quantified). HP bet its enterprise systems future on Itanium®, burnt all its bridges, and thus saw no choice but to continue with Itanium® to date.

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*HP bet its enterprise systems future on Itanium®, burnt all its bridges, and thus saw no choice but to continue with Itanium® to date.*

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- **HP Integrity Revenue Profitable:** Multi-\$B HP Itanium®-sunk investments aside, we estimate HP reached current-year operating profits on Integrity systems in 2006, and did better in 2007 and 2008 (when both Itanium® lines together hit 79% of HP BCS revenue). Years more of similar sales (not a given) would be needed to recoup HP's sunk Itanium®/Integrity investments, if these are ever repaid. HP did, however, escape from its PA-RISC/Itanium® chip development costs from 2005 onwards, a large saving. HP's Itanium® deal with Intel remains a closely-guarded secret.
- **Broad Server Family Range:** HP's Integrity server family spans a broad range of capacity/power/price points, from a single-processor Integrity blade server to a 64-MPU/128-core Integrity Superdome top-end enterprise server. This wide server range, plus the four diverse operating systems families supported, with their clustering options, provides customers with many alternative Integrity hardware/software topology and configuration options.
- **Familiar, Common Hardware Design:** HP Integrity servers are of relatively simple server design and construction at all points across the range, familiar to HP 9000 users. The two HP Integrity blade servers were the family's main innovation in recent years, apart from Itanium® MPU generation upgrades. All family servers are engineered with reasonable, but not outstanding, enterprise robustness appropriate to their roles. No advanced MPU packaging is used, and simple main-board or cell-board physical construction is used, not a high-reliability, high-density, nor a low-latency, approach. Although unsophisticated, this approach helped ease customers' (and HP's) transitions from HP 9000 PA-RISC to the HP Integrity Itanium®-based platform. Some changes to the server line-up are certain with the new quad-core Tukwila MC MPU.
- **System Architecture Restricted by MPU Constraints:** Using "lowest-common-denominator" Intel® Itanium® MPUs (like other Intel® Itanium® OEMs), with their fixed, low signal I/O counts, heavily restricted HP's innovation, differentiation, and system-level optimization possibilities, in the HP Integrity family. HP rightly focused its innovation and value-add on building two HP server chipsets over two generations, on virtualization, into supporting the four operating system families, into clustering support, into the system management software provided, and into adding relevant HP Services offerings. (We assess the results of some of these efforts in Section 6.)

- **x64 Decimates HP Integrity Low-end & Blade Prospects:** HP Integrity low to-mid-range servers were severely undermined by Intel/AMD MPU-powered x64 server successes. ISS servers (*notably HP's own successful ProLiant x64 systems*) swept most Windows and Linux workloads, and moved rapidly up-scale in power/capacity. HP Integrity blade/entry-low-end sales are now restricted mainly to small HP-UX or OpenVMS scale-out workloads, and for use as Itanium® Architecture development/test systems. So HP Integrity's future battleground has now really retreated up into the mid-range and high-end scale-up SMP server segments, where it confronts entrenched IBM Power Systems™ RISC-UNIX server and System z10™ mainframe, as well as Sun/Fujitsu RISC-UNIX server, main competitors head-on.
- **HP ProLiant ISS 8-Socket Server Limit Nonsense:** HP Integrity sales were much-boosted by the firm's long-standing policy of restricting its ProLiant x64 ISS servers to <8-sockets. Over that threshold, HP says its customers should exclusively use HP Integrity (*Itanium®*) systems. HP and Intel both sought to keep 8-sockets as their Xeon® MPU server top limit, just to keep Itanium® alive. However, that limit is a technical nonsense, as other major enterprise system vendors have long showed. Without that limit, much of the case for Itanium® instantly evaporates. (*See below.*)
- **Scale-up x64 Xeon® Enterprise Server Competitors:** Other vendors (*IBM, NEC, and Unisys*) long proved that competitive, scale-up SMP-style c.c. NUMA enterprise servers (*with <32-sockets/<128-192 cores*) could be built using Intel high-end Xeon® multiprocessor server MPUs, all breaking that artificial 8-socket limit. IBM X4 Architecture, Unisys ES7000, and NEC Express5800/A1160 systems are three main examples, all run Windows and Linux scale-up commercial workloads well. These systems post excellent commercial workloads benchmark performances, some better than those of HP Integrity mid-range and Superdome systems, and usually post better price/performance too. A next, Nehalem-EX-MPU based generation of such systems is due to ship in Q1 2010, promising huge performance advances, and rendering these fearsome competitors to HP Integrity larger systems.
- **New and Renewed Enterprise Server Competition:** The enterprise server industry landscape also just recently changed sharply, with two potentially-disruptive new HP competitor events. One was Cisco Systems' recent big plunge into the enterprise data center market with a new generation of unified (*Intel x64-based*) server, storage, and networking systems, highly-threatening to HP's volume standard server, storage and ProCurve networking businesses. The other is Oracle's planned acquisition of Sun Microsystems, likely to renew/strengthen Sun's competitive push with its recently-fading SPARC-based RISC-UNIX servers running Solaris, and also likely to weaken HP-Oracle partnerships. Both these major competitors will impact most heavily upon HP as their new efforts ramp up.
- **Tougher Times Ahead for HP Integrity:** HP faces far tougher times, and stronger market battles over the next 2- to 3-years than it faced so far with HP Integrity. Current pent-up order backlogs for new-generation Tukwila MC-powered HP Integrity servers may provide a sales lift when they finally ship in Q2 2010. These new HP Integrity systems will also provide a solid performance boost, but will not gain leadership, we assess. Most HP Integrity revenue to date came from replacing HP legacy platforms, but that process is now in its late stages, with replacement revenue dropping off. The economic recession hit developed global markets hard, IT spending is well down this year, so new enterprise server deals will be also be fewer and much harder fought.
- **Could HP Escape Deadly Itanic Embrace?** HP's enterprise system business now depends completely on Intel® Itanium® MPUs, as its last legacy system users migrate onto HP Integrity in the next year or two. If Intel does abandon Itanium® after its current roadmap pledges expire by end-2012 (*as many expect*), what could HP do next, with its in-house MPU chip design skills long gone? We know HP could readily build high-performing, cost-effective x64 Intel Xeon® (*Nehalem-EX*) MPU-powered enterprise servers, like the competitors mentioned above. Breaking its own self-imposed x64 <8-sockets-only limit, HP would just need to port HP-UX (*and associated middleware*) onto these new HP x64 enterprise servers. Linux and Windows are already in great shape on x64. It could then again migrate current HP Integrity users running HP-UX across onto these new x64 platforms over the next few years. For NonStop OS and OpenVMS, HP has two choices. It could keep providing Itanium®-based Integrity Non Stop and Integrity servers for these software users for a few-year end-of-life period, and then phase out, and/or port these OEs to its x64 platform for longer continued life-spans. HP ported both before, to Itanium®, so this no doubt could be done, although would be costly and slow. These moves would allow a full HP escape from the Itanic curse.. With wide Windows and Linux x64 software portfolios available at once, and HP-UX offerings to follow, ISV software support would soon exceed that on Itanium®. Good synergy from sharing components with its high-volume ProLiant ISS server siblings would also help keep HP costs for these enterprise servers down. But the move would render HP Integrity customer Itanium®-based system investments prematurely obsolete again

- **x64 HP Integrity Replacement:** Current top-end “Dunnington” six-core Xeon® 7400 EX MPU-based systems posted strong commercial server benchmarks. (Sources 18, 19, and 20, page 76.) A further major x64 performance advance is now certain with the new 8-core Xeon® EX (Nehalem-EX) server MPU behemoth (with QPI interconnect and Nehalem micro-architecture, on 45 n.m. technology) now due in end 2009. A 32-socket enterprise server with this MPU could provide 256 cores, and 512 threads of x64 capacity by Q1 2010. Such x64 systems could be excellent HP Integrity Superdome replacements, with better performance than current (and next) generation HP Integrity systems, at lower cost through better Intel economics. According to Unisys, its own such x64 enterprise systems also now deliver actual RAS levels just as good as their similar Itanium® systems did. (Sources 18, 19, and 20, page 76.)

HP took six long years from its 2001 first Itanium® server launch until the end of its 2006 FY to first top \$1B in Itanium®-based server revenue (\$1.352B for 2006), still only 37% of HP’s BCS 2006 revenue, and this after twelve years of huge HP and Intel joint investment. Only by 2008 FY did HP finally earn a decisive majority of BCS revenue from Itanium®-based servers (both lines) at \$2.785B or 79% of the BCS total, still with 21% coming from the EOS legacy platforms. (Source: HP 10K Returns 2006-2008.)

IBM continues to be HP Integrity’s dominant competitor vendor, with the strong current IBM Power Systems™ (POWER6+) RISC-UNIX servers and System z10™ mainframes as formidable contenders today. With storming next-generation advances for both these IBM platforms expected during 2010, and near-certain to retain dominant performance leadership through 2012 at least, HP has little chance to best IBM here on current plans. IBM, together with new and strengthened enterprise server competitors Cisco Systems and Sun/Oracle, will thus force HP to fight considerably harder for every openly-contested HP Integrity deal from 2009 onwards.

## 4. IBM System z10™ Mainframe Again Leads Enterprise Computing

### Huge IBM System z Mainframe Success This Decade – Introduction

We published many prior studies of IBM System z mainframe hardware/software in recent years, examples listed on page 77. In this Section, we summarize our recent, high-level findings on IBM’s fast-evolving IBM System z10™ mainframe hardware/software platform, based on these prior in-depth studies. This decade witnessed an extraordinary turnaround in the business fortunes, industry reputation, server market revenue share, technological leadership, and dominance amongst high-end enterprise system platforms, of the IBM 64-bit z/Architecture System z mainframe. From 2000 to 2008, the IBM System z mainframe, currently in latest System z10™ generation form, **doubled its share of the high-end enterprise server market** (from 17% to 34% of over \$250K servers from 2000 to 2008), to again seize and hold the unquestionable crown as the most sophisticated and powerful enterprise platform for large, mixed, commercial workloads.

This Section provides our high-level, introductory picture of why IBM’s System z10™ mainframe has done so well in doubling its market share this decade, similar to our picture of the competing HP Integrity enterprise platform in Section 3.

### Resurgent Growth, Renewed Respect for System z Won Over 2000 Decade

IBM’s ~\$10B, many-year transformation won System z burgeoning new-to-mainframe workloads, new enterprise-wide roles, swelling market resurgence, and the renewed respect of most experts increasingly over the 2000 decade. Advanced technologies, continual innovation, soaring capacity, unique service qualities, specialty processor engines, leadership IBM System z middleware/tools software, and radical price drops, combined to drive this sharp System z growth. Most enterprise mainframe customers in developed Western IT markets re-embraced and sharply expanded their mainframe environments.

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*The five new System z generations that IBM delivered since 2000 set a blistering pace...*

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System z also won many all-new footprints, especially in China, Brazil, India, Russia, and other such emerging growth markets. The five new System z generations that IBM delivered since 2000 set a blistering pace of technology, software, and economic advances no competitor enterprise platforms could match; with the latest System z10™ generation a true tour de force of major advances in multiple dimensions.

Figure 7 (on page 32) shows our selection of recent proof-points of this dramatic System z growth and enterprise IT platform market leadership at our Q2 2009 time of writing. System z10™ is now deployed far beyond traditional mainframe spheres, workloads, and roles, and now offers a healthy, over-5,000 ISV software applications software ecosystem.

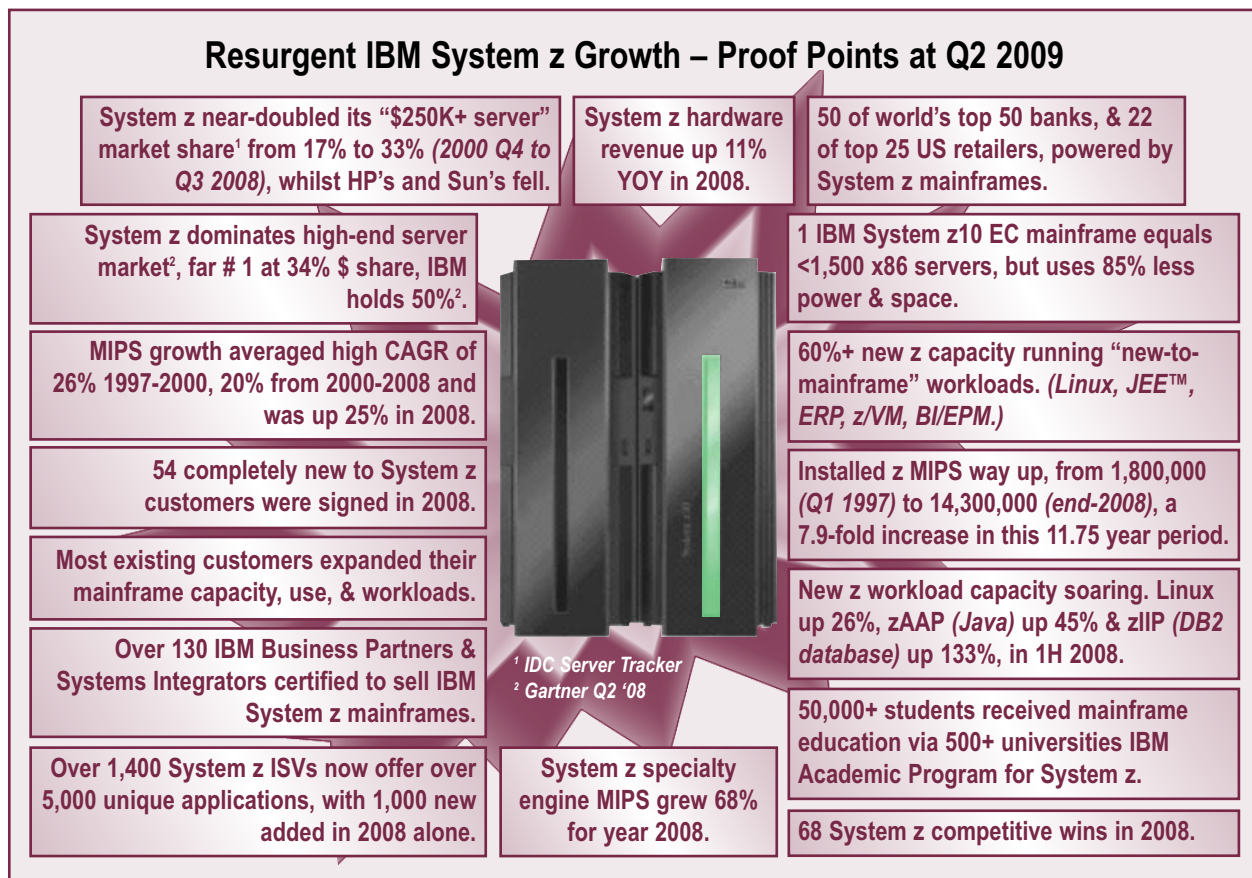


Figure 7: Resurgent IBM System z Mainframe Growth – Proof Points – Q2 2009

## New Workloads & Roles Mainframe Growth Drivers

More than 65% of post-2000 System z capacity growth was deployed to run new-to-mainframe workloads, and for new mainframe roles. These included new Linux applications and infrastructure tasks, mass-distributed server consolidation (*with z Linux under z/VM*), new-generation Java Enterprise Edition™ (*Java EE™*) Web applications (*now under SOA and with Web 2.0 capability*), and enterprise-wide data serving (*with System z's powerful DB2 & Information Management System (IMS) database engines*). Centrally deploying ISV enterprise applications (*e.g. SAP, Oracle, plus vertical applications*), and implementing IBM's dynamic BI solutions under its Information On Demand vision, were other major new workloads.

Extensive IBM middleware software, tools, hardware features (*e.g. specialty engines*), operating system advances, and radical mainframe cost model and economic gains over this decade enabled these important new workloads to run exceptionally well (*and cost effectively*) on System z, their wide adoption sharply raising the total MIPS of mainframe capacity deployed to over 14.3M by end-2008. This was a staggering, near-8-fold capacity increase since Q1 1997.


## 2008 Mainframe Banner Year – New System z10™, Four Major IBM z Software Domains Debut

2008 was truly a mainframe banner year, with highly-successful rollouts of the spectacular new System z10™ generation (*high-end and mid-range*), and of four strategic IBM System z software domains. We recap the former below, and the latter in a following subsection:

- IBM System z10™ Enterprise Class (z10 EC) – Major High-end Advances:** Our box headings in Figure 8 on page 33 summarize select System z10™ EC mainframe highlights, with more detail below. **Extreme scalability/capacity**, exceptional **new quad-core z10 MPU-powered performance**, **enhanced world-class middleware and tools software**, **"Gold Standard" virtualization**, and **35% price/performance gains**, were the five most notable z10 advances, we found. The z10 EC came in five models, starting from a just under \$1M US hardware price.



## System z10 Enterprise Class Mainframe Highlights – Biggest Ever Performance Jump



**IBM System z10 EC**

**Machine Type: 2097**

**Massive Scalability, Capacity:**  
 <64-way Symmetric Multiprocessing (SMP),  
 1.7X capacity\*, 3X memory\*,  
 <30,250 MIPS, 1-4 books.

**Stunning z10 MPU Performance:**  
 Quad-core, 4.4 GHz. -2.56X\*,  
 3MB L2/core, 991M transistors,  
 on-chip cryptographic, data  
 compression,  
 Decimal Floating Point -X10\*,  
 182GB/s chip bandwidth.  
 Close POWER6 sibling.

**Great Processor Flexibility:**  
 <77 total Processor Units (PUs),  
 <64 General Purpose Processors (CP)  
 SMP, <11 SAPs, 2 spare PUs. PUs can be  
 CPs, IFLs, ICFs, zIIPs, or zAAPs.  
 Each PU = c. 940 MIPS X1.6\*.

**Strongest System/Workload Management:**  
 Optimised cross-application & cross  
 LPAR, policy-driven workload  
 management. Smoothly runs mixed  
 workloads <100%.

**Superb, World-class Enhanced Middleware & Tool Software:**  
 Service Management Center for System z,  
 Smart SOA™, IOD, & AD/EM tooling.

**'Gold Standard' Virtualization:**  
 <60 logical partitions (LPARs),  
 <64 CPs /LPAR SMP.  
 Virtualized CPUs, I/O, Memory, Net. Runs  
 2X more z/VM virtual servers\*  
 <4 Logical Channel Sub-Systems,  
 HiperDispatch\*.

**Major Price/Performance Advances:**  
 c. 35-40% TCO savings\*. c 20%  
 hardware, <20% on software\*.

**Widest Capacity On Demand (COD) Range:**  
 Plus new 'Just In Time' COD.

**Massive Input/Output (I/O) Capability:**  
 <1,024 Input/Output channels,  
 <48 6GBps InfiniBand I/O interconnects\*  
 X2.2\*, 6GBps InfiniBand Coupling Links.

**Operating Systems:**  
 z/OS®, z/VM, z/VSE, TPF,  
 z/TPF, zLinux.

**5 Models:**  
 E12, E26, E40, E56, E64.  
 100 cap. settings on E12.

\* = Comparisons with z9 EC S54

IFL, ICF, zIIP, zAAP = Specialty System z workload processors

Figure 8: System z10™ Enterprise Class Mainframe Highlights – Biggest Ever Performance Jump

- IBM System z10™ – Stellar Performance Gains:** The z10 ultra-high frequency, 4.4GHz., quad-core MPU and system architecture delivered the largest-ever processor performance jump for any new mainframe generation in 45 years. With 1.7-times more system capacity, 2.0-times the processor performance, 3-times the memory support, and 2.2-times the I/O capacity (all vs. the System z9 Enterprise Class (z9 EC)), the z10 added outstanding performance on processor-intensive commercial tasks, complementing traditional fortes of transaction, I/O, and data-intensive workloads. Users can now consolidate workloads off ageing, inefficient UNIX systems (HP Superdome, Sun Enterprise, Fujitsu Enterprise and PRIMEPOWER, etc.), as well as from hundreds of x64 servers, onto one z10 EC. We review how the System z10™ MPU achieved these dramatic gains, drawing on shared components, processes and concepts from its blisteringly-fast sibling IBM POWER6 MPU, in Section 5 from page 39.
- System z10™ Business Class (z10 BC) – Mainframe Goodness in Smaller Sizes:** October 2008 saw IBM introduce the entry-mid-range System z10™ BC mainframe, a competitively-priced (from \$92,000 US up) mainframe server offering almost all the capability of the high-end z10 EC in smaller sizes, with 130 capacity options from a single model. Using up to four 3.5GHz. z10 MPU quad-core chips, the z10 BC can combine running existing mainframe applications, with support for new modern applications, whilst also consolidating distributed applications more efficiently, all at highest levels of QoS, and offering almost all the other mainframe unique strengths. The IBM z10 BC was ~40% faster, had 50%+ more total capacity, and could support ~4 times the maximum memory of its predecessor IBM System z9 Business Class (z9 BC).
- Broad z10 Benefits:** System z10™ mainframes enable both medium and large enterprises to sharply reduce costs, reduce energy use, and slash complexity in their data centers, exploiting the mainframe's "Gold-Standard" virtualization, dynamic policy-based management, and new "Just-in-Time" Capacity On Demand options. With industry-best DR/BC options, and far-lowest TCO for large commercial workloads, System z10™ is today's most compelling enterprise platform and Dynamic Infrastructure hub (see below).

- **IBM's "Dynamic Infrastructure (DI)" Hub:** System z10™ is IBM's cornerstone hub for hosting DIs for its enterprise customers. This strategic new enterprise vision offers IBM customers a roadmap to attain more efficient, dynamic business computing, and to co-managing physical business infrastructure over IP alongside IT from a common DI platform. Starting with infrastructure simplification, DI deploys cloud computing, extensive virtualization, management, and automation end-to-end over server, storage, and networking IT infrastructure, and extends management to enterprise physical plant and assets over the IP network. With System z10™ at its hub, a new Dynamic Infrastructure that responds far faster and more dynamically to changing business needs can be created.
- **\$3.5B Direct IBM Investment:** The System z10™ generation alone took a direct IBM investment of \$3.5B, and used 12,000 IBM staff for up to 5 years (*\$1.5B cost/5,000 people for hardware, and \$2.0B cost/7,000 people for direct software*). These huge mainframe investments once again showed IBM's unwavering commitment to its market-leading flagship enterprise system, and explains the major new advances and innovations this latest mainframe generation delivered.

These major 2008 mainframe advances further extended the platform's leadership and unique strengths; only a selection of which we highlight below.

## Strong System z Operating System Support

IBM supports five operating system lines on the System z platform, four IBM developed/supported, and has displayed laudable commitment to preserving long-standing customer investments in all these platforms.

- **z/OS®:** z/OS® V1.R10 (*a.k.a. V1.10*) is the latest shipping major release of IBM's rock-solid flagship, production operating system for System z mainframes, fully exploiting all z10 hardware advances, and is the 10<sup>th</sup> release shipped since z/OS® V1.0 was released in 2000. V1.11 is in development, with details on preview, for a September 2009 release. z/OS® is the direct z/Architecture lineal successor to earlier flagship IBM OS/390 and Multiple Virtual Storage (MVS) mainframe OSs. Robust, industrial-strength z/OS® offers strong investment protection, is well-suited to continuous, high-volume operations with high security and stability, and goes to great lengths to keep applications and data available, system resources secure, server utilization high, and programming environments adaptable, while maintaining long-term compatibility for customers' existing applications. With extensive autonomic technology embedded, smart and adaptive z/OS® technology today provides a secure, resilient, in a Dynamic Infrastructure that integrates business needs and IT capabilities. The pace and scale of development advances in z/OS® have been extremely high with those ten major releases this decade, new releases now regularly shipping each September, and each packed with substantial and significant advances. This strongly contrasts with the much slower pace, more limited content added, in HP-UX releases for HP 9000/Integrity between 2000 and 2009, with 2007's HP-UX 11i v3 the most recent major release.
- **Linux on System z:** Linux on System z blends all the above System z10™ advantages with the flexibility, open standards, and wealth of modern software available on Linux; including open source. System z Linux saw rapid, major growth this decade: today over 2,000 mainframe customers run Linux on System z. Both Red Hat Enterprise Linux (RHEL) V5 and Novell SUSE Linux Enterprise Server (SLES) V10.1 distributions are strongly supported by those vendors and IBM Global Services. Low-cost Integrated Facility for Linux (IFL) specialty processor engines (*and/or dedicated-all IFL System z10™ machines*) are highly cost-effective at a fraction of normal cost for Linux workloads. Distributed server consolidation, new Linux business applications, and efficiently running Linux infrastructure middleware, often alongside and closely-coupled to large-scale z/OS® workloads, fuelled this big success.
- **z/VM:** z/VM Version 5.4 is the latest version of IBM's famous z/VM "extreme hypervisor" that System z customers use to extend mainframe technology business value across the enterprise, by integrating applications and data whilst providing exceptional availability, security, and operational ease. z/VM virtualization technology allows customers to run hundreds to thousands of Linux servers on a single mainframe that can also run other System z operating systems, such as z/OS®. z/VM allows System z to be used as a large-scale, Linux-only enterprise server, using z/VM's proven capabilities to provide Linux guests with shared access to the mainframe's powerful resources. z/VM also enhances productivity by hosting non-Linux workloads running on other operating systems, such as z/OS®, z/VSE™ and z/TPF, such as test and development, as well as production, environments.
- **TPF & z/TPF:** z/TPF is the z/Architecture successor to TPF, the High Volume Transaction Processing (HVTP) platform of choice for many of IBM's largest customers for many years. These customers are found in several industries, including airlines, lodging/hotels, finance, health, and travel. This lean, efficient, HVTP OS makes maximum use of System z hardware resources to deliver massive Transaction Processing (TP) volumes securely and fast. z/TPF exploits select z/Architecture features.
- **z/VSE:** z/VSE V4.2 is the latest version of the robust, cost-effective, four decades VSE-heritage platform, designed to exploit selected IBM System z and IBM Systems Storage technology, and to address needs of VSE clients with a wide range of capacity needs, in most industries worldwide. z/VSE V4.2 advances focused on adding further improvements in scalability, security, interoperability, and SOA support. All mid-range System z servers can run z/VSE V4.2, and the release is eligible for Midrange Workload License Charges (MWLC) pricing with full-capacity and sub-capacity options on z10 and z9 servers.

In addition to this strong portfolio of four IBM-supported, and the two main Linux System distributions, operating systems on System z, another interesting development discussed below, may soon extend another option.

Sine Nomine Associates publicly demonstrated a working prototype of its **OpenSolaris for System z distribution** of the Sun-initiated OpenSolaris open source version of its Solaris OS. Sun put OpenSolaris out in source code to extend community development around its Solaris technology. A first release prototype, lacking some features, was made available free in October 2008 for testing, runs on IBM z/VM on System z, and can exploit IFLs. Whilst not yet commercially available, this development may enable OpenSolaris and Solaris workloads to run natively on System z in the near future.

## System z Mainframe Specialty & Dedicated Processors, On-chip Power, & Hybrid Processing

A highly-distinctive System z10™ feature is support for a range of specialty processor engines for common mainframe workloads. Specialty engines use the same powerful ~920 MIPS (*on z10 EC*) MPU cores as general-purpose System z CP processors, but are charged at a fraction of their price (*at an unchanged fixed price of \$125,000 on the z10 EC, and at a halved new \$47,500 rate on the z10 BC*) also with far lower maintenance costs. Specialty engines are crucially also free of any IBM System z software charges. Current z10 system specialty processors offer almost 50% more capacity than those on their z9 predecessors, at the same (*EC*) and halved (*BC*) prices compared to z9 predecessors, sharply increasing value. In addition, any upgrading System z customer already owning specialty engines uniquely receives the full, much higher capacity of each new generation replacement at no extra charge, great investment protection. System z software automatically redirects qualified workloads to the appropriate specialty engine processors where installed, without any application changes needed. The specialty, and other standard System z10™ processor engine roles, offered today are:

- **IFL:** Specialty Integrated Facility for Linux (*IFL*) processor, a cost-effective, dedicated off-load processor for all Linux workloads on System z. All-IFL, Linux-only System z10™ EC and z10 BC mainframes may also be ordered for exclusively Linux workloads.
- **ICF:** Specialty Integrated Coupling Facility (*ICF*) processor, a dedicated specialty processor for Parallel Sysplex® cluster coupling workloads, reducing the cost of implementing high-availability Parallel Sysplex® and Geographically Dispersed Parallel Sysplex® (*GDPS*®) clusters.
- **zAAP:** Specialty System z Application Assist Processor (*zAAP*), a dedicated, off-load processor for Java and eXtensible Markup Language (*XML*)-related workloads, such as those generated by WebSphere Application Server, and by SOA applications.
- **zIIP:** Specialty System z Integrated Information Processor (*zIIP*), a dedicated, offload processor for certain important DB2 data serving workloads, as well as data warehousing, BI, and Enterprise Resource Planning (*ERP*) workloads.
- **SAP:** Appropriate numbers (*3-11 on z10 EC, 2 on z10 BC*) of System Assist Processors (*SAPs*) come as standard on all IBM System z10™ servers, and are dedicated I/O processors that improve efficiency and cut I/O processing overhead for every IBM System z LPAR and System z OS running on the machine. Additional *SAPs* can be designated for highly I/O-intensive workloads.
- **CP:** System z10™ general-purpose Central Processor (*CP*) for all standard system workloads.
- **Spare:** A System z10™ not designated as any of the above, which provides back-up in case of any other Processor Unit (*PU*) failing. 2 Spare PUs per System z10™ EC are provided as standard.

The huge success of the System z specialty engines can be gauged from the fact that their combined installed capacity has grown by a staggering 93% CAGR yearly from 2003-2008. As planned, they made their supported workloads far more attractive and affordable to run on System z mainframes, and have been a significant factor in mainframe success.

- **More Extensive On-MPU Functions Boost z10 Throughput:** Another important, not always apparent, factor that helps to explain the huge workload capacity of System z10™ mainframes is the considerably larger number of common functions and tasks, which the System z10™ performs on-die within its MPU chip at many-fold higher hardware speeds in silicon, that competing enterprise systems must perform in far slower operating systems or middleware software running on their standard processors. Additional workload functions have continually been moved onto System z MPUs over successive generations. The z10 MPU now includes extensive virtualization support, cryptographic processing, database compression processing, Decimal Floating Point, and the most extensive RAS support of any MPU, etc., enabled by its extensive 894 instruction CISC ISA and 991M transistors. Such optimization is only possible with the System z10™'s MPU that is dedicated solely to, and completely optimized for, mainframe-specific workloads only. No servers based on lowest common denominator, standard MPU designs (*such as HP Integrity using Intel® Itanium® MPUs*) and aiming to meet wider diverse needs, can match its performance on these functions. The differences between the performance of such functions run on-die in-MPU hardware, versus in OS or middleware software on standard MPU is often massive, ranging from one-to-three magnitudes.

- **Hybrid Processing Complements System z10™:** Strong though System z10™ is today for its broad, targeted workloads and roles, IBM recognizes that not every type of workload, application, or function is always best processed on the platform's standard processors, able though these are. Optional, onboard cryptographic co-processor cards have long been offered for System z to provide still-higher throughput for demanding crypto-processing workloads like Secure Sockets Layer (SSL) transactions. Such dedicated, special-purpose, performance-boosting cards are one familiar form of hybrid processing, in this case, on-board and closely-coupled. Other good example is SOA XML parsing, security, and messaging tasks, all heavy workloads for general-purpose systems in software, yet central to large enterprise SOA deployment. Here, dedicated, low-cost SOA hardware appliances, such as the IBM WebSphere DataPower range that now offers five such specific appliances, are ideal solutions. These can be loosely-coupled with a System z10™ mainframe (*or other hosts*) serving as enterprise SOA application hubs, to offload demanding, specialist tasks like these, increasing overall SOA application performance and sharply reducing host processing costs.

A third emerging hybrid-computing case is where an important enterprise application needs to combine high-Giga Floating Point Operations Per Second (*GFLOPS*) imaging, gaming, and graphics-intense type processing on the one hand, with classic mainframe database serving and secure transaction processing on the other. Here, IBM's extraordinarily high-performing IBM PowerXCell™ 8i processor (*an enhanced version of the Cell Broadband Engine™ that powers the Sony Playstation 3*), offers extreme raw compute performance and bandwidth for the former at low cost, and can be loosely-coupled (*using a QS22 BladeCenter blade server*) to a System z10™ mainframe running the latter.

Other conventional IBM IT platforms also obviously complement System z10™. For example, some workloads' operating system/software stacks are not yet available to run native on System z10™ – Windows and Sun Solaris, for example. IBM System x and BladeCenter x64-based servers can support such workload needs, whilst interoperating with System z10™ DB2 data-serving.

Expect further extensions of all these types of hybrid computing in and around System z10™ mainframes and successors from IBM.

## Extensive Capacity on Demand (CoD) Options

System z10™ now offers the fullest range of permanent, temporary, and backup CoD options, covering processing capacity (*all engine types*) and memory. These options can now provide customer-initiated, dynamic capacity flexibility to cost-effectively meet varying customer workload needs, patterns, events, and demand profiles, without over-provisioning; improving QoS and reducing costs. System z10™ introduced radically improved, more flexible, Just-in-Time (*JIT*) temporary CoD options and facilities now including:

- **Permanent CoD:** Permanent upgrades of **all PU types and memory** for System z10™ EC servers, up to the server's maximum available PU and memory resources, can now be ordered as Customer Initiated Upgrades (*CIU*) over the Web, be downloaded, and be applied directly and concurrently by the System z10™ customer. Permanent CoD provides needed additional long-term capacity quickly, within a few hours under an Express option.
- **On/Off CoD:** Provides temporary access to unused PUs to augment installed system capacity so as to contain workload spikes, or peak workload periods, where permanent upgrades are not justified. The upgrade can be of CP capacity, or any/all specialty engine types, within physical limits. Up to four On/Off CoD scenarios can be installed, but only one can be active, and up to 200 can be staged on the Support Element (*SE*). Each scenario remains active for 180 days, can be turned on and off many times within that period, and can be replenished. One <24 hour long, no-charge test is allowed to validate scenario process operations. Thereafter, On/Off CoD hardware and software capacity is charged per 24 hours used. Various PU limits apply to On/Off CoD upgrades.
- **Capacity Back Up (CBU):** Provides temporary access to unused PUs, to replace enterprise capacity lost due to a disaster. Any of the machine's spare PUs available can be configured, as CP and/or any specialty engine types, for <10 days (*test activation*) and <90 days for a true disaster, with 5 test activations included. Time spans covered by CBU can be from 1- to 5-years, and extra test activations can be ordered in multiples of 5.
- **Capacity for Planned Events (CPE):** New for the System z10™ EC only, CPE provides temporary access to unused PUs to replace enterprise capacity due to planned events, like a facility upgrade, or a system relocation. Similar to CBU, but only for short-duration, planned events lasting up to 3 days maximum. Any of the machine's spare PUs available can again be configured as CP and/or as any specialty engine types.
- **z/OS® MVS Capacity Provisioning:** Provides automated control of temporary capacity, allowing users to set up rules for when additional capacity can be provisioned to meet a business need, based on practical criteria like specific application, maximum extra capacity, time, and workloads conditions. This support provides a fast response to capacity changes and ensures sufficient processing power will be available with the least possible delay even if workloads fluctuate.

The System z10™ now supports more flexible, JIT On/Off CoD, CBU, or CPE options above, including partial activation, options to extend On/Off CoD scenarios, allowing Permanent CoD upgrades to be made whilst any of the three temporary options are active.

## Superior System z Middleware & Tools Software

IBM made huge software investments over the 2000 decade, greatly extending its enterprise middleware and tools software portfolios, with the System z mainframe a central platform target in recent years. The result is now a comprehensive, leading-edge, IBM System z10™ software stack, tightly integrated with, and optimized for, the foundation System z software engines, including DB2 for z/OS®, CICS, IMS, z/OS® and z/VM, which themselves have also advanced at unprecedented rates. Four major System z leadership software domains, each the culmination of years of investment and innovation, are now:

- **Market-Leadership IBM Smart SOA Software on System z:** Open industry standards-based SOA has become the almost universal way modern enterprise applications are now built, deployed, integrated, managed, governed, and secured, delivering compelling business and IT benefits. Since 2004, IBM built a market-dominating <64% market share winning, extensive SOA and Business Process Management (BPM) middleware/tools software and services portfolio, especially strong on the System z10™ mainframe. This was the result of a 5-year+, cross-company, multi-\$B IBM SOA effort, including many ISV acquisitions. Today, over 1,500 System z customers have already adopted IBM WebSphere SOA mainframe software, transforming core business processes by hosting new, enterprise-level, composite SOA applications. These new SOA solutions easily link/reuse their rich mainframe applications, transactions, and database assets with newly-built software, to create new workflows bringing major new business value. Highly virtualized, massively scalable, energy-efficient System z10™ mainframes easily host scores of such enterprise, composite SOA applications, supporting thousands of users, accessing large-scale mainframe DB2 or IMS databases and proven CICS transactions, at highest efficiency, with complete reliability and security, and at the lowest TCO. Smart SOA extended rigorous Process Integrity to IBM's SOA offering, uniquely differentiating System z as the only platform offering a totally secure, high-QoS, widely-scalable, enterprise-wide SOA hub, providing seamless synchronization between services, human tasks, and information.
- **Great System z Development Tooling Today:** By 2008, IBM Rational had transformed the System z Application Development/Enterprise Modernization (AD/EM) tools portfolio. This became an extensive, modern, world-class and Smart SOA-supportive, Rational Software Development Platform (RSDP)-based, major asset to System z users. All types of development, including traditional CICS, IMS and batch, as well as modern SOA-composite, integration, BPM-based, and Web 2.0 application styles, are supported. Both traditional host languages COBOL, PL/1, and Assembler, plus modern C/C++ and Java EE™ languages/skills, are fully supported in these cohesive System z Integrated Development Environments (IDEs). Open Eclipse-platform-based, these tools now provide a superior IBM z IDE, tightly coupled to, and well integrated with, the full System z software environment, easily extensible with add-ins from other ISVs. This facilitates mainframe software asset reuse in SOA, leverages and supports both traditional and newer languages/skilled developers in highly productive IDEs, and supports newer application styles (SOA integration, BPM-based, Business-Event-based, and Web 2.0 mashup) to the mainframe. Rational's exceptional team development facilities now also support such mainframe developments, improving team collaboration and responsiveness. We now assess this System z AD/EM tooling as considerably superior to that available on any other enterprise system platform, and a big advance.
- **Enterprise Information on Demand (IOD) From System z:** IOD is IBM's ambitious, four-year-old strategy that has delivered an innovative new generation of IBM Information Management (IM – home of DB2, IMS, Informix, etc.) software solutions and services, with strong System z10™ versions centrally featured. IOD helps global enterprises rapidly deliver trusted, reliable, accurate, consistent, and current information, as-and-when-needed (both structured data and unstructured content) to applications, business processes, and people, throughout the company. IOD complements SOA, the two closely linked via open standards, feeding vital information into SOA composite applications. IBM made over 25 significant ISV acquisitions, and has invested over \$15B (our estimate) in IOD so far; a major effort even for IBM. This included IBM's largest-ever, \$5B acquisition of BI leader Cognos, whose powerful Cognos 8 BI/Enterprise Performance Management (EPM) suite is now an IOD centerpiece, on System z and other platforms. Other major new InfoSphere-branded products included the impressive IBM InfoSphere Information Server (for Extract, Transform, and Load (ETL) functions), the innovative IBM InfoSphere Master Data Management (MDM) Server, the recent new unified IBM Data Studio data development tool, and the IBM InfoSphere Data Warehouse based around DB2, all now offered on System z. This powerful new IBM IOD software now enables System z10™ mainframes to efficiently serve as the enterprise-wide "IOD hub" for real-time dynamic data warehousing, and world-class business BI/EPM, delivered via the IBM Cognos 8 offerings, underpinned by the other InfoSphere products mentioned above, and by DB2 on z/OS®. Exploiting z Linux and z/OS® environments combined, these powerful, new System z IOD offerings moved IBM far ahead of its IM software competitors (Oracle, Microsoft, Sybase, Teradata, and Informatica, etc.).

- **Enterprise-wide Service Management from System z10™:** Central to IBM's Dynamic Infrastructure strategy is IT Service Management (*ITSM*) that enables major IT processes to be automated on industry best-practices. Introduced in mid-2008, the Service Management Center for System z (*SMCz*) provided powerful software to deploy ITSM over all enterprise IT platforms and operations processes, with System z10™ acting as the enterprise-wide hub integrating and managing business services end-to-end. SMCz brought powerful process automation and service management, using proven best practice processes from the IT Infrastructure Library (*ITIL*) V3. New IT financial management capabilities also empower IT departments to accurately account/recharge IT resource usage, and better manage software licenses and IT contracts, from a mainframe. Policy-driven processes, like incident and problem management, change and release management, discovery, and business service management, can all now be smoothly managed enterprise-wide from a System z hub. SMCz combined new IBM Tivoli-developed software, software from important IBM Tivoli ISV acquisitions, and enhanced releases of existing Tivoli System z operational management tools. New System z-based service management platform capabilities discover, standardize, and share crucial IT operations information about the whole enterprise application infrastructure. SMCz enables enterprise-wide industrialization and automation of IT operational processes, directly linking IT service performance to Key Performance Indicators (*KPIs*) of the business, helping to cut IT operations costs sharply.

In these four main areas, this IBM System z software is now considerably ahead of that available on other enterprise hardware platforms from competitors, and will often alone justify System z10™ selection/purchase.

## Our Analysis – z10 Advances Extended Now Unrivalled Mainframe Strengths

The advances in Figure 8 above further strengthened System z10™ absolute enterprise server leadership in a number of other major areas, as well as those noted above. These included:

- **Gold-standard, Industry-best Virtualization:** The System z10™ extends the mainframe's long record of pioneering the most powerful, fine-grained, refined, and flexible virtualization capabilities of any IT platform. Many applications can be safely run in a single LPAR partition, with securely-enforced isolation for each in true multi-tenant processing. System z10™ can share all CP, memory, I/O, and internal network resources, flexibly across up to 60 rock-solid, secure, dynamically adjustable LPAR partitions, running all-supported System z OS mixes. In addition, the extraordinary z/VM extreme hypervisor allows up to 1,500 significant (*x64 2-way server workload-sized*) Linux virtual servers to be consolidated on one System z10™, amongst other invaluable roles. Unique internal virtual networking provides huge savings and performance gains over external, network-linked applications. Other UNIX vendors' virtualization offerings remain relatively primitive by comparison.
- **Industry-best Resource Utilization:** The System z10™ gold-standard virtualization above combines with outstanding, long-optimized, within-partition, multi-tenant workload management (*z/OS® Workload Manager*), and the impressive Intelligent Resource Director (*IRD*) across-LPAR workload optimizer, to deliver premium QoS levels defined through policy for each workload. These combined allow System z10™ mainframes to reliably and smoothly run at up to almost 100% utilization rates. Competitors' large UNIX systems rarely better 40-45% average utilization rates, mid-range UNIX or x64 servers often average 15-20%, and traditional x86 volume ISS servers 5-10% utilization. Huge savings in support staff, software license, power/cooling, and total costs over 3-7 years, are therefore available by consolidating workloads off these wasteful platforms using virtual Linux servers on a shared System z10™ mainframe under z/VM.
- **Extreme RAS with “Never Go Down” Service Delivery:** These attributes are deeply engineered throughout the System z10™ MPU and into every level of hardware and software, and extend far beyond those of even the best UNIX or Intel-MPU-based servers. The list of System z10™ RAS capabilities runs to many scores of items, and has been extended systematically over 10 IBM CMOS mainframe generations since 1994. Single-system hardware Mean Time Between Failure (*MTBF*) is now measured at 50-60 years, with service availability at 99.995%+. With Parallel Sysplex® mainframe clusters ~99.9995+% service availability can be achieved.
- **Far Highest Security Levels of Any IT platform:** Built in throughout the z10 hardware and software stack, including on-MPU-chip cryptographic, and specialized cryptographic co-processing cards for extraordinary crypto performance, Evaluation Assurance Level (*EAL*) 5 certification, rock solid security and access management software, and scores of other advanced security capabilities, are again far in advance of any UNIX/distributed system, and have long provided the most highly-trusted, never-broken levels of security that no other commercial IT platform approaches.
- **Huge I/O Capacity and Capability:** With their unique, channels I/O architecture (*which uses hundreds of embedded MPUs*), supporting up to 1,024 I/O channels per z10 system, and their powerful, dedicated central SAP I/O processors (*<11 on a top z10 EC*), System z mainframes easily handle huge data-serving, transactional and application serving I/O-intensive workloads that bring other vendors' UNIX systems to their knees. Up to 48 ultra-high performance (*6GB/s*) standard InfiniBand-based links are now used on the System z10™ for the I/O interconnects, with others used for Sysplex cluster coupling, each at 2.2X the capacity of prior, IBM-proprietary STI links. These links can now deliver a unique 288GB/s of system I/O bandwidth.

- **Most Scalable & Refined Full-system Clustering:** IBM z/OS® Parallel Sysplex® is the world's most scalable and advanced, refined, and mature enterprise full-system clustering environment for commercial computing. It extends the unrivalled single-system strengths of the System z10™ to an <32-mainframe cluster, of <2,048 processors and <968,000 MIPS capacity, that can be managed and run as a single System z system of still-higher availability (99.9995%+) and vast capacity, sharing workload efficiently across all mainframes in the cluster.
- **Top-end DR/BC Capabilities:** IBM's GDPS® service solution extends these z/OS® Parallel Sysplex® clusters to two or three-site distributed mainframe clusters, supporting the market's strongest range of DR/BC options, when combined with the enterprise-class IBM System Storage (DS8000 and DS6000) and IBM System Storage replication/recovery software options.
- **Highest Systems Automation Levels, Lowest Staffing:** For the last decade IBM poured continuous, major R&D efforts into implementing many scores of autonomic self-managing, self-optimizing, and self-healing features and capabilities throughout every level of the System z hardware, firmware, operating system, and middleware stack, all aimed to simplify and reduce the time and effort needed to manage and support mainframe workloads. This process has been triumphantly successful, achieving a cumulative 7- to 10-fold reduction in support staffing/effort per 5,000 MIPS of workload needed over the last decade. As a result, System z10™ requires from 1/3 to 1/5 the staffing level required to support/run equivalent capacity/workload distributed platform configurations, a major source of large cost savings with the mainframe versus distributed platforms like HP Integrity.
- **Fewer MPU Core Software Licenses:** Most middleware/system software, and many applications, are licensed by the number of processors/cores using the software. Where lower power, older distributed RISC-UNIX or x86/x64 servers are used, large numbers of software MPU/core licenses are needed at high software license and maintenance cost. With the typically low server utilization rates above, these software licenses are equally wastefully under-utilized. Consolidating such applications/workloads onto System z Linux under z/VM, using hugely powerful ~920 MIPS z10 (EC) IFL Linux specialty processor cores, each of which can be utilized <95-100%, and which cost a fraction of general CP processors, allows major savings. 20 to 30:1 software core license consolidation ratios are often achieved in such cases, bringing major software savings with System z10™.
- **Greenest Dynamic Infrastructure Hub:** System z10™ mainframes also have the smallest data center footprint, the lowest power, and the lowest cooling costs (*per enterprise workload and/or per 1000 users*), as well as providing the most flexible, highest QoS, and most secure service delivery. Just one actual example illustrates these major green savings. One IBM System z10™ BC (10 IFLs, 2 I/O drawers) equals the capacity of <232 x86 servers (1p rack x86 units) but has an 83% smaller data center footprint (z10 30 sq. ft. vs. x86 150 sq. ft.), up to 93% lower energy costs (z10 4.5 KW vs. x86 67 KW), and a much higher level of security, control and automation – allowing for up to 100% utilization.

In addition, these unique mainframe strengths combine and contribute to cost savings that now make today's z10 mainframes, both high-end and mid-range, often much the lowest overall 3- to 5-year TCO/Total Cost per User (TCU)/Cost-Per-Transaction (CPT) platform for mixed commercial workloads, Linux consolidation, data serving, and dynamic BI/EPM, workloads.

## 5. Enterprise Server MPU/System Architecture Battle Red-hot 2009-2011

### Today's Enterprise Server MPU Winners Clear – Ranks Dramatically Thinned

MPU and system architectures determine enterprise platform success, and divide winners from losers. The performance, economics, RAS, virtualization and security capabilities, power consumption, and other crucial enterprise server capabilities, are determined by the design, performance, and capabilities, of their MPUs, their packaging, the system architecture supporting them, and by the software stack that integrates all these parts into a complete platform.

Earlier wide diversity of CISC and RISC MPUs/system architectures dramatically thinned in recent years, as old MPU/system architectures passed EOL. At least eight, shown on the right-hand side of Figure 9 on page 40, are now completely dead/gone, with two more also nearing EOL. Three vibrant, successful, leadership MPU/system architectures now unquestionably dominate the 2009 enterprise computing MPU/system architecture landscape. These are:

- **IBM System z10™ mainframe CISC MPU, and z/Architecture mainframe system architecture.** High-end, scale-up enterprise server market leader MPU/system architecture platform.
- **IBM POWER6/6+ RISC MPU, and IBM Power Systems™ architecture.** RISC-UNIX server market share leading MPU/system architecture platform, dominant in high-end, scale-up UNIX systems.
- **Intel 64/AMD64 CISC x64 CISC MPUs and associated server architecture.** Now power most high-volume ISS rack and blade servers, workstations, and HPC clusters. x86/x64 MPUs now account for 50% of server market revenues, and most of the nearly 8M servers sold in 2008. Some scale-up, x64-based enterprise servers are also offered.

These three successful MPU leaders are shown on the left-hand side of Figure 9 as our “**Vibrant Leaders**”. The two high-end IBM MPUs are shown at the top of the chart, symbolizing their enterprise server market share-leading positions. The Intel/AMD x64 MPU-platform is shown bottom right, symbolizing its strong dominance in high-volume, scale-out ISS servers and HPC clusters. We firmly expect these three platforms to each extend their dominance in the next several years, based on their track record, and the planned strong advances their successors will deliver through 2009-2010, assessed next in this Section.

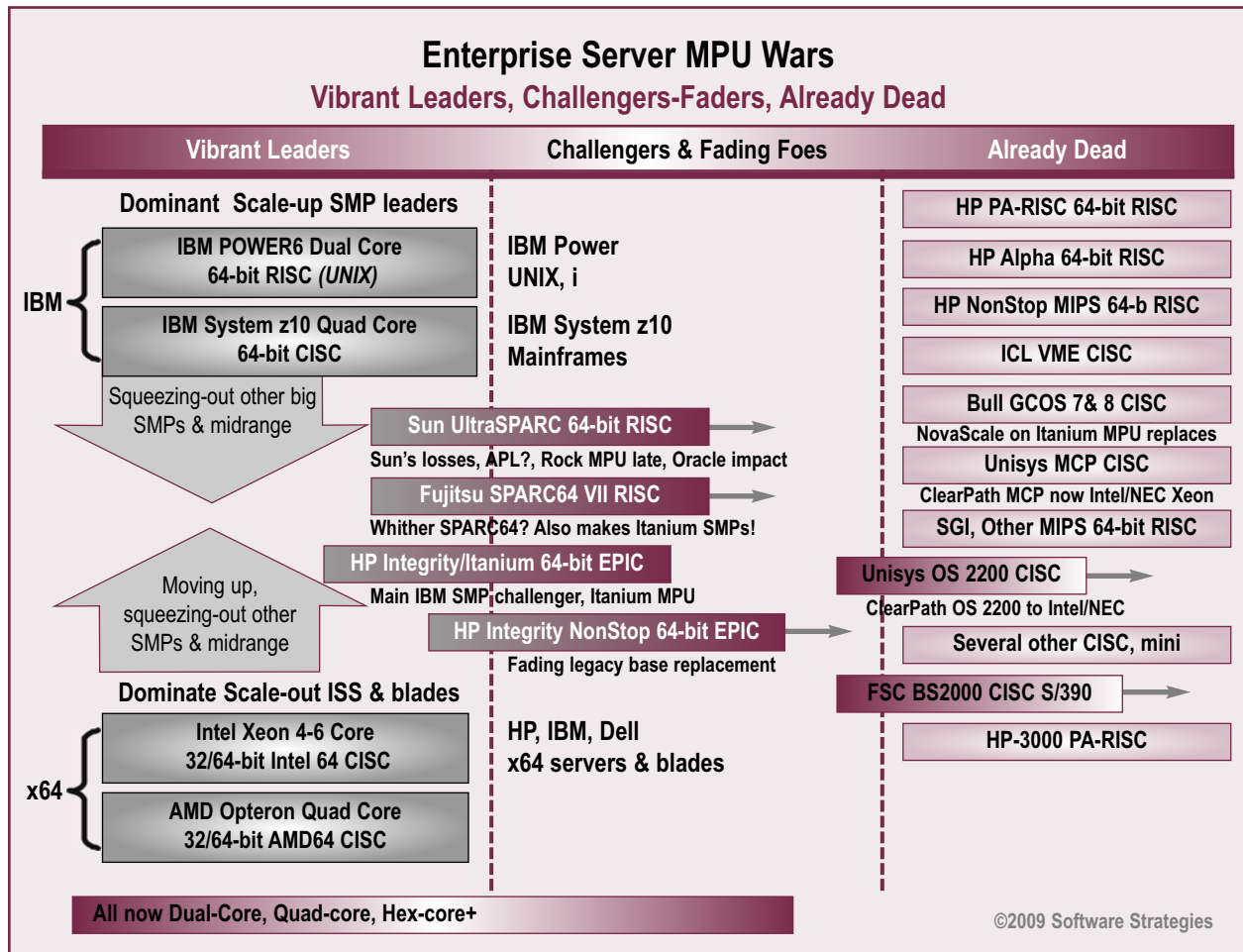


Figure 9: Enterprise Server MPU Architecture Wars – Vibrant Leaders, Challengers-Faders, Already Dead

## Squeezed From Above & Below – Challengers, Fading Foes Fight for Shrinking Share Left

In Figure 9’s centre, labeled “**Challengers, Fading Foes**”, we show the four other surviving enterprise system MPU/system architectures. Each is battling with our three main MPU/system architecture leaders above, and are also fighting each other for the minority share left by the three MPU leaders.

These three leaders have fiercely crushed the four survivors in a pincer movement from above and below. The two IBM high-end enterprise server MPU champions exerted immense pressure downwards, and the burgeoning x64 platform moving upscale has exerted a fierce upwards push. This powerful squeeze caused the four other survivors to lose share. It also sharply compressed the previously wide mid-range server segment, because sharply scale-up x64 ISS systems now address much more of that space today. Main “**Challenger**” is our subject, the Intel® Itanium® MPU-powered HP Integrity platform, which gained share replacing legacy HP platforms.

“**Fading Foes**” are the SPARC partners Sun Microsystems and Fujitsu. Sun withdrew/wrote-off its uncompetitive UltraSPARC IV higher-end server inventory, and sold Fujitsu-built SPARC64 VII-powered, Sun Enterprise-branded, mid-high-end servers through 2008 and 2009. Sun’s own-built, low-end servers using the many-threaded and many-cored UltraSPARC T1 (8 cores by 4 threads), T2, and T2 Plus (both 8 cores by 8 threads) RISC MPUs, optimized for scale-out throughput computing, enjoyed modest success.



But Sun's losses/traumas saw it lose UNIX market share, mainly to IBM, since 2001. Its long-delayed **UltraSPARC RK (Rock)** high-end enterprise server/HPC-targeted MPU is a radical 16-core, dual-threaded, 65 n.m. technology, 396 m.m.2 die size, <2.3GHz frequency design, running in a hot <250 watts Thermal Design Power (*TDP*) thermal envelope, and offering several other MPU innovations (*scout threads & transactional memory amongst them*). RK was promised for delivery in a new range of Sun Supernova enterprise servers in late 2H 2009, after several earlier MPU delays. The RK MPU targets higher per-thread performance, higher floating-point performance, and much greater SMP scalability than the Sun UltraSPARC T1, T2, and T2 Plus (*Niagara/Victoria Falls*) chips. Sun also sells x64 standard servers and blade servers.

How Oracle's April 2009-proposed Sun acquisition will impact this MPU & system strategy is not yet fully clear. Oracle comments suggest it intends to sell integrated stacks of its software on Sun hardware and Solaris. Oracle ownership will dramatically slim the firm, but may increase system customer confidence and slow its steady server market decline. If Sun succeeds in actually getting the RK MPU-powered Supernova systems out this year, it could shake up enterprise server markets with a substantial performance hike, and make Sun/Oracle a stronger **Challenger** again. This would have most impact on HP Integrity sales. Some new form of Sun/Oracle hardware arrangement with Fujitsu now also seems likely.

Also shown under "**Fading Foes**" are the Itanium® MPU-powered HP Integrity NonStop niche fault-tolerant systems that HP offers as hardware replacement to the fading customer base still using proprietary (*ex-Tandem, ex-Compaq*) predecessor NonStop MIPS-RISC powered systems. (*Not considered further here.*)

## Evaluating Current Enterprise Server MPU/System Architectures Leaders/Challenger

We assessed today's Intel® Itanium® 9100 Series Montvale, and next-generation Intel® Itanium® Tukwila MC, MPUs in Section 2, and Montvale's use in today's HP Integrity server family in Section 3. As noted above, their main competitors are IBM's POWER6+-MPU-based IBM Power Systems™ RISC-UNIX servers and System z10™ mainframes, the two dominant enterprise server MPU/system architectures by revenue share, technology, and innovation in recent years. To assess how these IBM platforms compare with current Itanium® 9100 MPU-based HP Integrity systems, we first review their MPUs/system architectures in more depth below:

- **IBM POWER6/POWER6+ RISC MPU/IBM Power Systems™ architecture:** IBM's POWER4, 4+, 5, and 5+, and the groundbreaking POWER6/6+, enterprise server RISC MPUs strongly dominated UNIX markets (*as IBM p Series, System p, and now IBM Power Systems™*) delivering consistently leading performance over the widest span of industry benchmarks, often with best RISC-UNIX price/performance too. These IBM server MPUs also offer the UNIX market's most advanced, mainframe-inspired server virtualization, extensive RAS, and increased power-saving technologies, leading competitors in these vital enterprise server MPU attributes, as well as on performance, since 2001. Higher-end IBM Power Systems™ servers also fully exploited IBM's unique blend of unrivalled MPU design skills, sophisticated MPU packaging, advanced server system architectures, unique IBM chipsets, leading-edge IBM semiconductor process R&D, and advanced 300 n.m. chip fabrication facilities, etc. All based on IBM's Power Architecture™ instruction set architecture, lower-end versions of these MPUs/systems also usually outperform, and now often also compete on price with, Intel/AMD x64 ISS and blade systems. The evolution of the IBM POWER server MPUs with their main distinguishing features, are recapped in Figure 10 (*on page 42*), which also shows the next major IBM roadmap milestone, the POWER7 MPU, due in 2010 and assessed below. This latest IBM POWER roadmap does not show POWER6+ derivatives which featured on several earlier roadmap versions seen in prior years, but see our comments below.

The ultra-high-frequency IBM POWER6 RISC MPU generation, first delivered in June 2007, was widely acknowledged as the **world's fastest, most powerful server MPU to date**, delivering 32.0 GFLOPS sustained. Shipped versions of the 790M transistor, IBM 65 n.m. Silicon-On-Insulator (*SOI*) process-based, dual-core POWER6 ran from 3.5GHz. up to **a highest-ever 5GHz. clock frequency** (*POWER6+ MPUs will run at <6GHz.*), and incorporated IBM Simultaneous Multi-Threading (*SMT*) with two efficient threads per core, giving four threads per chip, within reasonable power envelopes. The now mostly in-order execution POWER6 MPU also incorporated on-chip AltiVec™ Single Instruction Multiple Data (*SIMD*) hardware units on each core, and a **first-ever on-chip Decimal Floating Point (DFP) hardware unit**. Often tagged "money math", DFP is essential for accurate financial calculations/rounding in all financial/commercial applications. POWER6's DFP hardware unit runs such calculations over 10 times faster than the usual software alternatives, and with greater precision.

Each POWER6 core has 4MB of on-die L2 cache, which both cores can access, and each MPU can access an off-die, shared <32MB L3 cache through 80GB/s of L3 cache bandwidth/chip. The POWER6 MPU can be configured with 0, 1, or 2 on-chip L3 cache controllers, and with 1 or 2 on-chip memory controllers, to suit widely-diverse IBM server applications. These MPU options combine with sophisticated packaging options to power IBM's range of POWER6 servers, which now includes two new POWER6+-MPU-based blades. (*Using lower-power MPU options.*)

Packaging includes a high-end, mainframe-like IBM POWER6 Multi-Chip Module (MCM), which houses 4 POWER6 chips and 4 L3 cache chips, in an ultra-dense, very-high-performance, 8-core and 16-thread SMP, multi-layer ceramic MCM, used in the high-end enterprise IBM Power Systems™ 595 server. A cost-effective Dual Chip Module (DCM) houses two POWER6 MPU chips and 2 L3 cache chips for the modular mid-range IBM Power Systems™ 560 and 570 servers, whilst the low-end and blade servers use Single Chip Module (SCM) packages. The specialized, HPC-market-targeted, IBM Power Systems™ 575 ultra-dense cluster node system uses a unique, water-cooled packaging design, squeezing 32-cores into a tiny 2U format unit.

*This POWER6 MPU bandwidth is ~29 times higher than the bus bandwidth of the current Itanium® today's HP Integrity servers.*

POWER6 used a further-improved IBM distributed switch architecture ("Elastic I/O") which scaled up directly with MPU clock frequency, providing an **enormous 305GB/s+ of total chip bandwidth**, (at 5GHz. clock frequency) far higher than any competitor, and a key driver of the many performance victories IBM POWER6 systems have won. This POWER6 MPU bandwidth is ~29 times higher than the bus bandwidth of the current Itanium® 9100 Series (Montvale) MPUs used in today's HP Integrity servers.

POWER6 also provides hardware support for IBM Power Virtual Machine (VM)™ server virtualization, supporting <10 partitions per MPU core, and <254 partitions per system, with live partition mobility that allows running partitions to be moved. Extensive mainframe-inspired RAS capabilities, extending those of early POWER MPUs, are also included, along with dynamic energy management capabilities.

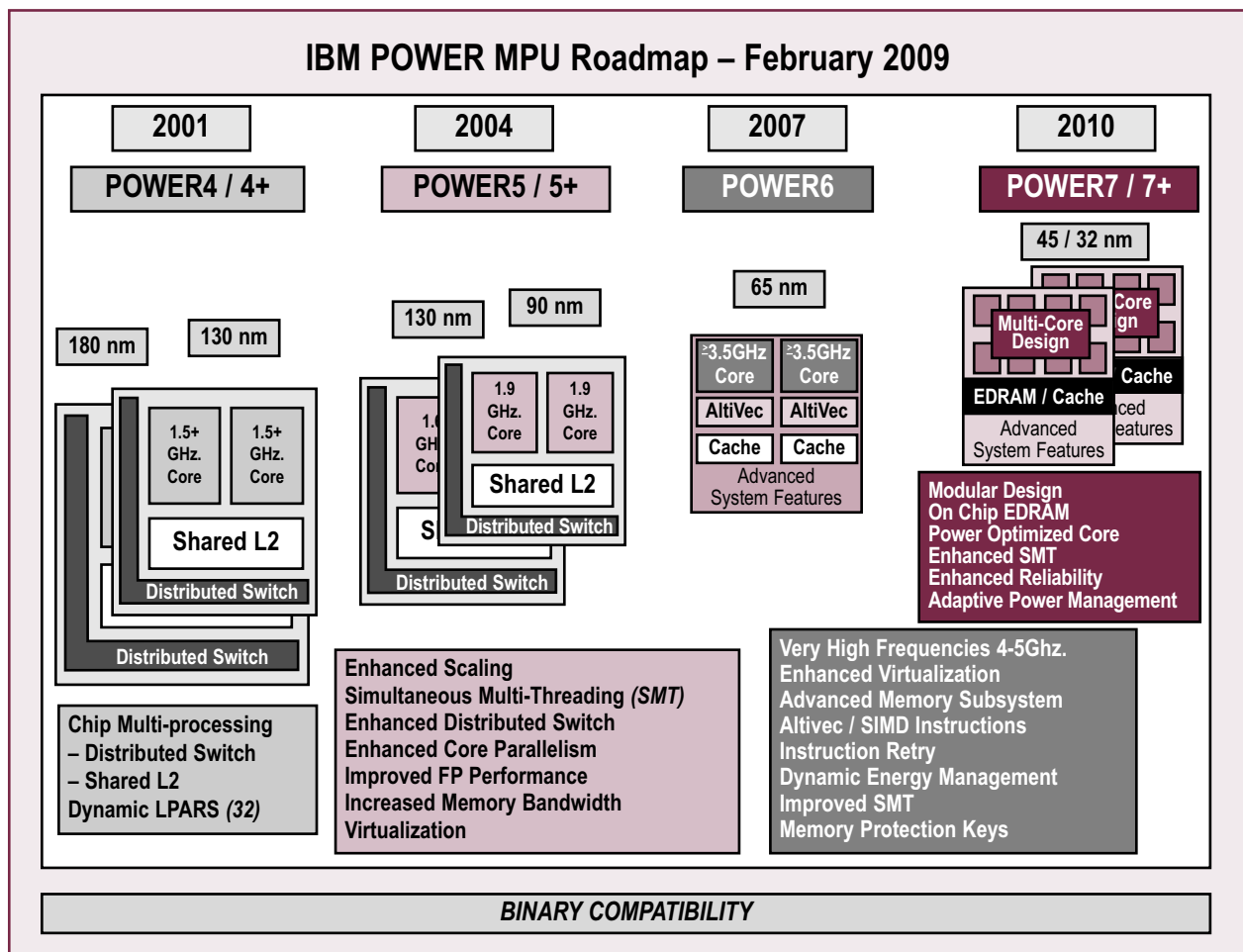


Figure 10: IBM POWER Enterprise Server MPU Roadmap February 2009

- “POWER6+–based” IBM Power Systems™ Kickers Already Shipping – May 2009: With both POWER4 and POWER5, IBM followed each major POWER MPU generation with improved, faster POWER4+ and POWER5+ intermediate generations. Earlier (2006-2007) IBM POWER roadmaps showed a similar POWER6/POWER6+ progression had originally been planned. POWER6, introduced with IBM Power Systems™ servers from June 2007 to mid-2008, was highly-successful and moved IBM far ahead of its competitors (each with delayed next-generation MPUs).

But a later IBM POWER roadmap of Figure 9 (February 2009) showed no POWER6+ step, and IBM has said nothing. However, these enhanced POWER6+ MPUs were actually built and were quietly rolled out. Higher clock frequencies, support for larger memories, increased virtualization capacities for consolidation, and robustness improvements, were the main POWER 6+ MPU improvements. These new MPUs were quietly slipped into the IBM Power Systems™ line-up with the:

- **IBM's October 7<sup>th</sup> 2008 Power™ server announcement**, featuring enhanced Power™ 570 (32-core version using POWER6+ MPUs), Power™ 560 Express (for example, sporting <8 slower 3.6GHz POWER6+ chips, <16 cores, <32 threads, supporting a massive 160 LPAR partitions, and a class-leading 384GB of memory, for consolidation), Power™ 550 Express, Power™ 520 Express, and JS12 blade servers.
- **IBM's April 28<sup>th</sup> 2009 Dynamic Infrastructure announcement** previewed new, strongly-enhanced IBM Power™ servers to ship late-May 2009. These are a new Power™ 550 (with 1-4 5.0GHz. POWER6+ MPUs, 2-8 cores, and 4-16 threads on four SCMs, in 4U format, supporting <80 LPAR partitions, and <256GB memory), a new Power™ 520 (new options with <2 <4.7GHz. POWER6+ MPUs, with <4 cores on 2 SCMs, now also with 32MB L3 cache on the MPU SCM, in 4U format, posting a 26% rPerf performance hike over the prior 4.2GHz. 520 without L3 cache). Also announced was a new JS23 blade server (<2 MPUs, <4-core, using new 4.2GHz. POWER6+ with 32 MB L3 cache, offering 20% more rPerf performance than its JS22 predecessor), and the new double-wide JS43 blade (that clips together two 4-core JS23 blades into one 8 core, 128GB of memory SMP blade able to support up to 80 LPARs of Power VM™ virtualized/consolidated workload per blade).

Indications are that average server performance improvements in the +20-25% range were posted by these POWER6+-enhanced systems over their nearest POWER6 predecessors. IBM could no doubt have rolled-out a new top-end IBM Power Systems™ 595 server, using a top-performing ~6.0GHz. POWER6+ MPU, in the MCM packaging that allows highest POWER MPU frequency, if it so chose. However, with the latest, May 2009-announced, further six month delay in Tukwila MC OEM deliveries now back to Q1 2010, it no longer needs to do so competitively. The current IBM Power Systems™ server range remains amply competitive until well through 2010. The enhanced mid-range IBM Power Systems™ above will still outperform or equal the new HP Integrity, and match Intel® Xeon® EP (Nehalem)-based 2-to-8-socket mid-range systems, particularly in virtualization and consolidation roles, where IBM's larger memory capacities, superior Power VM™ virtualization, and top-performing POWER6+ MPUs will likely continue IBM performance leadership. IBM will then roll out its next, POWER7-based server generation, expected from end-Q1 2010, and which is certain to dominate the UNIX server market on performance over the following two years.

Big Blue switched IBM Power Systems™ marketing emphasis away from its past, mainly performance focus to “performance plus”, the “plus” being the strengths and richness of the platform's innovative capabilities, including virtualization, energy/power management, ITSM, and Cloud computing, where IBM software strengths are ahead of competitors. One example is the recent extension of already UNIX market-leading IBM Power VM™ virtualization, which was first to offer live partition mobility. IBM just (April 29<sup>th</sup> 2009) added industry-first IBM Power VM™ Active Memory Sharing. (This lets memory automatically flow from one LPAR to another, for higher utilization and flexibility by pooling and dynamically redeploying memory to best suit changing LPAR workloads.)

We wrote at this length on IBM POWER6/6+ MPUs here for three important reasons. Firstly, these MPUs power IBM's market-share and performance-leading IBM Power Systems™ RISC-UNIX servers (2007 to date), which current HP Integrity systems (see Section 3) powered by current Itanium® 9100 Series (Montvale) MPUs could rarely match. Secondly, POWER6/6+ MPUs are close siblings to, and shared many aspects (process node and semiconductor technology, logic design, execution units, DFP unit, bus technology, and pipeline design style) with, IBM's blockbuster System z10™ mainframe MPUs, which we review next below. Thirdly, because POWER6/6+ holds the server MPU performance crown, they set high hurdles all challengers must best with their next-generation MPUs, if they want to compete.

- **IBM System z10™ CISC MPU/IBM z/Architecture mainframes:** For its System z10™ mainframes, IBM achieved unprecedented advances with the striking z10 quad-core MPU/z10 system architecture. This delivered far the largest-ever inter-generational advance in MPU (and system) compute-intensive performance/capacity in the platform's 45-year history, boosting it dramatically to highest-ever levels. The ultra-high frequency z10 MPU runs at <4.4GHz. (in the z10 EC) and is the highest clock frequency/fastest CISC server MPU ever built. IBM System z10™ EC high-end mainframes using the z10 MPU first shipped in February 2008, and the mid-range System z10™ BC in October 2008 used 3.5GHz. z10 MPU versions in SCM packaging. (See Figure 1 on page 6 for photos of the z10 EC and z10 BC mainframes.) With the z10 MPU, IBM achieved a **staggering 2.59 times/158% increase in clock frequency** over its 1.7GHz. top-end z9 EC MPU predecessor. The z10 MPU uses a deep, 15-FO4 cycle, superscalar, low-latency, in-order pipeline design (similar to POWER6), and many other advanced techniques, to boost the MPU's clock frequency to these sky-high levels.

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*The z10 MPU is the highest clock frequency/fastest CISC server MPU ever built.*

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The 993M transistor, 8,765 contact, IBM 65 n.m. SOI process-built, single-threading **z10 MPU was also IBM's first-ever quad-core server MPU, providing a 4-way SMP on-a-chip** building-block. Memory controller and I/O controller (GX bus) functionality are now integrated onboard the MPU die, helping reduce the System z10™ EC Central Electronics Complex (CEC) to just 2 main chip types (down from 5 types on the z9 EC CEC).

The IBM z/Architecture CISC ISA for z10 now sports a massive 894 total instructions, 668 implemented entirely in hardware, adding 50+ new instructions for improved code efficiency, others for software/hardware cache optimizations, and to support 1MB page frames. "Extreme CISC ISA" springs to mind! The z10 ISA remains fully backwards-compatible with prior IBM mainframe software architectures all the way back to the original IBM System/360. This prized benefit for long-standing customers enables System z10™ machines to run mixes of earlier software simultaneously.

Extensive z10 MPU on-die hardware supports industry gold-standard System z virtualization, advanced cryptographic support, database compression support, and the same new DFP unit (*Institute of Electrical & Electronics Engineers (IEEE) 754 compliant*) as on POWER6 (*which brings enormous performance gains on money-math*). In addition, this 10<sup>th</sup> generation IBM CMOS mainframe MPU has far the most extensive, sophisticated, long-refined, and further extended, on-chip RAS support of any MPU, by a big margin. In all, IBM incorporated over 20,000 error checkers on the z10 MPU. Error-Correcting Code (ECC) is used on the L2 and L3 caches and on buffers, and extensive parity checking is incorporated elsewhere. Processor core state is buffered such that precise core retry is allowed for almost all hardware errors. These, and scores more, MPU-level, system-level, and software-stack-level RAS features underpin the extraordinarily high RAS levels that System z10™ mainframe servers achieve. Note some close similarities with POWER6 above, but also that the different z10 MPU ISA gave it quite different processor cores. Other major MPU aspects, like cache structure and coherence approach, SMP interconnection topology and protocol, and the chip layout/organization, are also very different on the z10 MPU.

Each z10 MPU core has its own L1 instruction and data caches, plus its own private 3MB on-chip L2 cache, and can access up to two shared 24MB L3 caches (*see next point*). A huge (*1.6B transistor, 7,984 interconnects*) companion SMP Hub Chip provides that 24MB of L3 cache, and provides communication with other z10 MPUs and SMP Hub Chips through 48GB/s ports. Each z10 MPU can share cache across two SMP Hub Chips, providing <48 MB of shared L3 cache per MPU. Total z10 MPU chip bandwidth is 240GB/s, made up of two 48GB/s SMP Hub ports (*for L3 cache and local SMP access*), four 13GB/s memory ports, two 17GB/s I/O ports, and 58GB/s of interconnect fabric bandwidth (*other book/MCM access*), which is **22.6 times the chip bus bandwidth of the top-end Itanium® 9100 (Montvale)** MPU that powers the current HP Integrity Superdome. Little wonder System z10 EC systems far outperform comparably-cored HP Integrity Superdome systems.

Up to four sophisticated IBM multi-layer ceramic MCM packages are used for the z10 EC, one for each "book". Each MCM houses five z10 MPU chips, and two SMP Hub chips, for seven main chips in total per MCM. The MCMs for the top E64 model have 77 PU cores available ( $3*20+1*17$ ), whereas the MCMs for the four other z10 EC models each have 17 available cores. System z10™ usage of these PU cores was discussed in Section 4.

The 4.4GHz. z10 MPU's huge advances gave System z10™ EC servers exceptional MPU performance gains, and an 1.7X overall hike to <30,250 MIPS top-end capacity, with 3X the memory supported (<1,525GB), and a 2.2X I/O throughput increase (*over the z9 EC*). As a result, the System z10™ EC delivered outstanding performance on the increasingly common processor-intensive commercial workloads, as well as on its long-established I/O and data-intensive business transaction and data-serving workload fortes. This huge System z10™ performance advance, plus further substantial price/performance gains, allowed many more workloads (*in the past run on UNIX*) to run superbly well, and more affordably, on System z10™ mainframes, with the lowest TCO per transaction or unit of work when fully loaded.

An important IBM Statement of Direction also pledged Big Blue would deliver new hybrid-processing support on the existing System z10, supporting close-coupled, integrated, attached x64-MPU based, application-specific blades to optimize/boost System z10 data warehousing workloads performance and price/performance. Expected around Q4 2009, this major strategic hybrid processing direction step will be further extended in next-generation "z11" mainframes onwards.

These dramatic MPU/system advances help explain why System z10™ has done so well in the market, adding scores of new wins to the mainframe customer base, and continuing the 20%+ CAGR MIPS capacity growth the mainframe enjoyed since 1997, as new customers, workloads, and market share, were all won away from Sun, HP, Fujitsu, and other competitors' high-end enterprise servers.

- **Intel® Itanium® 9100 Series "Montvale" EPIC/HP Integrity systems** – Fully reviewed in Sections 2 & 3, and now close to replacement by Tukwila MC.

To help readers easily compare, Figure 11 on pages 45-46 summarizes main characteristics of the three current leader, and the four next-generation contending enterprise server MPUs/system architectures due before end-2010. The latter are the IBM POWER7 MPU/IBM Power Systems™, the Intel® Itanium® Tukwila MC MPU/HP Integrity systems, next System "z11" mainframe MPU/systems, each direct successors to the MPUs above, plus the significant Intel® Xeon® EX (*Nehalem-EX*) MPU-based systems. Figure 11 data on the three current MPUs is almost complete, public, and accurate. Of the four future MPUs, much (*but not all*) is known about first-to-arrive Intel® Tukwila MC (*assessed in Section 2*). Basic information on IBM's upcoming blockbuster POWER7, sketched on the IBM POWER MPU roadmap (*in Figure 10 on page 42*) has been published. Considerable details on specifications of the Intel® Xeon® EX (*Nehalem-EX*) MPU have just been announced. But nothing at all has yet been disclosed about IBM's next-generation mainframe MPU. Our surmises/estimates (*marked\**) fill in many of the gaps.

## Main IBM and HP/Intel® Current and Next-Generation Server MPUs

MPU Characteristics	Current Enterprise Server MPU Generation <sup>1</sup>			Next Enterprise Server MPU Generation <sup>2</sup>			
	IBM POWER6 MPU	IBM System z10 MPU	Intel® Itanium® 9100 Series Montvale	Intel® Xeon Nehalem-EX	IBM POWER7 MPU	IBM System “z11” <sup>***</sup> MPU	Intel® Itanium® “Tukwila MC”
MPU Type:	Ultra-High Frequency RISC	Ultra-High Frequency CISC	Low Frequency EPIC ILP	Medium-Frequency CISC	Ultra-High Frequency RISC	Ultra-High Frequency CISC	Medium-Frequency EPIC ILP
Pipeline Design:	Deep, 15-stage, low latency, mostly in-order pipeline	Deep, 14-stage, low latency, mostly in-order pipeline	In-order, VLIW with <6 instructions/cycle	4-issue, superscalar, 16-pipeline stage, out-of-order pipeline	Deep, low latency, in-order pipeline *	Deep, low latency, in-order pipeline*	In-order, VLIW with <6 instructions/cycle
Top-end Servers Powered:	IBM Power Systems™ 595	IBM System z10 EC Mainframe	HP Integrity Superdome, & NonStop	IBM X4 System x Intel® 8-way	IBM Power Systems™ 595, Blue Waters	IBM System “z11” Mainframe	HP Integrity Superdome, & NonStop
First Shipped/To Ship Date:	6.2007	2.2008	11.2007	End 2009	1H 2010	2H 2010*	Q1 2010
Number of Cores On Die:	2 (Dual)	4 (Quad)	2 (Dual)	<8 (Octa)	8 (Octa)	4 (Quad)*	4 (Quad)
Max. MPU Clock Frequency:	<5.0GHz.	<4.4GHz.	1.44-1.66GHz.	<2.75GHz.*	<4.0GHz.	~5.0GHz.*	<2.0GHz.
Instruction Set Architecture/ Microarchitecture:	IBM Power ISA v.2.05	IBM z/Architecture, z10 Gen	Intel® Itanium® ISA EPIC	Intel® 64 (x64) Nehalem	IBM Power ISA v.2.06	IBM z/Architecture “z11” Generation	Intel® Itanium® ISA EPIC
System/MPU Packaging Options:	MCM, DCM, SCM	MCM (EC), SCM (BC)	Cellboard, Mainboard, MPU	Cellboard, MPU	DCM, SCM	MCM (EC), SCM (BC)	Cellboard, MPU
MPU Multithreading Type:	IBM Power SMT V3 – 2 threads	Single-threaded	Intel® MT – 2 thread	Intel® Xeon new SMT – 2 thread*	IBM Power SMT V4 – 4 thread	IBM z SMT V1* – 2 thread	Intel® MT – 2 thread
MPU Threads/Core & /MPU:	2 & 4	1 & 4	2 & 4	2 & 16*	4 & 32	2 & 8*	2 & 8
Single System Scaling:	<32 MPUs, <64 cores, <128 threads	4 MCMs, <20 MPUs, <77 PU cores total, <64 customer PUs	<64 MPUs, <128 cores, <256 threads	<32 MPU, <256 cores, <512 threads*	<32 MPU, <256 cores, <1,024 threads	<4 MCM, ~24 MPUs, ~76 customer cores/ 93 total, ~152 threads*	<64 MPU, <256 cores, 512 threads
No. Of Transistors on Die M:	790M	991M	1,720 M	2,380 M	1,400-1,500M*	1,500-1,600M*	2,046M
Semiconductor Node, Process:	65 n.m. CMOS 11S	65 n.m. CMOS 11S	90 n.m.	45 n.m. P1266	45 n.m. IBM HKMG	45 n.m. IBM HKMG	65 n.m.
MPU Die Size m.m. <sup>2</sup> :	341 m.m. <sup>2</sup>	453.5 m.m. <sup>2</sup>	596 m.m. <sup>2</sup>	NA	NA	NA	700 m.m. <sup>2</sup>
Power Envelope Watts TDP:	100-160 watts TDP	NA	75-104 watts TDP	90-130 watts TDP	<160 watts TDP*	NA	130-170 watts TDP
On Die L2 Cache:	4MB/core	3MB/core	3-12MB/core	256KB/core	4MB/core*	4MB/core*	256K/core
Total L3 Cache:	32MB/ MPU chip Off-die on MCM	24MB-48MB/MPU on SMP Hub Chip	3-12MB/core, <24 MB/chip on die	24MB on-die shared/MPU	64MB/MPU* Off-die	32MB-64MB/MPU on SMP Hub Chip*	6MB/core, <30 MB/chip on die

Continued on next page...

### Main IBM and HP/Intel® Current and Next-Generation Server MPUs

MPU Characteristics	Current Enterprise Server MPU Generation <sup>1</sup>			Next Enterprise Server MPU Generation <sup>2</sup>			
	IBM POWER6 MPU	IBM System z10 MPU	Intel® Itanium® 9100 Series Montvale	Intel® Xeon Nehalem-EX	IBM POWER7 MPU	IBM System “z11” <sup>5</sup> MPU	Intel® Itanium® “Tukwila MC”
MPU Interconnect Type:	IBM Power Distributed Switch, 5 <sup>th</sup> Gen.	IBM z Distributed Switch + SMP Hubs, InfiniBand I/O	Intel® Front Side Bus	4 Intel® QuickPath Interconnect (QPI) Links @ 6.4 GT/s	IBM Power Distributed Switch, 6 <sup>th</sup> Gen, InfiniBand,	IBM z Distributed Switch+ SMP Hubs InfiniBand I/O	4 Intel® (QPI) full-wide & 2 half-wide Links at 4.8 GT/s
System Maximum Memory:	1,024-4,096GB	<1,520GB	<2,048GB	>1,024GB*	>4,096GB*	>1,520GB*	<2,048GB*
System Max. Memory/Core:	64GB	23.75GB	16GB	>4GB*	>16GB*	>23.75GB	32GB*
System MPU to Memory Bandwidth (Peak):	<2,400GB/s 32-MPU	1,040GB/s 20-MPU E64	553.0GB/s 64-MPU	1,632GB/s 32-MPU	NA	NA	NA
System L2 to L3 Cache Bandwidth (Peak):	2,560GB/s	1,920GB/s	On-die	On-die	NA	NA	On-die
System Interconnect & I/O Bandwidth (Peak):	4,800GB/s	1,832GB/s	737.6GB/s	1,632GB/s	NA	NA	NA
Total System Ext. Bandwidth:	9,760GB/s	4,800GB/s	1290.8GB/s excluding L2-L3 b/w	3,264GB/s	NA	NA	NA
MPU-Memory Bandwidth/MPU:	75GB/s	52GB/s	8.64GB/s	51GB/s	NA	NA	34GB/s
MPU to L3 Cache Bandwidth:	80GB/s	96GB/s	38.4GB/s on-die	On die	NA	NA	On die
Interconnect Bandwidth/MPU:	130GB/s						
I/O Bandwidth/MPU:	20GB/s	34GB/s	2.88GB/s	-	NA	NA	-
Total Ext. Bandwidth/MPU:	305GB/s	240GB/s	20.2GB/s	102GB/s	NA	NA	130GB/s
LINPACK HPC Per MPU, Core:	32.0 GFLOPS/chip 16.0 GFLOPS/core	NA NA	11.64 GFLOPS/chip 5.89 GFLOPS/core	NA NA	256 GFLOPS/chip 32 GFLOPS/core	NA NA	40 GFLOPS*/chip 10 GFLOPS*/core
Other Major MPU Chip Features:	Modular chip design AltiVec SIMD units IBM Power VM™ support Power 6 <sup>th</sup> gen. RAS Decimal FP (DFP) unit More power management Water-cooled HPC model	z 10 <sup>th</sup> gen. RAS z virtualization z cryptographics z data compression Decimal FP (DFP) unit HiperDespatch SMP aid	Intel® VT virtualization Intel® MT multithreading Intel® Cache Safe tech. Itanium® gen 6 RAS DBS power mngmt. Core-level lockstep PAC611 socket	Nehalem micro-arch. Intel® VT virtualization Intel® Hyper-Threading Tech. Intel® Turbo-Boost Tech. Machine Check Architecture (MCA) Recovery Modular chip design Cache & core recovery LGA-1567 socket.	IBM Power VM™ Support 4 thread SMT Modular chip design Decimal FP (DFP) unit Power 7 <sup>th</sup> gen. RAS Elastic I/O scaling Optical interconnect*	z 11 <sup>th</sup> gen. RAS z virtualization z cryptographics z data compression 1 <sup>st</sup> z SMT 2-thread Decimal FP (DFP) unit	Intel® VT virtualization Intel® MT multi thread. Intel® Cache Safe Itanium® gen 7 RAS. DBS power mngmt. Core-level lockstep New Itanium® socket

Notes: 1. Current MPU specifications. Mainly published/known, data high accuracy. Newest IBM POWER6+ details not shown.  
 2. Next-generation MPU specifications. Itanium® Tukwila MC much known, IBM POWER7 and Intel® Xeon Nehalem-EX early data only known. IBM System “z11” all our estimates/surmises.  
 3. Entries marked \* = Our estimates/surmises.  
 4. NA= Not available  
 5. IBM POWER6+. Quietly shipping un-announced. MPU details not shown here.  
 6. All bandwidth figures above are peak bandwidths.

Figure 11: Main IBM and HP/Intel Current and Next-generation Server MPUs Compared

## Evaluating Next Generation Enterprise Server MPU/System Architectures Leaders/Challenger

To help large organizations with their selection of, and investment in, enterprise server platforms over the mid-2009 to 2012 period, we must look beyond current server MPU/systems architectures, helpful though those were in explaining the current market share positions and ratings of the platforms covered, to assess their next-generation successors too:

- **Intel® Itanium® Tukwila MC EPIC MPU/HP Integrity systems:** Fully reviewed in Section 2, now again delayed a further six months and so now due to reach OEMs in Q1 2010, and to power new-generation HP Integrity servers succeeding the current line-up reviewed in Section 3.
- **IBM POWER7 RISC MPU/IBM Power Systems™ architecture:** Considerable information is known about IBM's blockbuster new POWER7 RISC server MPU, now finishing its four-year development period, because it, and IBM's Productive, Easy-to-use, Reliable Computing (PERC) HPC system concept, **won Big Blue the \$244M Defense Advanced Research Projects Agency (DARPA) PetaScale project in 2006**. The DARPA PetaScale project's goal was that the winner would build a system **100 times more powerful** than 2006's top-performing HPC/supercomputer system **within 48 months**, using commercially-available MPUs/parts. This new IBM HPC colossus, called **Blue Waters**, is now being built for the National Center for Supercomputing Applications, and is to be installed from early 2010 in the new data center now rising in construction at the University of Illinois. IBM's proposal for this PERC system, and Blue Waters' design, needed much R&D into new chip and interconnect technologies, operating systems, compilers, and programming environments, and is based upon IBM's new POWER7 MPU.

**Blue Waters will be the most powerful computer ever built** when brought fully up to speed. It will use 38,900 POWER7 MPUs, with 311,200 processor cores, to deliver a first-ever **>10 PetaFLOPS aggregate performance**, with a total of 620TB of main memory, filling 100+ racks, and occupying <4,400 sq. ft! A massive 1.30 PetaBytes per second (PB/s) interconnect will link Blue Waters' nodes, and its planned 26PB of storage, backed up by one ExaByte of archival storage. Several indicators suggest advanced, new IBM optical interconnect technologies were created for the POWER7/Blue Waters interconnects.

The IBM POWER7 MPU is **a radical, eight-core, four thread, 32-threads/MPU, ultra-high-frequency behemoth**, built using IBM's high-end 45 n.m. process, to deliver a dramatic 256 GFLOPS per MPU from high-end, ~4.0GHz. clock frequency parts. The cores themselves are expected to be similar to, but refined from, those of POWER6, again using a deep, low-latency, mainly in-order pipeline design, but running at least 20% slower than in POWER6 to keep the thermal envelope down. eDRAM (*embedded DRAM*) will be used for on-die cache on the POWER7 MPU, for wider buses, increased access speeds, and to allow larger cache sizes through its higher density.

- POWER7 is **IBM's first general-purpose, eight-core MPU**, optimized for ultra-high compute performance usage in UNIX servers and for HPC leadership, a radical four-fold increase in the number of cores over POWER6.
- Built with IBM's high-end, 45 n.m. High-K Metal Gate (HKMG) semiconductor process, we expect POWER7 will pack ~1,500M transistors, up from the ~790M on POWER6, accommodating the four-fold increase in cores and other on-die additions.
- POWER7 will also be **IBM's first quad-SMT-threaded server MPU, with 32 threads** per MPU chip, an eight-fold threads/MPU increase over POWER6.
- Quoted LINPACK HPC figures indicate POWER7 delivering twice the HPC performance/core, at 32 GFLOPS/core vs. 16 GFLOPS/core for POWER6, each for top-end parts. Per MPU, POWER7's 256 GFLOPS/chip is ~8 times higher than the POWER6 chip achieved. (*4 times the cores at twice the GFLOPS each.*)
- Some IBM POWER roadmaps indicated overall relative performance of POWER 7 was expected to be ~10-times that of POWER5, and ~5 times that of POWER6, no doubt based on IBM's rPerf UNIX workloads metric.

A standard IBM Power Systems™ POWER7 HPC server (*the IBM Power™ 575's successor*) will be offered in an amazingly dense, 2U rack format node, using 4 POWER7 DCMs to deploy 8 POWER7 MPUs, giving 64-cores and 256 threads within an amazing 2U format. Each 2U unit supports 128GB of memory and produces 2 TeraFLOPS, and up to 32 2U units can be connected into a large cluster with 64 TeraFLOPS of horsepower. Other new servers in the new IBM Power Systems™ server line-up using POWER7 will be revealed at announcement near to their release, expected around end-Q1 2010. These are likely to differ from the POWER6+ family for packaging/optimization reasons. With five to eight times the MPU performance (*depending on workload*) of still-competitive IBM POWER6 MPU-based systems, new POWER7 systems look set to completely blow away all known competitors in MPU and system performance, especially the further-delayed Tukwila MC MPUs in new HP Integrity systems.

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*...POWER7 systems look set to completely blow away all known competitors in MPU and system performance...*

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- **IBM System “z11” CISC MPU/IBM z/Architecture mainframes:** No information at all has yet been disclosed about the next-generation IBM mainframes/MPUs, not even names. We use “System z11” and “z11 MPU” labels merely as logical, but unconfirmed, nametags here. There are good reasons IBM keeps silent up to announcement day. Mainframe sales drop sharply whenever official words on a next generation are spoken, so omerta prevails. Silence also keeps competitors guessing, important with renewed HP mainframe attacks, and likely new Sun/Oracle assaults, ahead. For the 2000 decade, IBM averaged a just over two-year interval between the four main/five total System z mainframe generations built, with variations. High-end systems (*EC*) debut first, with mid-range systems (*BC*) often following some months later. For example, the z10 generation debuted in February (*EC*) and October (*BC*) 2008. Indicators suggest that IBM will keep up this decade’s faster mainframe advance pace that proved so successful for the platform. Because the z10 brought the largest-ever mainframe performance boost, and because of the current recession climate, we expect a slightly longer ~2.5 year interval this time, putting the new high-end “System z11” launch in late-Q3 or early Q4 2010. What will the “z11” MPU offer? Our surmises are:
  - We expect the **“z11” MPU to be mainly be a process node shrink/speed up**, further refining/optimizing (*within similar architectural features*) the z10 MPU, the most logical next step after 2008’s radical z10 chip and z10 system architecture advances.
  - The System “z11” MPU will again share major features (*e.g. DFP*), components, concepts, and its process, with its radical POWER7 sibling detailed above, whilst remaining very different in other areas, optimized specifically for its different mainframe workloads roles.
  - IBM’s 45 n.m. semiconductor process node will be used, as for POWER7 (*confirmed*), bringing a likely transistor count of ~1,500M, up from 991M with this shrink-down from 65 n.m. This gives IBM broad transistor budget scope (*~509M transistors*) to fit in the expected SMT addition below, to extend cache and memory control support, add further new hardware instructions on “z11” cores, further extend already strong RAS, and to extend power management.
  - The “z11” MPU will again be an ultra-high frequency **CISC MPU, we expect running at around ~5GHz**, through further optimization of the again in-order, deep, low-latency, superscalar pipeline design (*refined from that on the z10 MPU*). The clock frequency increase, which scales through the interconnects, may add a 6-10% performance gain.
  - We expect IBM will scale up the maximum number of cores on the “z11”. For example, IBM may use 6 quad-core MPU “z11” chips per MCM to offer perhaps ~76\* customer cores/~93\* total cores, in order to boost Single-System-Image (*SSI*) capacity. (*Customers needing higher System z capacity scaling can use well-proven z/OS® Parallel Sysplex® clustering of <32 System z systems.*)
  - The “z11” MPU will, we expect, retain the quad-core configuration, cache architecture, and SMP Hub connectivity approach pioneered on the z10 MPU, with interconnect bandwidth scaled-up in line with higher frequency, plus other optimizations/enhancements. A low-probability alternative would see IBM jump to an octa-core MPU (*as used in POWER7*). However, we think this more likely to feature on the next-but-one “z12” mainframe generation, sharing this by-then well-proven on POWER7 feature.

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*We do expect that IBM will add a first mainframe multi-threading implementation on the “z11” MPU...*

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- We do expect that IBM will add a first mainframe multi-threading implementation on the “z11” MPU, with IBM SMT-type dual threads per core, of which it now has extensive experience. We expect a top-notch SMT dual-threading implementation to add ~20-30% in performance/core.
- eDRAM will be used for on-die L2 caches on the z11 MPU, for increased bus width, faster access speeds, and to allow larger cache sizes from their higher density (*also used on POWER7*).
- With the shrink to 45 n.m., IBM can probably stay within a similar thermal power envelope as on the z10 EC MPU, again needing hybrid cooling of the MCMs.

We surmise that **this “z11” MPU may provide ~1.25 times\* the capacity of the z10 MPU (~1,150 MIPS per core\*)**, with perhaps ~43,000 MIPS from the top-end, ~76 CP System “z11” EC system. In addition, the “z11” system will add to/extend the hybrid processing support of closely-coupled x64 application processing blades, with central mainframe-hosted virtual machine management across both, that was expected to first debut on the z10 in late 2009. This healthy, further mainframe advance, with expected regular price/performance dividend gains, is thus likely to arrive just fifteen months from our Q2 2009 time of writing. These new systems will ensure further market share gain successes for IBM’s mainframe platform from late 2010 through 2012 against all comers, in a market by then hopefully emerging from recession.

- **New Intel® Xeon® (Nehalem-EX) CISC MPU/high-end x64 servers:** Intel and HP sought to keep Xeon® EX mid- to high-end MPUs in a separate “market box” from Itanium® MPUs. Both support these powerful x64 server MPUs in <8-socket servers only, in order to keep Itanium® alive. But we see other OEM’s top-end x64 Xeon®-EX-based multiprocessor servers providing formidable, direct competition to the next Itanium® Tukwila MC-based HP Integrity systems and their successors (*see below*), so it would be unwise not to consider them more fully here.



The next top-end Xeon® EX MPU, code-named Nehalem-EX, is an impressive <8-core (*octa-core*), single-die x64 CISC MPU, built on the Intel 45 n.m. P1266 (*High-K Metal Gate*) semiconductor process, using the excellent new Intel Nehalem micro-architecture, adding new Intel® Hyper-threading with dual threads per core, and so running 16 threads per chip. The MPU sports a massive 2,350M transistors, uses the Intel 64 (x64) instruction set architecture (ISA), with parts expected to run within a moderate 90-130 watts TDP thermal envelope. The cores support SSE4 extensions. Shipping clock frequencies have not been disclosed, but we expect these will fall in a modest 2.0-2.4GHz.\* range in order to achieve the thermal footprint above. Each two processor cores share an on-die L2 cache, and the whole MPU/all 8 cores share a 24MB on-die L3 cache. The Nehalem micro-architecture used is the most significant major improvement to Intel x64 server chip/system architectures in a decade, and also allows considerable OEM flexibility in configuring specific system solutions.

Nehalem-EX uses Intel scalable memory buffers and scalable memory interconnects, supporting up to 16 memory slots per processor socket.

Quad on-board DDR3 memory controllers each provide <6.4GT/s of memory transfers, and four Intel® Quick Path Interconnect (QPI) Link Controllers each provide <6.4GT/s of inter-MPU transfers. This architecture removes the throttling FSB bottleneck that so drastically constrained chip bandwidth of all pre-Nehalem Intel® Xeon®, and prior Itanium®, multiprocessor server MPUs. **We estimate total Nehalem-EX chip external bandwidth at a healthy 130GB/s\*** (excluding on-die L2 to L2 cache).

Supported by Intel's new Boxboro EX I/O Hub chipset, the Nehalem-EX architecture allows direct glue-less construction of <8 socket, 8 Nehalem-EX MPU, 64-core, 128-thread standard server systems, using four standard Intel Boxboro EX I/O Hub chipset parts. Third-party OEM chipsets will allow larger SMP systems to be built. Another interesting feature of this huge Nehalem-EX MPU is Intel's first use of core and cache recovery. These allow Intel to disable defective cores or caches, so these chips can still be sold as a lower cores, or smaller cache part, crucial to increasing the low chip yields huge MPUs like this typically achieve. Strong Xeon® EX RAS facilities are again built in, and have been extended. Extensive three-zone clock scaling and power management facilities are also included. We also expect Xeon® enterprise server builders IBM, Unisys, & NEC will again offer modular enterprise servers using these Nehalem-EX MPUs, using their own IBM (X4) and NEC (MX5800 or new) scalable chipsets, to provide <32 socket, <256 core, <512 thread\* Xeon® EX enterprise servers. It also now seems likely Fujitsu will join this group, which would deal a further blow to Itanium®.

Pricing has not yet been disclosed. However, the current, top-end Xeon® multiprocessor MPUs costs just over two thirds of the price of a comparable Itanium® MPU, a major source of Xeon® price/performance advantage. For example, the Intel OEM list price for today's Itanium® 9100 (*Montvale*) top-end part is \$3,692, whilst today's top-end Xeon® EX MPU (6-core, 2.66GHz., 16MB L3 cache, "Dunnington" E7640) lists at \$2,729 each, 72% of the Itanium® part price (for trays of 1000 MPUs).

Intel's May 26 2009 press release now indicates Nehalem-EX MPUs are now due to ship from late-2009, with OEM server systems following over Q1 2010. Next-generation HP Integrity systems will now arrive a quarter or more later in Q2 2010, and we fully expect that OEM Xeon® Nehalem-EX-based server competitors will assault them fiercely. (For Linux and Windows workloads.) Intel claims that Nehalem-EX provides the largest-ever jump in Xeon® server MPU performance. 9X the memory bandwidth, 2.5X the database performance, 1.7X the integer throughput, and 2.2X the floating point performance, of the current top end Xeon® EX 7400 are claimed, and look credible given the chip's high specification.

Enterprise servers based on this new Intel 64 ISA, CISC Nehalem-EX MPU also look firmly set to substantially outperform comparable 65 n.m Itanium® Tukwila MC-based HP Integrity systems, especially for database serving and ERP workloads, and should also offer better price/performance. Nehalem-EX MPUs offer twice the number of cores, twice the number of threads, are built on Intel's much-higher higher-performing 45 n.m. HKMG process, have superior Intel Hyper-threading, run at higher clock frequencies, and have all the other Nehalem micro-architecture improvements, compared to Tukwila MC, making it hard to see how the former can compete against its own sibling. Which leads directly to the question as to why continue with Tukwila MC?

## **Integrating Unequalled MPU, Semiconductor, System, & Software Skills, Makes Winning IBM High-end Systems**

Although high-end MPUs are a major determinant of enterprise system performance and capabilities, winning top-end systems must also optimize not only the MPU design, but also the semiconductor process to built it and the chip packaging, blend those with strong system architecture/design, and surround these with firmware, operating systems, and a strong run-time middleware and tools software stack, all tightly-integrated and well-optimized for the platform. IBM has the industry's strongest abilities to optimize and integrate these layers of its system stacks. It has used this approach systematically to great advantage, sharply differentiating both winning lines of high-end enterprise systems from its competitors.

Key elements of this were:

- **IBM STG Unified MPU & System Design Strengths:** Behind IBM's two winning high-enterprise server MPUs and systems are IBM STG's unified MPU and system design/development organization, the world's most experienced and skilled high-end MPU design, packaging, and advanced systems architecture design/development organization. This unified team brought many mainframe-pioneered advances directly into IBM Power Systems™, and other IBM servers, and added lower-cost, standards-based technologies into several IBM platforms, including mainframes, accelerating advances of both of these sharply this decade, whilst reducing costs. HP, in contrast, divested all MPU design/development, and much of its own and acquired system design/development, and OS capabilities, over this decade, and never had any mainframe skills to draw upon.
- **Power Architecture™ and IBM Microelectronics Underpin:** These advanced system-building skills are supported by the in-house IBM Microelectronic semiconductor powerhouse. IBM Power Architecture™, the firm's successful RISC MPU instruction set architecture, is a major underpinning of its system success. With a thriving open Power.org ecosystem and community architecture guidance, Power Architecture™ MPUs today power all of the world's leading games consoles, the largest supercomputers, and hundreds of other embedded MPU and consumer electronics applications, as well as top-performing IBM Power™ RISC-UNIX servers. These other MPU markets provided high chip volumes, supporting IBM's server chip-making ecosystem. For example, IBM has now supplied over 50M custom-designed Power Architecture™ MPU chips to Nintendo alone, powering their highly-successful and market-leading Wii™ games console, from November 2006 launch to early-March 2009. By contrast, HP must rely totally upon Intel/AMD for the standard Intel/AMD MPUs now used in all HP systems, and so can no longer improve MPUs, or the MPU/system interface, directly itself.
- **IBM-led Global Semiconductor Alliance Redefines Chip Industry:** The Power Architecture™ ecosystem, and IBM Microelectronic's semiconductor R&D leadership, are also strongly supported/extended by the successful Common Platform semiconductor manufacturing alliance (*of IBM, Chartered Semiconductor, and Samsung*), plus the associated Joint Development Alliance for semiconductor process advancement (*of IBM, Chartered Semiconductor, Samsung GLOBALFOUNDRIES, Toshiba, Infineon Technologies, FreeScale Semiconductor, and ST Microelectronics*). These important groupings bring major shared R&D benefits, huge scale, extensive fabrication capacity, and know-how sharing, that strongly supports IBM's development of leading-edge chip technology for IBM Systems, and benefits all these partners too. HP exited from their joint Itanium® MPU development partnership with Intel in 2005, shedding its last MPU design team/skills, to complete a final exit from MPU design and manufacture. Main IBM MPU competitor Intel must carry all Itanium® R&D investment and marketing burdens alone, with HP totally reliant on Intel's delivery.
- **IBM Software Group System Synergies:** IBM's SWG, with revenues of \$22.01B (2008) is the world's second largest software business, focused on its extensive portfolio of enterprise middleware and tools software for all major IT platforms, and on supporting the firm's own operating systems. IBM made over 50 ISV acquisitions over the last decade to radically expand this highly-successful, profitable system software business that leads the market in many middleware segments. Over this 2000 decade, IBM SWG maintained highest rates/levels of advance in OS, middleware, and tools software optimized for the IBM System z10™ mainframe (45% of IBM SWG revenue) and for top-performing IBM Power Systems™ servers. By contrast, HP's software business is barely a seventh the size of IBM's, and so adds correspondingly far lower value atop HP Integrity server systems.
- **Integrated, Optimized, Fully Architected Systems Model Wins:** With high-end System z10™ mainframes and IBM Power Systems™ especially, IBM fully exploited its strong R&D innovation rate, mastery of, and control over, all layers of the platform stacks above. This allowed IBM to attain tighter integration between the layers, implement multiple levels of optimization across the layers, introduce more innovation, achieve higher-performance, and add unique QoS characteristics, with IBM as the single supplier taking full responsibility for the combined, integrated hardware/software platforms. This means much less integration work, better performance, better QoS, and more differentiated systems, for IBM customers. We say the notable market success and share gains these advanced IBM systems made through this decade proves that this model works best for enterprise systems.

Oracle recently stated that it also plans to adopt a similar vertically-integrated, optimized stack-based business model for its planned Sun-acquired hardware, and extensive software portfolio combinations, after the Oracle/Sun deal closes.

By contrast, HP and Dell Computer rely on the "horizontal" system-building model, assembling (*or contracting assembly*) of standardized design PCs, notebooks, ISS servers, storage, and printers, etc., from bought-in components provided by leading horizontal specialist parts makers, including Intel and AMD (*MPUs*), Microsoft (*OS and middleware*), VMware (*virtualization*), Canon (*laser engines*), SAP (*ERP software*) and many others. Whilst this incurs lowest vendor R&D costs, limited innovation is the result, margins are thin, and commodity-pricing-based considerations are foremost. Done well, this model can succeed for the simplest, highest-volume, most commodity-like IT products such as PCs, notebooks, and printers, etc., but we conclude that it fails for serious enterprise systems platforms above basic ISS servers, because much deeper integration/optimization and real innovation is vital for these.

## Our Analysis

Summing up our findings, based on our analysis of the current and next-generation enterprise server MPUs above, we conclude:

- **Tukwila MC a Big Itanium® Improvement:** Tukwila MC, with quad cores, dual threads, the new QPI interconnect, and still large on-die cache (*although L3 cache is down from the generous 12MB/core of Montvale to 6MB/core on Tukwila MC*) will bring substantial bandwidth and performance advances to new HP Integrity systems when these finally ship around their further six months-delayed, now Q2 2010 expected debut, providing a doubling (*or more*) of performance over (*feeble*) Montvale predecessors, and at last removing the notorious Itanium® bottleneck of the antique FSB.
- **IBM POWER6+-based Systems Remain Ahead:** Based on our assessment of IBM POWER6/6+ MPUs above, we expect the performance of the newer IBM Power Systems™ will keep them ahead of new Tukwila MC-powered HP Integrity systems on most workload benchmarks, measured per core, until IBM POWER7-based servers arrive.
- **System z10™ MPU and System Success Explained:** The huge performance and capability jump of the IBM System z10™ MPU, heavily leveraging POWER6 innovation, drove System z10™ EC systems to a new high-point of performance, as well as extending their advanced, highly-differentiated RAS and QoS capabilities. These factors explain their market success, and the substantial all-round enterprise system superiority they hold today over contemporary HP Integrity systems. System z10 EC mainframes will thus now remain far ahead of the current HP Integrity Superdome in performance and capability until at least Q2 2010. (*Discussed in Section 4 and Section 6.*)
- **Expect HP Benchmark & FUD Barrage:** Now arriving two-and-a-half years after the late-2007 and relatively minor last HP Integrity refresh (*Montvale*), and with at least two years before the mooted next Itanium® Poulson MPU generation, HP and Intel will make the maximum noise about new Tukwila MC-based HP Integrity systems when they finally launch. Enterprise users can expect a torrent of HP/Intel claims, benchmarks, more hoopla and Itanium® FUD, from the time these new HP systems are announced ~Q2 2010. However much of their thunder will have already been stolen by the quarter earlier release of Nehalem-EX-PU-based enterprise servers from other vendors. In the light of this Paper's findings, and the duo's past record, we advise enterprise users to treat all this with great caution and extreme skepticism. Because:  

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*...new POWER7 RISC MPU-based IBM Power Systems™ will also absolutely blow away new Tukwila MC-based HP Integrity systems by a wide country mile...*

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- **POWER7 Will Blow New Itanium® Away in Early 2010:** By our assessment above, IBM's storming new POWER7 RISC MPU-based IBM Power Systems™ will also absolutely blow away new Tukwila MC-based HP Integrity systems by a wide country mile, when these ship from around end-Q1 2010\*. POWER7 is now far advanced in final development, with the new chips running validation in IBM labs now, their breakthrough performance above assured by Blue Waters/DARPA contract terms. We assess the new HP Integrity systems will be deeply uncompetitive with POWER7-based IBM Power Systems™.
- **New System "z11" Mainframe in Late 2010, Will Also Stride Ahead:** We also forecast that a next-generation IBM System z MPU (*tagged "z11" for short here*) will be a substantial refresh/shrink of the current z10 MPU, adding ~40-45% to MPU level capacity from the expected addition of SMT dual-threading, a frequency increase, the 45 n.m node shrinkage, and other improvements. New System "z11" EC high-end systems can be expected around end-Q3 2010 on past IBM mainframe lifecycles, and will further extend System z mainframe leadership for the following two years or more through 2012.
- **Intel® Xeon®-based Enterprise Servers Out-price/Out-perform Tukwila MC Systems, Say Unisys:** Despite Tukwila MC's improvements (*see Section 3*), according to high-end Intel systems expert Unisys, new Itanium®-based systems will not beat high-end Intel® Xeon® EX-based systems already shipping today, for database and application serving and BI, on price/performance, undercutting Itanium® options by some 40% on 3-year TCO. The next-generation, Nehalem micro-architecture-based, high-end <8 core Xeon® EX MPU (*Nehalem-EX*) now due to ship late 2010, will pull even further ahead of Tukwila MC systems, on both price/performance but also on absolute performance, as can be seen above and from our Figure 11 data. High-end x64 enterprise servers using this Nehalem-EX MPU will provide formidable competition to HP Integrity, as will high-performing Xeon® 5500 standard servers in the lower-mid-ranges, for all Linux and Windows workloads.
- **Sun/Oracle, Sun Systems, Rock = Heavy HP Impact:** Oracle's bid for Sun Microsystems now looks sure to complete. Oracle said it intends to continue Sun's servers/Solaris system business, whilst absorbing its software interests, and doubtless slashing staff/costs. Oracle stated it would optimize/integrate hardware and software "from the disk upwards" to work well together, reducing Oracle/Sun customer integration efforts. If seen to be done post-acquisition, weak current confidence amongst Sun server/Solaris users might lift.

Sun/Oracle may also succeed in bringing new Sun Supernova (*UltraSPARC RK MPU-based*) servers to market late in 2009 as promised. This may give Oracle/Sun a competitive high-end UNIX server offering at last, with HP Integrity certain to be the main loser. HP's long-held close ties with Oracle as a leading ISV will likely weaken. HP also supplies the HP Oracle Database Machine, and the HP Oracle Exadata Storage Server hardware systems that Oracle sells. It seems unlikely these deals could continue for long with Oracle running Sun's server business. The triple whammy of stronger Oracle/Sun server competition, this major partner becoming a direct system competitor, and loss of current hardware OEM business, are direct blows HP will suffer here.

New HP Integrity systems using new Intel® Itanium® Tukwila MC MPUs will finally bring a much-needed, although belated, substantial performance boost over the current, far-lagging HP Integrity systems using Intel® Itanium® 9100 Series MPUs. Our comparative assessment of main MPU competitors above found these HP/Intel gains will be insufficient. Whilst HP will enjoy a pent-up orders backlog, and a relatively more competitive Integrity line, these platform advances are insufficient against refreshed IBM Power™ (*POWER6+*), and deep System z10™ mainframe competitive strengths. These new HP Integrity systems will also be far behind again when the leapfrogging, next-generation, IBM POWER7-based systems (*end-Q1 2010*) and new System “z11” mainframes (*late 2010*) ship and pull far/well ahead. x64 Nehalem-EX based enterprise servers will provide formidable competition.

HP must thus battle such a strongly-placed IBM, at the same time as the easier business of replacing its own legacy platforms with HP Integrity nears completion, in the teeth of a deep recession. HP also faces tough new Xeon®-based x64 enterprise server competition, and likely much stronger Sun/Oracle competition as well. New HP Integrity sales will thus be much harder to find through 2009-2012.

The next Itanium® Poulson-MPU-based generation now appears to offer the HP-Intel duo what we assess to be their final chance to deliver a fully-competitive specification and performance Itanium® MPU, but indications suggest this is likely to arrive too late.

## 6. HP Integrity Superdome Versus IBM System z10™ EC Compared

### Introduction

In Sections 2 to 5 we examined and assessed the Intel® Itanium® MPUs (*Section 2*), HP's Integrity enterprise servers (*Section 3*), IBM's System z10™ mainframes (*Section 4*), and the market's main contending current and next-generation enterprise server MPU/system architectures (*Section 5*). In this Section 6, we draw together our assessments, and summarize comparisons between IBM's System z10™ mainframes and HP Integrity Superdome enterprise servers. Because a new generation of Itanium® MPUs, and thus of HP Integrity servers, are due in Q2 2010, our comparisons below assess both the current (*Itanium® 9100*) and the next (*Itanium® Tukwila MC-based*) HP Integrity generations expected. In addition, although IBM's System z10™ mainframes are unlikely to be replaced until Q3 2010 or later, and no official information has been released on future mainframes or their MPU's, our comparisons include our surmises/estimates\* covering next-generation (*unnamed*) System “z11” mainframes and “z11” MPUs. Except where specifically stated otherwise, HP Integrity references below are to HP Integrity Superdome high-end servers. Also, unless otherwise stated, System z10™ or “z11” in this Section refer to System z10™ EC or System “z11 EC” high-end mainframes.

### Our Ratings Explained

To broadly compare these complex, large-scale systems, we use relative ratings within this market segment. These most clearly show the areas of closest similarities and widest differences between these complex, high-end platforms. The rating scale used, and its graphic representation, is:

Much strongest capability =	██████████	██████████	██████████	██████████	██████████
Strong capability =	██████████	██████████	██████████	██████████	
Average capability =	██████████	██████████	██████████		
Some/limited capability =	██████████	██████████			
Weakest capability =	██████████				
No capability offered =	██████████				

This approach allows readers to absorb the ratings “at a glance”, with longer black bars denoting higher ratings. The following subsections display our relative summary assessments of the two families, and two generations, of these competing high-end mainframes and enterprise servers, for what we assess are the fourteen most important, differentiating comparison factors. We excluded here several factors where competing systems are closer to each other's capabilities as less interesting. For example, server physical dimensions, weights, and operating conditions, are not vastly dissimilar, so were not covered. Footnotes indicate sources within this White Paper used to reach ratings shown.

A challenge for several of the major differentiating factors covered, was that full detail comparison, explanation, and assessment of all the features and functions these complex, large systems offered in that area could alone fill an entire White Paper of this size. We focused on providing a higher-level, summary picture over the major enterprise platform differentiating selection factors.

## A. MPU Capability, ISA, Interconnect, Bandwidth, & MPU-level Performance

Our composite overall rating of the MPUs powering these high-end enterprise systems, considering their number of cores, number of threads, clock frequency, breadth and power of instruction set (ISA), the range and power of on-chip functions, the strength and capacity of the chip's interconnect, overall MPU bandwidths, and broad MPU performance for target workloads. Such on-chip capabilities are the base foundation for enterprise server capability and performance. Over time, more and more system functionality has migrated onto the MPU, with transistor counts for these four contenders now in the colossal 990M to 2,046M range. The current z10 EC MPU was by far the most radical and substantial advance in frequency, capability, and performance ever seen in mainframe history, a real IBM MPU tour de force using many sibling POWER6 elements. By contrast, current Itanium® 9100 (*Montvale*) processors powering current HP Integrity systems since late 1997 were the dampest squib, and the most minor advance, amongst Itanium® generations to date.

A. MPU Capability, ISA, Interconnect, Bandwidth, & MPU-Level Performance:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"™*	"z11" MPU*					
HP Integrity*	Tukwila MC					

Sources: Deeply analysed in Sections 2 & 5, Figure 11, Figure C1

The result is that Intel® Itanium® 9100 Series MPUs powering current HP Integrity servers are heavily outclassed by current IBM System z10™ EC mainframe MPUs (*and by the POWER6+ MPUs used in IBM Power™ RISC-UNIX systems*). This wide, current gap will be narrowed (*but not closed*) by the Tukwila MC MPU-based HP Integrity systems, now further delayed until the new, end-Q1 2010 launch. We expect late 2010-on delivery new System "z11" mainframes will re-extend System z MPU leadership with a substantial further performance hike.

## B. MPU Packaging, System Architecture, Chipset, Bandwidth & System-level Performance

With the long-term, continuing industry pattern of previously separate system architecture elements and functions moving onto the MPU die into ever-denser silicon, achieving optimized system performance and QoS today requires ever-closer integration across, and optimization between, the MPU, the server chipset, the packaging technology, the virtualization firmware, the OS, and the rest of the system hardware.

Our composite overall rating of the quality, strength, and performance potential of these high-end enterprise system's MPU packaging used, the system design and architecture adopted, the server chipset used, the system's interconnection topology, and overall system bandwidths (*cache, memory, I/O, and total system*). These factors provide the system foundations, when combined with the MPU attributes in A above, for a server's overall performance, rated under factor D below.

B. MPU Packaging, System Architecture, Chipset, Bandwidth & System Level Performance:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"™*	"z11" MPU*					
HP Integrity*	Tukwila MC					

Sources: Deeply analysed in Sections 2, 3, 4, 5, Figure 11, Figure C2

The IBM System z10™ EC mainframe is in a different league, using much more sophisticated MPU packaging, a clever new fully interconnected system architecture, implemented with IBM's huge new SMP Hub chip, combining with the MPUs to provide a much stronger interconnect, with far higher total chip and system bandwidths than HP Integrity Superdome systems. We expect similar, sound, but relatively unsophisticated, system design/construction will again be used in the next HP Integrity Superdome generation, albeit with substantial bandwidth improvements from the new Tukwila MC MPU, as per Section 2.

## C. Heterogeneous Processing – Specialty and Dedicated Processors, Hybrid Processing Support

Many diverse workloads and different types of processing are needed in the wide spectrum of enterprise commercial computing. Some important classes of these may sometimes best be run on processors specifically optimized for those tasks, not on relatively higher-cost, general-purpose enterprise server MPUs, whose design is always a compromise. Such processor optimization/specialization brings improved performance, lower processing costs, or a combination of both. Heterogeneous processing systems combine several different types of processors on-board, closely-coupled to achieve better overall performance, interconnection, economics, and manageability, within a single system frame. Loosely-coupled external co-processing systems have also long provided multi-platform, heterogeneous computing, often linked in multi-tier applications. Such off-board co-processing systems can be general-purpose systems (*commonplace*) or specialized systems (*appliances, graphics, etc. – a newer approach*).

IBM System z10™ mainframes today, and “z11” tomorrow, already extensively embed, exploit, and support on-board, closely-coupled heterogeneous processing, with a strong range of specialty processors offered, standard use of dedicated-function processors (*SAPs, spares, and channel-embedded MPUs, etc.*) and integrated on-board accelerator cards (*cryptographic co-processing*). System z10™ mainframes now also support loosely-coupled, highly workload-complementary, specialized external IBM high-performance co-processing systems (*DataPower SOA appliances, and IBM Cell Broadband Engine-based graphics optimized server blades, etc.*). These provide magnitude-higher performance/lower cost processing for such specific tasks, well integrated with System z10™ via IBM middleware software/tools.

C. Heterogeneous Processing – Specialty and Dedicated Processors, Hybrid Processing Support:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Discussed in Sections 3, 4, & 5						

HP Integrity Superdome systems, in contrast, are homogeneous processing systems, in which only standard Intel® Itanium® main processors are used onboard to process all types of workloads, tasks, and services, inevitably a compromise for many of these roles. Only additional dedicated system management processors are used. Naturally, both System z mainframes and HP Integrity Superdome systems can both equally be, and frequently are, loosely-coupled with other general-purpose co-processing systems, which can be IBM (*Power™ Systems, System x, BladeCenter*), HP (*ProLiant, BladeSystem*), or systems from other vendors. System z10™ mainframes are, for example, now frequently used as the enterprise data-serving, transaction processing, and now often SOA, hub platform, that supports and co-processes many other mid-tier application serving and other systems enterprise-wide.

## D. Single-System Scalability, Capacity, & Overall Workloads Throughput

Broadly a function of the power/capacity of individual MPUs and cores used (*A above*), multiplied by the number of CPU/cores supported in the largest single-system offered, the efficiency of SMP scaling achieved with the system architecture and interconnect technology used (*B above*), the capacity/performance contributions made by heterogeneous processing resources on-board (*C above*), and the ability of the operating system to efficiently manage and exploit those resources. IBM provides accurate and reliable mainframe-relative performance tables (*the LSPR*) rating/comparing each System z10™ model with prior mainframe models on several typical modern mainframe workload mixes. Big Blue also provides a similarly useful metric for modern UNIX workloads for its IBM Power Systems™ RISC-UNIX servers, named rPerf. These provide helpful, accurate system capacity planning and sizing guidance for users of both IBM platforms.

D. Single-System Scalability, Capacity & Overall Workloads Throughput:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3, 4, & 5, Figure 10, Figure C2						

Standard public benchmarks are never run for System z10™ or prior mainframe platforms. However, IBM's close System z10™ EC MPU siblings, the POWER6 MPU-based IBM Power Systems™ family, hold a huge range of top public benchmark results, most considerably outperforming HP Integrity systems. (See Sources 22 and 23, page 76.)

Actual sizing studies performed for real customer large commercial workloads typically show up to four current top-end HP Superdome servers are usually required to equal one top-end System z10™ EC, when each are configured to provide similar high QoS and availability levels. System z10™ users regularly run smoothly at much higher utilization rates, frequently up to a 90-95% level, whereas 40-45% is the normal best achieved on large, partitioned UNIX servers like the HP Integrity Superdome. Much larger I/O capacity, excellent batch throughput, efficient Online Transaction Processing (OLTP), and this high utilization, enable a single System z10™ EC to handle workloads needing 2.5-4.0 current HP top-end Integrity Superdome systems. Many large enterprise customers process between 2.5-5.0B real-world commercial transactions per day through a single, top-end System z10™ EC machine, which also frequently support 10,000+ enrolled user populations each.

## E. Clustered System Scalability, Capacity, Manageability, Resilience, & Workloads Throughput

For higher scalability, higher availability, and DR/BC, enterprise system clustering plays a crucial role in adding further scale beyond largest single-systems, in delivering still-higher availability levels, providing enhanced protection against disasters, and in ensuring higher business service continuity. Clustering software technology, cluster coupling, cluster management software, and cluster failover for resilience and DR/BC, are vital enterprise server platform capabilities, that must work in concert with advanced storage replication.

**IBM z/OS® Parallel Sysplex®**, first introduced in 1994 and continuously refined/extended for 15 years since, is the most advanced, refined and manageable enterprise full-system commercial cluster environment, operating near-transparently to users, networks, applications, and IT operations. IBM z/OS® Parallel Sysplex® combines parallel processing and read/write data sharing across multiple systems with full data integrity. Up to 32 z/OS® mainframes can be interconnected in a z/OS® Parallel Sysplex® cluster, can be readily managed as one single-image system from a Single Point Of Control (SPOC), offering huge scalability. A top cluster of 32 z/OS® systems, with <2,048 CP processors, can reach ~ 1B MIPS of capacity. All major IBM mainframe software subsystems (DB2, CICS, IMS, and Resource Access Control Facility (RACF), etc.) have also been deeply adapted to run well on, to scale, and to be manageable, under z/OS® Parallel Sysplex®, and highly-favorable IBM software pricing metrics are offered for these clusters. Other System z OSs can be run on LPARS or z/VM virtual servers on systems also hosting a Parallel Sysplex®. IBM's GDPS® (Geographically Dispersed Parallel Sysplex®) end-to-end application availability solution service extends and automates Parallel Sysplex® tasks, manages remote copy and storage subsystems, can support two and three-site configurations, and enables DR/BC failure recovery from a single point of control. Parallel Sysplex® has long offered the facilities of a large-capacity, hugely-scalable Cloud Computing environment, with a System z10™ EC well cast as the enterprise-wide Dynamic Infrastructure hub.

E. Clustered System Scalability, Capacity, Manageability, Resilience, And Workloads Throughput:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"*	"z11" MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 and 4						

For HP Integrity, diverse clustering solutions are offered, according to the HP Integrity operating system/environment concerned. HP OpenVMS inherits extensive, excellent clustering capabilities as successor to the renowned VMS VAX Cluster heritage, still used by VAX software legacy users on HP Integrity hardware. Windows Server 2008 for Itanium®-based Systems supports like-OS HP Integrity clusters of up to eight nodes, offering Microsoft Cluster Server (MSCS) failover clustering support for high-availability, business-critical Windows workloads only. For HP Integrity under Linux, HP currently still offers HP Serviceguard for Linux HA clustering, but has announced discontinuance beyond its last A11.19 release, with EOS on 10.31.2009. Standard Red Hat and SUSE Linux enterprise version HA clustering support will then provide all Linux cluster support on HP Integrity platforms. **HP Serviceguard Solutions for HA & DR** provide the main HP clustering support for the mainstream HP-UX 11i v3 OEs, with A11.19 the latest release. The software, and most related tools, come inclusively within the HP-UX HA OE and HP-UX DC OE bundled operating environments. A quite broad range of HP and partner clustering applications, and DR/BC options, are therefore offered here.

## F. Range, Granularity, and Flexibility of Capacity On Demand Offerings

Enterprise server customers today rightly expect to be able to increase and/or adjust their server capacity for planned growth, to cover workload peaks, to handle special events, and to provide capacity cover for disasters, without having to pre-buy spare “white space” capacity far in excess of average needs. For CoD, vendors ship the enterprise server more heavily (*or fully*) populated with resources (*MPUs, memory, and I/O*) than the customer initially purchased, and provides mechanisms/options to allow these to be deployed for/by customer use.

Built-in CoD facilities were first seen on IBM’s S/390 G5 mainframe in the late 1990s, and were greatly-extended and refined on System z this decade. Each vendor uses different names and terms for their CoD offering, but the main types are permanent CoD upgrades, temporary or On/Off CoD, backup CoD for use only in DR situations, special event CoD for short-planned period usage, and metered resource CoD usage. Processor capacity is the main CoD resource offered, but memory is also offered on some options, and I/O resources have also been offered.

IBM System z offers all the above except metered pay-per-use CoD. A new Capacity for Planned Events (*CPE*) CoD option, and more flexible new JIT, customer-initiated upgrade flexibility, with automated provisioning software support, was added with the latest System z10™ EC generation. These facilities now extend not only to standard CPs, but also to ICFs, IFLs, zIIP, and zAAP processors. CBU also covers memory. A number of different Temporary On/Off CoD scenarios can now also be set up on these mainframes, and invoked when required.

With System z10™, automated control of installed On/Off CoD temporary capacity can be implemented with **z/OS® MVS™ Capacity Provisioning**, working to customer-defined rules on when and how much extra capacity can be used. These can be according to application, maximum increases, times, and workload conditions, providing rapid, automatic provisioning of capacity where needed under the rules the user defined.

F. Range, Granularity, and Flexibility of Capacity Upon Demand Offerings:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”™*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5						

UNIX enterprise server vendors, including IBM and HP, followed the IBM mainframe’s lead, by steadily adding CoD facilities to their mid-high-end enterprise servers over recent years. HP cell-based Integrity systems, including the Superdome, support HP Instant Capacity (*iCAP*) which over-populates a new customer system with extra cell-boards, processors, and/or memory, beyond the purchased capacities. iCAP hardware is part prepaid (25%) up front. When the customer switches on iCAP hardware with a code, the price balance (75%) becomes payable. Prepaid HP Temporary Instant Capacity (*TiCAP*) provides for 30 days of temporary processor core usage, along with the needed HP software license rights, which customers can use at will, and replenish when fully depleted. HP Pay Per Use (*PPU*) offers a metered capacity usage model for processor core capacity usage. These capabilities operate in conjunction with the HP Virtual Server Environment (*VSE*).

IBM System z10™ remains ahead of the HP Integrity Superdome in the range and flexibility of the CoD options and facilities offerings.

## G. Range, Quality, Functionality, and Advance Rates, of Operating Systems Supported

Enterprise operating systems, with their upper layers of extended services that provide complete operating environments, are hugely important components of any enterprise system platform; as important as the hardware itself. Our contending System z 10 EC and HP Integrity Superdome enterprise platforms currently support five and four operating system families respectively, these being:

- **System z10™:** z/OS®, z/VM, Linux (*two major enterprise distributions*), z/VSE, z/TPF-TPF.
- **HP Integrity:** HP-UX i11, Linux (*two major enterprise distributions*), OpenVMS, Windows Server 2008 for Itanium®-based Systems.

For System z10™, it is creditworthy that IBM continued to support/develop modern z/VSE and z/TPF versions of these specialized low-end business, and high-volume OLTP, mainframe operating systems under z/Architecture throughout this decade, preserving those customer groups’ investments.



z/OS® is IBM's main, rock-solid, industrial-strength, richly-functional production OS for System z10™ mainframes, which has continued to benefit from extremely strong IBM development advances, with major releases now issued each September. (*V1.11 due in September 2009.*) z/OS® can only be described as in vibrant health with bounding functional, feature, performance, etc., advances delivered yearly. z/VM is IBM's impressive extreme hypervisor, enhanced and refined from decades of earlier VM experience, providing many of the mainframe's uniquely flexible, granular, and manageable virtualization capabilities, and supporting into the thousands of virtual servers per system. z/VM benefited from major releases bi-yearly this decade (*V5.4 current*). Linux on System z has been a huge success, with some 2,000 mainframes to date now running Linux, and bringing the open source software world to the mainframe. Red Hat Enterprise Linux (*RHEL*) and Novell SUSE Linux Enterprise Server (*SLES*) distributions are offered. Linux has brought these flexible, modern, UNIX-like environments to System z, and now supports a wide portfolio of modern LOB applications, most popular modern middleware and tools (*including over 120 IBM software products on System z Linux*), and much open source software. It also enables mass-consolidation of workloads from x86, x64, and UNIX scale-out distributed servers (*under z/VM*). Ultra-low-cost IFL Linux specialty processors provide System z hardware quality for Linux workloads at a small fraction of normal CP costs, a major success-factor for Linux on System z. A third-party OpenSolaris for System z under z/VM port is also in progress.

G. Range, Quality, Functionality, And Advance Rates, of Operating Systems Supported:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"*	"z11" MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5						

To its credit, since 2005 HP has offered the capable VAX-legacy OpenVMS operating system on HP Integrity, after a lengthy porting effort, providing software platform continuity for OpenVMS users on HP Integrity hardware, with a reasonable roadmap ahead. A specialized, limited role, many-functions-removed, high-end Microsoft Windows Server 2008 for Itanium®-based Systems version offers a top-end-featured HP Integrity Windows environment, designed to run only data serving (*SQL Server*), LOB custom applications, and ERP packages, and is not widely used. Itanium® RHEL and SLES enterprise Linux versions for HP Integrity provide the main modern alternatives to HP-UX below, for classic Linux scale-up SMP workloads and software, but generally underperform HP-UX because they have not been as fully optimized for Integrity hardware as HP-UX. HP-UX 11i is HP's main, flagship UNIX operating system environment for HP Integrity, and is a solid, capable, enterprise UNIX, bundled into four OE versions with much of HP's (*considerable*) supporting solutions and tools software inclusively packaged. Major HP-UX releases have been infrequent at 3- to 4-year intervals (*v2 2003, v3 2007, v4 2010*), and are considered to have fallen behind IBM AIX (*much-accelerated*) and Sun Solaris (*steady*) in their rate of advance and functional additions this decade. (*Source 24, page 76.*) This was primarily because of the large efforts HP made to port, rewrite, and optimize a new code-track of HP-UX, and much supporting OE software, for HP Integrity/Itanium® Architecture hardware in the 1999-2004 period, whilst also still supporting HP-UX on PA-RISC-powered HP 9000s in parallel for half a decade plus. So where HP's UNIX competitors forged ahead with new functions and capabilities, much HP-UX effort went into this porting, and two parallel OS versions support, efforts. HP-UX staff resources were also sharply cut after that porting effort was completed. HP's new functionality development efforts are now exclusively centered on the HP-UX Itanium® Architecture code-track. A HP-UX 11i v3 Upgrade 4 minor release was recently announced in April 2009, and v4 is scheduled for 2010 on current HP roadmaps.

Readers should bear in mind that a number of the system capability areas reviewed in this Section 6 are operating system dependent/specific. In general, IBM z/OS® and HP-UX 11i support the fullest and most extensive range. Just as a example, OpenVMS on HP Integrity can only support up to 16 processors/32 cores per image, whereas HP Integrity Superdome systems can support images of up to 64 processors/128 cores.

## H. System Virtualization, Partitioning, Workload Management, and System Utilization

Virtualization today is a central IT foundation technology, the best enabling a far more efficient sharing of an enterprise's installed system resources and capacity over their many applications and workloads, and over their business schedules and calendars, as well as sharply reducing costs. All types of IT resource types can, in principal, be virtualized. Server partitioning, dividing a server's resources into multiple, isolated virtual servers (*machines or images*), each running separate workloads (*and often operating systems*), is the most common virtualization approach. Dynamic partitioning, where partition resources can be changed "on-the-fly", is vital where business services demands vary rapidly. In the best virtualization implementations, these elements are extended into advanced, virtual server management, with dynamic resources moved and shared between virtual servers under optimized workload management, for better (*or even best possible*) utilization of system resources.

*...System z10™ is today the unquestioned IT industry virtualization “Gold-Standard”.*

Virtualization was pioneered, deployed first on, and was most extensively developed and refined for, the IBM mainframe platform, over two and a half decades. The IBM System z10™ is today the unquestioned IT industry virtualization “Gold-Standard”. All types of System z10™ mainframe resources can

be fully virtualized, including processor cores, memory, I/O resources, and on-board virtual networking. Unlike most other platforms, System z10™ mainframes can safely and securely run many different applications inside one partition/OS image, with strong isolation and independence ensuring that no application interferes with another through memory protection keys (*System z’s form of containers*), all efficiently managed by the ultra-sophisticated **z/OS® Workload Manager** that ensures policy-set Service Level Agreement (SLA) QoS goals for each partition application are met. The System z’s long-optimized **dynamic LPAR (Logical PARTition)** bare-metal Type 1 hypervisor (**PR/SM™**) allows a z10 EC to be divided into <60 LPARs, each a rock-solid, totally isolated and ultra-secure, EAL5-rated partition, the resources of which can be dynamically changed and which runs its own OS (*any System z OS*). Processors, memory, and I/O resources, may be dedicated to an LPAR (*or virtual server*), or be shared across several, and resources can be dynamically added and deleted whilst LPAR partitions and virtual servers are actively running, which allows system-wide optimization across partitions. For this, IBM provides the **impressive Intelligent Resource Director (IRD)**, its industry-first, SLA policy-driven, cross-LPAR and cross-system workload optimizer that dynamically adjusts flexible LPAR resources to attain the extraordinarily high utilization rates (*often 95%+*) and consistent SLA delivery System z10™ machines reliably achieve (*which no others can*). LPARs can host separate development, test, and production environments, support multiple company, country or regional applications, and/or run other all System z operating systems/workloads, within a single System z10™ server. Support for the PR/SM™ hypervisor’s dynamic LPARs is deeply built into the z10 MPU and system hardware, and supported throughout its software stack.

A third virtualization layer is provided by **IBM’s famous z/VM extreme virtualization, bare-metal (Type 1) hypervisor** that can run within an LPAR, or on the System z metal. z/VM can uniquely host ~1,500 significant-weight Linux virtual servers (*on a top-end System z10™ EC*), each running the workload of a 1-2p x64 standard server, for huge consolidation gains. IBM’s Virtual Machine Resource Manager (**VMM**) software manages resources applied to workloads over virtual server groups within z/VM, and an extensive set of IBM software tools are packaged with, or offered for, z/VM.

Another invaluable System z virtualization unique is **HiperSockets™**. These are high-performance, very-low-latency, internal System z Transmission Control Protocol/Internet Protocol (**TCP/IP**) virtual network links between LPARs that allow extensive “within-the-box” virtual networking between applications in different partitions, at wire speed and without any external network switches, and cabling, etc., for huge performance and networking cost savings. Each System z10™ machine supports <16 HiperSockets™.

H. System Virtualization, Partitioning, Workload Management, and System Utilization:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5						

HP Integrity cell-based servers first provided HP nPartitions (*nPar*), static, electrically-isolated, coarse-grained hard partitions along cell-board boundaries. Mid-range rx7640 servers support 1-2 nPars, an rx8640 supports 1-4 nPars, and Integrity Superdome servers support 1-16 nPars, depending on model. An nPar can comprise one or several cell-boards, and runs its own operating system/workload in their combined resources. nPars first allowed HP 9000/Integrity systems to run multiple OS images, and different OSs on one HP 9000 UNIX server. Current Superdome cell-boards have 4 sockets, 8 Intel® Itanium® 9100 Series cores, <128GB main memory, and <12 I/O slots, so nPars are large, coarse-grained partitions. Cell-boards may now be concurrently added to/removed from a running nPar.

*nPars first allowed HP 9000/Integrity systems to run multiple OS images, and different OSs on one HP 9000 UNIX server.*

HP-UX next offered **HP Virtual Partitions (vPars)** software partitions allowing multiple, software-isolated HP-UX instances to share a server or an nPar hard partition, allowing dynamic resource changes, and with coarse granularity down to one processor core. **Secure Resource Partitions (SRO)**, HP’s form of containers, isolates applications within a partition/HP-UX operating system image, allowing multi-tenant/applications to share partition resources safely.

The HP **Virtual Server Environment (VSE)** includes nPars and vPars, but also adds virtual servers (see *HP Integrity Virtual Machines below*) whose resources can rise and fall under software or user control, to gain application-defined SLA goals. Newer, fine-grained **HP Integrity Virtual Machines (IVM)** software partitioning now let several IVM virtual servers share a single CPU and I/O resource, and can also support multiple guest operating-system instances/types (*HP-UX 11i, Windows, and Linux*). Traditional **HP-UX Workload Manager** manages HP-UX tasks and systems resources across partitions on a single HP Integrity system, whilst the newer, ambitious **HP Global Workload Manager (gWLM)** manages tasks and system CPU resources over multiple HP Integrity systems, and is recommended for new deployments. Both dynamically allocate (*different*) server resource sets seeking towards SLA goals defined by utilization priorities, where possible. gWLM integrates more closely with IVM above, and with **HP Insight-Dynamics-VSE**, the virtual server management component of **HP System Insight Manager (HPSIM)** that is included in HP VSE. For the UNIX market, these HP offerings comprise a broad virtualization, partitioning, workload management, and physical/virtual resource management palette that has considerably improved the utilization levels attainable on cell-based HP Integrity servers, from typical UNIX larger system 20-25% (2003) rates towards a better 40-45% (2009) average overall utilization level today.

It should be noted here that the now much richer, more well-developed, and more mature virtualization and virtual machine management that has developed for x64 platforms over the last decade (*VMware, XEN, Microsoft, etc.*) are way ahead of the Itanium®/HP integrity virtualization facilities above, although this x64 virtualization still remain a long way behind the System z10's unrivalled virtualization capabilities. This puts Itanium®/HP Integrity virtualization in fourth place, behind System z10, IBM Power Systems™, and x64 virtualization.

For both platforms, these virtualization and workload management capabilities are intertwined with their CoD capabilities (*point F above*), which offer options to increase and decrease certain system resources used, and to also help support higher-availability service delivery, as discussed in point I below.

This System z10™ long-refined and optimized multi-level virtualization of all system resources at a fine-grained level, supporting all the platform's OS environments, and its long-proven, policy-driven optimizing workload management capabilities, enable single large systems to concurrently handle scores of major applications, thousands of users, mixed OLTP, batch and interactive processing concurrently with utilization up to 95% or beyond, and with SLA goals automatically met. This allows extensive consolidation of many types of traditional and newer workloads, including classic mainframe OLTP and batch, newer data-serving and application-serving workloads like Java EE™, distributed server workloads on Linux, and also to run enterprise-wide DI hub roles/tasks (*including enterprise service management, asset management, security management, DR/BC, and information on demand, etc.*).

## I. Business Service Reliability, Availability, Serviceability, and DR/BC

Especially vital in high-end enterprise servers are extreme levels of reliability, availability and serviceability. These are essential to provide consistently-high QoS and availability for large, supported, mission-critical business applications, to eliminate as many types and instances of interruptions to a service as possible, to facilitate rapid and/or self-healing repair/recovery, and to allow most or all repair, maintenance, and recovery operations to be performed concurrently. Such "enterprise RAS" needs scores and scores of specific features and capabilities to be weaved and threaded deeply through every level of the enterprise system stack, from the MPU itself, up through all system hardware, through the virtualization firmware, across the operating system, across the supporting storage, over most of the platform's higher-level middleware software subsystems, and even into major applications.

IBM System z10™ EC mainframes are widely acknowledged as the most reliable, available and serviceable, general-purpose commercial computing systems, the culmination of 45 years of RAS-focused IBM mainframe development that continues today. System z10™ EC-based, single-system-powered, business services today can consistently achieve end-to-end ~99.995+% availability, with hardware MTBF now up to 1 in 50-60 years, and z/OS® Parallel Sysplex® cluster-based business services regularly exceeding 99.9995% availability. System z10™ mainframes achieve these outstanding levels through decades of advanced IBM RAS engineering, deeply built-in throughout the MPU (see *Section 3*), system, virtualization firmware, OS, and IBM System z middleware subsystems and engine stack, levels. Extensive error checking and correction of almost every chip function is built into the MPU, extensive further system-level error checking and correction covers cache, memory, chipset, I/O and other system hardware. Extensive redundancy and sparing are widely built in (*including spare processors*), the design eliminates all single-points-of-failure, autonomic self-diagnostic and self-repair capabilities are extensively used, much predictive failure analysis is built-in, and checkpoint/recovery techniques extensively employed to recover/restore most failure conditions.

Most major parts are hot-swappable, and extensive, concurrent update capabilities minimize most types of planned, as well as almost all unplanned, downtime. The tightly-coupled, long-optimized, well-integrated IBM System z virtualization firmware, operating system software, cluster software, middleware subsystem engines, and the system management capabilities, all contribute additional, as well as integrate these baseline platform RAS capabilities, better than on other platforms. Full program, address space, and data integrity, plus applications, subsystem and data recoverability, are built-in throughout this mainframe software stack, contributing much to the platform's high RAS, only possible with a highly-optimized, fully-integrated single-vendor stack. GDPS® extends z/OS® Parallel Sysplex® mainframe clusters (see *point E above*) to dual- or triple-site configurations, providing advanced DR/BC resilience across data centers, when combined with advanced mainframe IBM System Storage™ hardware and software (*DS8000 Turbo enterprise storage system, and the FlashCopy®, Global Mirror, Metro Mirror, Metro/Global Mirror and Global Copy flexible replication services software for backup and DR needs*).

I. Platform Business Service Reliability, Availability, Serviceability, and DR/BC:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 2, 3, 4, & 5						

By comparison, HP Integrity Superdome systems today fall well short. Intel has added increased basic RAS capabilities into Itanium® MPUs over its six generations to date, which HP Integrity systems harness and benefit from. But of twelve main Itanium® chip-level RAS functions implemented to date, ten are now also supported on the next Xeon® EX multiprocessor server MPU (*now code-named Nehalem-EX*), so Itanium® offers little more. HP also used standard large UNIX enterprise server approaches of SPOF elimination, N+1 redundancy (*fans, power supplies, and power input sources*), hot-swappable hardware components (*cell boards, fans/blowers, power supplies, PCI I/O cards*), HP chipset RAS support for memory error checking and correction, some HP-UX operating system support for RAS, service processor server event monitoring and management, and HP Serviceguard HA clustering solutions, to provide reasonably high RAS levels for Superdome systems. We would succinctly characterize their overall RAS capabilities today as being about 5-6 years and 3-4 generations behind those of the IBM System z10™ EC mainframe.

HP does, however, also offer the completely different architecture HP Integrity NonStop Massively Parallel Processing (*MPP*) cluster hardware (*also now using Intel® Itanium processors*), with its own NonStop operating system, that is built to a higher-RAS design point, to provide modern replacements for the dwindling, ex-Tandem/Compaq NonStop customer base. These fault-tolerant systems can achieve almost a magnitude higher availability than standard HP Integrity, at a price premium. HP therefore naturally sees little need to engineer higher levels of RAS into the standard HP Integrity servers, because doing so would further undermine the case for these HP Integrity NonStop systems, which it now also offers in blade format as well as in traditional NonStop MPP-node frame packaging.

Not surprisingly, amongst enterprise UNIX servers, IBM’s Power™ Systems RISC-UNIX systems have directly implemented the most System z mainframe-inspired RAS technologies in their POWER6+ MPUs, in the 560, 570, 575, and 595 server systems, in IBM’s Power VM™ hypervisor, and in the AIX operating system and clustering environment, because the same unified IBM STG system development organization builds both.

In many large enterprises, outage costs often exceed \$1,000,000 per business hour, and for such enterprises, operating high availability IT-powered business services is a financial imperative, and near-7\*24\*365 service continuity is often also required. The System z10™ EC shines for such requirements.

**J. System Security, Protection, Control, Audit, and Integrity**

Burgeoning enterprise computing Internet usage brought huge benefits, but amplified enterprise security risks/threats, now global. Viruses, malware, phishing, denial-of-service attacks, and fraud attempts, grew, inflicting serious reputation damage, and/or financial losses. The costs/complexity of defending businesses against such multi-fold threats thus increased, absorbing much IT staff time and effort, and money. Distributed systems are much the most widely attacked and most vulnerable (*Windows, Linux, UNIX in that order*) because of their weak security architecture, numerous OS holes/security issues, and for the frequent/costly patching needed. Enterprise server platforms hosting the largest, most mission-critical and sensitive enterprise data must deeply protect and secure enterprise users, applications, data, servers, and networks.

IBM System z10™ mainframes are the most secure, best-defended general-purpose commercial systems, a result of the intrinsically secure z/Architecture, many years of innovative IBM security advances/refinements, and many scores of security, protection, control, and integrity features, that alone allow IBM mainframes to claim “never-broken” status.

The System z10™ is uniquely Common Criteria Evaluation Assurance Level 5 (*EAL5*) certified for the security of its LPARs. System z10™ EC security starts with the **CP Assist for Cryptographic Function (CPACF)**, the platform’s standard, on-MPU-die, clear key encryption hardware unit, shared between each two CP or IFL PUs. CPACF performs Advanced Encryption Standard (*AES – 128-, and now also 192- and 256-bit keys*), Secure Hash Algorithm (*SHA1, SHA-224, SHA-256, and now also SHA-384 and SHA-512 for message digest*), Data Encryption Standard (*DES*) and Triple DES, and Pseudo-Random Number Generator (*PRNG*) encryption functions, in this MPU hardware at chip speed. This delivers uniquely powerful, chip-level cryptographic support for security-rich mainframe transactions under the four main System z10™ EC operating systems.

Optional System z10™ **Crypto Express 2 cryptographic-adapters** offer configurable, secure co-processing and/or SSL acceleration, enabling dramatically superior SSL transaction performances for Linux and z/OS (*at <16,000 SSL/sec per adapter*). Crypto Express 2 can now be dynamically added on an LPAR. Each Crypto Express 2 feature provides two PCI-X adapters that may be designated as co-processors or SSL accelerators, and a System z10™ EC can support <8 Crypto Express 2 features with <16 PCI-X adapters. Co-processing is Federal Information Processing Standard (*FIPS*) 140-2 Level 4 certified. The **z/OS® Integrated Cryptographic Service Facility (ICSF)** component transparently uses all available cryptographic functions (*CPACF and/or Crypto Express 2*), to balance cryptographic workloads and improve applications performance.

The powerful **z/OS® Security Server** (*Previously called RACF*) provides centralized authentication (*with IBM Tivoli Directory Server for z/OS®*). Extensive, fine-grained user and system resource accesses logging and reporting (*via System Management Facility (SMF)*), enables comprehensive audit support, compliance and risk management. Centralized certificate lifecycle management (*via z/OS® PKI Services*) cuts out third-party vendor digital certificate costs. The Automated Teller Machine/Point Of Sale machine (*ATM/POS*) remote key load facility enables centralized key management, and eliminates manual site visits and key entry errors. Lightweight Directory Access Protocol (*LDAP*) support is now provided for Hardware Management Console (*HMC*) user authentication. The IBM Trusted Key Entry (*TKE*) Workstation provides security-rich local and remote key management, and allows an optional Smart Card Reader to be attached. Centralized, mainframe-based, key management streamlines the management of encryption keys for enterprise IBM System Storage encrypting tape and disk, and will be eased by new **IBM Tivoli Key Lifecycle Manager** software (*in z/OS® V1.11*). Many other security features are built deeply into, and well integrated with, the System z10™ EC hardware, the IBM operating systems, and the IBM Tivoli middleware software stack.

J. System Security, Protection, Control, Audit, and Integrity:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5, other research						

Each HP Integrity operating system offers different security facilities too complex to fully assess here. HP Integrity servers provide no MPU-based, or hardware-accelerated encryption comparable to the high-performance System z10™ on-chip and Crypto Express 2 co-processors/accelerators (*also deeply supported in IBM OS and middleware*) above. HP Integrity can therefore only encrypt SSL magnitudes slower in software. Nor do HP Integrity systems provide an equivalent to the secure, high-performing System z10™ HiperSockets™ virtual networking links, which greatly cut exposure, and speed “in-box” networking.

HP-UX 11i V3 naturally provides the most security support, with basic facilities provided in all OE versions. **Standard Mode Security Enhancements** offer granular account and password policies system-wide or per-user, and can generate detailed system audits. More sophisticated identity and access management requires third-party software (*Red Hat Directory Server v7 for HP-UX 11i*) that is included as standard in RACF on z/OS®. **HP Security Containment for HP-UX 11i** adds containment (*isolating access to compartments*), fine-grained privileges, and more manageable role-based access controls. **HP-UX Bastille** provides flexible lock-down hardening. **Install-Time Security** allows default lockdown levels to be set on installation. **Host IDS** monitors for attacks, generates alerts, and can respond in real time. **IPFilter** provides system firewall capabilities.

These, and several other HP-UX security services (*authentication, naming services, Single Sign-On (SSO), and PKI, etc.*) enable the HP Integrity platform under HP-UX to offer a sound, enterprise UNIX level of security protection, access control, authentication, and audit compliance support.

On virtualization, HP nPar partitioning (*only*) is certified up to EAL4, whereas System z10™ LPAR is uniquely certified to EAL5, and z/VM is certified up to EAL4+ Common Criteria Assurance Level.

System z10™ users thus enjoy much more extensive, hardware-enhanced, and IBM software-enabled, security facilities that contribute to the System z mainframe’s unblemished security record, which also protects enterprises from malware and viruses as standard. System z10™ customers suffer few security breach costs, and spend far less time/effort/money on defense than distributed systems users. Several thousand banking/financial services mainframe users (*for whom top security is vital*) depend on this strength.

## K. Vendor’s Platform Middleware and Tools Software Stack

Much of the power, added-value, workloads enablement, application and solution deployment power, and appeal of an enterprise platform today now comes from the vendor’s middleware and tools software stack, and how well this is developed to integrate, fully exploit and support the platform’s latest operating systems and hardware capabilities. These must support and efficiently run a wide spectrum of enterprise workloads to deliver high-value, enterprise-wide business solutions with high top QoS, and strong economies of scale.

IBM is the world's number two software company after Microsoft, and the leader in most categories of enterprise middleware software and tools, with \$22B in 2008 revenues. System z mainframes have long been a major source of more software than hardware revenue to IBM, and so has been a central IBM software development platform focus this decade.

We extensively assessed main IBM new software categories on the IBM System z10™ mainframe in a number of in-depth papers (see page 77.) This decade IBM made continuous, intensive investments (totaling many \$B) into OS software, into central mainframe middleware software engines, including DB2, IMC, CICS, MQ Series, RACF, and OMEGAMON, etc., and into new domains. In recent years IBM added world leadership-class, new software suites in the strong growth domains of:

- **System z-Hosted SOA, BPM, & Business Event Processing.**
- **System z Application Development and Enterprise Modernization Tooling, Built on Eclipse.**
- **System z IOD, BI, and EPM.**
- **Enterprise Service Management Center hosted by System z for ITSM automation of IT.**

New open standards, innovative IBM R&D-based new technology, and dozens of IBM ISV acquisitions, were all deployed to build wide IBM and System z platform leadership into each domain's new IBM software offerings. Each is tightly integrated with, and fully optimized to exploit, the System z10™ mainframe platform's unique strengths and QoS, and to enable the numerous classes of new workloads that have driven most of the IBM mainframe capacity growth in recent years. In each area above, IBM's System z platform software is now the best in the world for any system platform, often by wide margins of advantage, our research found.

In addition to IBM's strong System z software advances since 2000, a burgeoning third-party ISV ecosystem is once again actively supporting the growing System z customer base, now extending to over 1,400 ISVs today offering a total of over 5,000 System z software applications, and providing a great choice of solutions to mainframe customers.

K. Vendor's Platform Middleware and Tools Software Stack:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"*	"z11" MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5 and other research						

HP, by contrast, has a much smaller, c \$3.00B per year, HP software business, one the company has sought to grow with acquisitions, including Mercury Interactive, Peregrine Systems, and OpsWare, and others, over recent years. HP's software interests are in IT Management (for which it is best known), Information Management, Communications and Media, and Printer and Server Management. HP long held a strong position in the telecommunications industry, and its Communications and Media infrastructure software serves those vertical industries. Printer and document management software complements HP's IPG printer/imaging systems business. In its larger IT Management segment, HP now offers a substantial portfolio of Business Technology Optimization (BTO) software for ITSM, including demand & portfolio management, SOA support, applications security, performance validation, QA, business service automation and management. HP Server Management offerings are highly-relevant in our context here, and the HP System Insight Manager and the HP Virtual Server Environment central parts of HP Integrity were discussed in Section 3 and elsewhere. HP seeks to grow in Information Management, where it has BI, business continuity/availability and enterprise document automation software solutions.

However, for all other core enterprise database, middleware and tools software categories, as well as for all other horizontal and vertical business applications solutions, HP depends entirely on third-party ISV partners, with Microsoft, Oracle, SAP, and IBM Software the largest and strongest of these. Earlier this decade, HP divested its own unsuccessful enterprise middleware interests. Oracle's acquisition of Sun makes this major HP software partner now also a head-on HP Integrity server platform competitor, an uncomfortable situation for HP.

Much of HP's (mid-sized) software portfolio obviously supports and runs on HP Integrity, with HP-UX the operating system offering most HP products. Because the HP Integrity platform started only from 2003, this portfolio remains relatively young in this current architectural incarnation, whereas IBM's System z stack has been optimized and refined over a far longer direct lineage.

In addition, the mainframe boasts a strong, dedicated community of ISVs providing a range of System z software tools (for example, capacity management, systems management, workload management, etc.). With the strong resurgence of the mainframe, many of these mainframe ISVs are now heavily reinvesting in, and actively enhancing and extending their System z offerings again, which often complement or extend IBM's own System z software products.

## L. Vendor Platform Support, and Professional Services, Capability/Quality

Enterprise platform customers have demanding support requirements for their mission-critical IT infrastructure, especially for the central mainframe and enterprise server platforms that host their most important, largest, applications and databases. They expect efficient, responsive, professional hardware service, parts, and repairs, regular vendor software enhancements and responsive vendor efforts to resolve customer-reported software issues with vendor operating systems and platform middleware, infrastructure, or management, software.

In addition, many enterprises need extensive vendor professional services when making major changes, advances, extensions, upgrades, or delivering new solutions, on their mainframes or enterprise server platforms. They often expect their main system vendors to provide extensive portfolios of well-defined and proven service solutions, and experienced teams with the depth of business area and technology backgrounds needed, at the capacity levels and in the locations major enterprise customers often require.

IBM System z service levels for both hardware and systems software are of a legendarily high standard. The extensive self-diagnosing, predictive failure analysis on System z machines detects most approaching hardware failures before they even occur, many failures are locally overcome with sparing and recovery options, but the systems also automatically call home, faults are fully diagnosed online, and service staff with parts are dispatched automatically when needed. An IBM service engineer has often visited and replaced a fading part before the customer even becomes aware! IBM System z software is also developed, tested, packaged, and released to extremely high, disciplined standards that increase its serviceability to the levels demanded in the rigorous System z environment and that eliminates many issues that other platforms suffer from. Graded levels of fast escalation and response, up to the highest standards for "mission-critical system down" priority issues are provided globally for System z mainframe customers.

IBM Global Services, with \$58.95B revenue in 2008, and 190,000 staff, is the world's largest IT services provider, offers an unrivalled breadth, depth, and coverage with the widest portfolio of professional services for every aspect of System z mainframe platform deployment, operations, expansion, clustering, DR/BC, and also for business solution deployment. This is complemented by IGS's extensive business consulting expertise in all major vertical industries, including those where mainframe usage remains central, such as banking, insurance, government, retailing, transportation, and utilities, etc.

It should be remembered that IBM's entire mainframe-related business franchise (*System z hardware, operating systems, IBM software, IBM storage, hardware and software maintenance, extensive professional services, and financing*) still comprises a huge c. \$35B p.a. (*we estimate*), or nearly-one third of IBM's annual revenue, and almost half of its profits, so IBM efforts to support and provide services around the mainframe platform are immense.

L. Vendor's Platform Support, And Profession Services, Capability/Quality:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System "z11"*	"z11" MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5 and other research						

HP held a generally favorable reputation for hardware maintenance and the support services it provides for the HP BCS enterprise systems of concern here. The construction of HP Integrity hardware is also generally rated as robust and solid, which along with the RAS, sparing, and hot-swappable provisions of the cell-based HP Integrity mid-to-larger systems, aids serviceability and speed of repair. Software support and developments of HP operating environments and related HP platform management, etc., software are less favorably viewed. HP is felt to have been slow and lagging with HP-UX OE-related developments for much of this decade. Whilst the OS is a relatively solid enterprise UNIX, some areas have fallen behind its competitors. Reduced HP-UX and other software support resources, and consequent weaker HP staff morale, are issues experienced by these HP customers.

In terms of professional services around the HP Integrity platform, HP itself traditionally centered its offerings around basic levels of IT technology-centric services, combining its own teams with the Compaq/Digital Equipment services resources acquired early this decade. These it has steadily broadened, including adding some higher-level, HP Integrity-specific service solution offerings in areas like DR/BC, clustering deployment, infrastructure consolidation, and ITSM, etc. HP's acquisition of the major EDS services business, now the hub of HP professional services, obviously added a wide range of outsourcing and high-end, but less HP-platform-specific, EDS services to that mix. The HP and EDS portfolios are in the process of being integrated, de-duplicated, cost-reduced, and rationalized, during this deep recession. As this process is completed, HP EDS will clearly offer a much more extensive breadth and depth of services portfolio than HP alone before, albeit still much smaller than that of IBM Global Services.

## M. Platform Total Cost of Ownership (TCO), Cost Per Transaction

Discussions and comparisons of mainframe costs versus UNIX/distributed platform costs, relative to capability and capacity, have for many years been deeply controversial, laced with ancient mainframe myths, fraught with endless UNIX and x64 platform marketing claims, and often lacking rigorous data. We researched mainframe, UNIX, and x64-platforms, and their comparative real total costs, extensively over the last five years, the basis for our comments following:

UNIX and x64 platform advocates invariably claim lower hardware purchase costs for their individual servers, always downplaying (*or ignoring*) the invariably now much larger software costs in every commercial computing role, and the high people costs needed to operate and support their platforms. Total Cost of Acquisition (TCA) centered on hardware is the focus of this approach. Proponents also downplayed the multiple servers and software sets essential to reach acceptable QoS levels, and the inefficient and wasteful actual utilization these multiple installed server hardware and software configurations achieve. Also often ignored were the extensive networking switches, links, and cabling costs needed to network-connect them, and the high power, cooling, and floor space area costs that multiple distributed systems needed. These distributed platform costs added together sharply compound over the full service lifetime period enterprises must consider when deciding their strategic platforms, 10 years plus. The total of such “outside-of-the-box” costs, always underplayed for UNIX and x64 enterprise platforms, are always many-fold higher than hardware acquisition costs, over all realistic 5-7-10-years lifecycle evaluations. Much of the case for the HP Integrity platform centers on single-box hardware purchase price-based arguments, claiming these as lower because they use “standard Intel processors”, and with these other aspects downplayed. Serious relative enterprise IT platform costs/economics consideration today must take fully into account:

- All major resource types, and all cost sources, needed to provide/run the whole enterprise platform. (*Servers, storage, network gear and links, data centre space and plant, operating system, middleware, tools, and applications software, all staff costs, power and cooling, and finance costs, etc.*)
- Software costs now nearly always outranks hardware costs several-fold in commercial IT today, so all software cost sources (*license, maintenance, subscription, support renewal, user licenses, CPU licenses, backup, and DR/BC, etc.*) must be accurately included. Using fewer software licenses more efficiently, on fewer systems and on fewer processor cores, is thus crucial to overall IT TCO reduction.
- In advanced markets, staffing costs today often are the largest part of overall TCO and recur yearly throughout the platform lifecycle. The many staff, tasks, and people-related costs, of implementing, supporting, operating, manage, securing, and administering an enterprise IT platform (*including the server hardware, storage, networking, OS and systems software, applications software, operations, security, performance management, and backup, etc.*) today can either equal or exceeds software costs as the highest IT platform cost in many countries. Obviously, country staff cost rates vary widely from the richest, most advanced nations, down to lower-cost emerging nations where wages are lower, driving the former to deploy more automated and productive platforms. There are also far wider differences in the levels of platform management/automation, and thus staff productivity, than most realize, with the mainframe ranked much the highest today.
- Fair comparison must be made of TCO for all IT platform service-related costs, over the full service lives that major IT assets and software depreciates over, at least 5 and up to 10 years for mainframes/large systems – to accurately weigh all cost-stream effects.

The IBM System z10™ EC mainframe, in contrast to HP Integrity, is a highly-integrated, consolidated, all-in-a-single-box solution, with all platform hardware and software fully pre-integrated and optimized by IBM. QoS levels for all attributes of enterprise platform service delivery are the highest any general-purpose single commercial system can deliver. Utilization of mainframe hardware and software resources reaches an extremely high level at <95%. Many diverse applications, new and traditional workloads, can all be easily and securely run together on one mainframe system, so far fewer software licenses are needed. System automation and self-management is the highest of any enterprise platform, System z support staff productivity has increased at least 7-fold in the last decade, and today System z support staff levels per 5,000 MIPS of service capacity/enterprise workload are the lowest amongst major platforms.

IBM System z hardware and software price curves provide sharply better unit costs as capacity increases, both on a single system, but especially for z/OS® Parallel Sysplex® clusters. This means already low costs per mainframe transaction (TCPT) drop sharply with increased usage scale. It thus pays greatly to add incremental workloads onto an existing mainframe. One large z10 EC mainframe can today readily deliver 2.5-5.0B real commercial transactions (*not artificial benchmarks*) per day, at a TCPT of \$0.000025 per transaction. IBM street prices for new high-end System z hardware have fallen a staggering 115-fold since 1990, and 15-fold since 1995, the latter at 20% CAGR per annum (*\$115,000/MIPS in 1990, \$14,900 in 1995, \$1,000/MIPS in 2008*), and IBM System z aggregate software prices have also fallen sharply, at a yearly ~19% CAGR from 1997 to 2009. Because System z10™ mainframes pack such huge capacity into a single, efficient box, they are also the greenest enterprise platform, needing the smallest data center space footprint, and far the lowest power and cooling costs per enterprise workload, 5000 MIPS capacity, or 10,000 users. However, at \$1M US street upwards, new z10 EC system hardware remains premium priced, reflecting the immense value of these above “in-the-box” QoS capabilities.



## M. Platform Overall TCO and TCPT:

IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”*	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5 and other research						

With HP Integrity large systems the biggest item in enterprise customer’s 7-10 year TCO will usually be for third-party ISV software for applications, middleware and tools (*Oracle, SAP, IBM, and BEA, etc.*) deployed on the Superdome systems, with a minority software costs for the HP-UX OE and management software to HP. The firm improved the value included with extended HP-UX OE bundles from HP-UX 11i v3 onwards. Total staff costs of running and supporting these large systems (*and all their software, storage, networks*), invariably used in multi-system clusters of 2-8 systems needed for large enterprise workloads (*see below*), will usually rank close to software as equal or next largest 7- to 10-year TCO source. HP Integrity hardware acquisition and maintenance costs will usually be third-placed in 7- to 10-year TCO cost item ranking, requiring one or two refresh/replace cycles depending on period. Whilst minimum, entry-level Superdome hardware list prices start at ~\$200,000, top configurations quickly reach several \$M list tags. A combination of networking gear and link costs, power, cooling, and data center capacity costs combined rank next in TCO contribution .

It has often been shown in practice that one top-end, 64-core System z10™ EC can run a large, commercial, mixed OLTP, Batch, and BI/EPM workload (*of ~30,000 IBM MIPS*) throughput that requires <4 top-end (*64-socket, 128-core, and big memory*) current HP Integrity Superdome systems to deliver comparable QoS (*response, I/O throughput, performance, availability, and DR/BC*) with both. This is because:

*It has often been shown in practice that one top-end, 64-core System z10™ EC can run a large, commercial, mixed OLTP, Batch, and BI/EPM workload throughput that requires <4 top-end current HP Integrity Superdome systems to deliver comparable QoS...*

- A System z10™ EC smoothly runs at <95% average utilization, but even partitioned HP Integrity Superdome systems rarely exceed 40-45% average, so roughly twice as much HP Superdome raw capacity must be installed for that factor alone. Superior System z10™ EC virtualization, and workload management optimization, account for this big difference.
- Most such major commercial workloads involve huge I/O volumes, and the I/O capacity, throughput, and performance of a IBM System z10™ EC is several-fold higher than that of an HP Integrity Superdome, so more than one are needed to handle typical I/O loads, for the reasons discussed earlier.
- 4.4GHz IBM System z10™ EC ~920 MIPS CISC MPUs are far faster, more powerful processors than HP Integrity Superdome 1.6GHz Intel® Itanium® 9100 Series processors, for such commercial workloads. 64 System z10™ EC processor cores can match <512 current HP Integrity Superdome processor cores in delivered work, an 8:1 MPU advantage, see below.
- A multi-system (2-4) HP Integrity Superdome Serviceguard cluster configuration is invariably needed to support such a size of workload, with concurrent service/support at equivalent high enterprise mission-critical service availability.
- A four HP Integrity Superdome cluster requires 4-8 times more software licenses than for a single comparable System z10™ EC, where software is certainly the largest TCO item, even when item-for-item System z software may be dearer.
- Staffing costs, usually the second largest TCO item, to operate and support four top-end HP Integrity Superdome machines are at least four times those needed to run one, highly-automated, and more productive, System z10™ EC.
- For deals of this size, large enterprise systems hardware cost is all special bid/usually vendor-discounted to win. So one top-end System z10™ EC at \$25M list hardware price might be discounted to \$15M within a larger overall IBM bid, and the equivalent four at \$5M list (*\$20M total*) top HP Integrity Superdome system hardware bid might discount to perhaps \$14M, almost equal initial hardware costs for the much longer-life System z10™ hardware.
- Networking gear, links, power, cooling, and data centre space costs, are all also far lower with the System z10™ EC solution.

The decade-and-a-half of radical IBM mainframe hardware and software cost reductions, and soaring mainframe performance/capacity, extreme-virtualization-driven efficiency, extensive automation/low staff needs, and excellent “green IT” strengths, now often make System z10™ the lowest true TCO cost, and always the lowest cost per transaction, platform for substantial, mixed, commercial workloads today. IBM’s Power Systems™ 595 has the top TCO/TCPT for UNIX performance-focused workloads, so we show them as equal (*but for different workloads*) to System z on this crucial factor.

## L. Platform Investment Protection and Safety

This important strategic consideration gauges how well a customer's enterprise platform's hardware, software, applications, data and people skills investments are protected in the long term. This heavily affects enterprise platform TCO (*discussed above*) over the decades, and also determines how safely customers can build their IT infrastructures upon that platform. IBM System z mainframes feature decades-long customer software upwards compatibility, high-quality hardware, longer service lives (<6- to 8-years – versus 3+/-\* for UNIX/distributed systems), strong system residual values, attractive upgrade paths, carry-forward of bought major components, superb IBM support, and extensive service offerings, all adding System z investment value. Attractive upgrade paths to new generations/higher models are always offered. Purchased specialty processors and channel I/O gear can be reused on new mainframes without charge. Great platform stability, continuity, and deeply engineered-in upward compatibility dating back 45 years, are well-known. These factors make IBM System z consistently better at preserving customer application software, transactions, data, and staff skill investments than any other enterprise IT platform. IBM is also unquestionably and publically committed (*Mainframe Charter*) to continued, intense System z development, far ahead for the next decade/decades.

N. Platform Investment Protection and Safety/Risk:						
IBM System z10™	z10 MPU					
HP Integrity	Itanium® 9100					
IBM System “z11”**	“z11” MPU*					
HP Integrity*	Tukwila MC					
Sources: Sections 3 & 5 and other research						

By contrast, HP killed-off four major server platforms, and two major operating systems, already this decade, inflicting costly, disruptive discontinuities (*of MPU, system architecture, and operating system*) on many thousand HP customers using these now no-longer-sold systems. Many such HP customers lost much of their platform investments. HP Integrity systems, built from 2003, have reasonably replaced HP 9000 systems running HP-UX, but thousands of others (*including HP e-3000 and HP AlphaServer users*) needed complex, costly migrations. Many rejected HP Integrity, and/or fled from HP, as a result. In fairness, HP fully ported HP-UX and OpenVMS to HP Integrity, carrying forward customers' software investments in those OSs. It also offered useful HP 9000 to HP Integrity hardware carry-forward and upgrade options that helped investments last longer during the transition, including in-chassis upgrades.

The turbulent, much-delayed, under-performing Itanium® MPU saga (*see Section 2*) left HP Integrity Superdome servers often lagging behind main-competitor IBM from 2003-2009, making them poor investment value for customers. Now, rising strategic uncertainty surrounds the medium-term future of Itanium® MPUs, and hence of this HP enterprise platform. Itanium® cancellation by Intel two- to three-years ahead is now openly forecast by competitors and some analysts. That record, and these uncertainties, make HP Integrity Superdome customer investment protection much weaker, and strategic platform continuance risks much higher, than for the IBM System z10™, whose track-record is unimpeachable, and whose future is solidly assured.

## Our Analysis

We conclude this White Paper with a single chart encapsulating, summarizing, and visualizing our main findings in graphical form: Figure 12 on page 67. We combined our actual-data-based ratings on each of the above fourteen main differentiating factors of comparison for the current generation, with our part data/part surmise-based ratings for the next generation, of our main subject IBM System z EC mainframes (*current System z10™ EC and next System “z11 EC”*) and HP Integrity Superdome (*current Montvale and next Tukwila MC-based*) platforms. We added our relative ratings of the IBM Power Systems™ 595 enterprise servers (*expected 2009 POWER6+ version, and 2010 POWER7 replacement*) on these factors to further clarify the relative strengths of all three platforms.

This chart therefore provides our relative assessments of these three enterprise platforms over the period 2009 to 2012, across their current, and their next-generation advances, on these fourteen differentiating factors. Figure 12 shows the strongest-rated platform symbols to the left, and the lowest rated platform symbols to the right, each positioned to scale on the chart within ranges bounded by upper and lower scores for each factor. We use this format to clarify and accentuate differences between platforms by design. The System z10™ EC mainframe is universally recognized as the most sophisticated and advanced enterprise platform, whose capabilities all enterprise servers contenders strive to copy, so it is no surprise this reference standard scores most top ratings within these three families.

It should be born in mind that a bottom rating within this elite group of three top-end enterprise systems may well still be an acceptable rating for many users/purposes. We also stress that the factors used here did not cover every consideration, and that we specifically excluded several where differences were rather less marked.

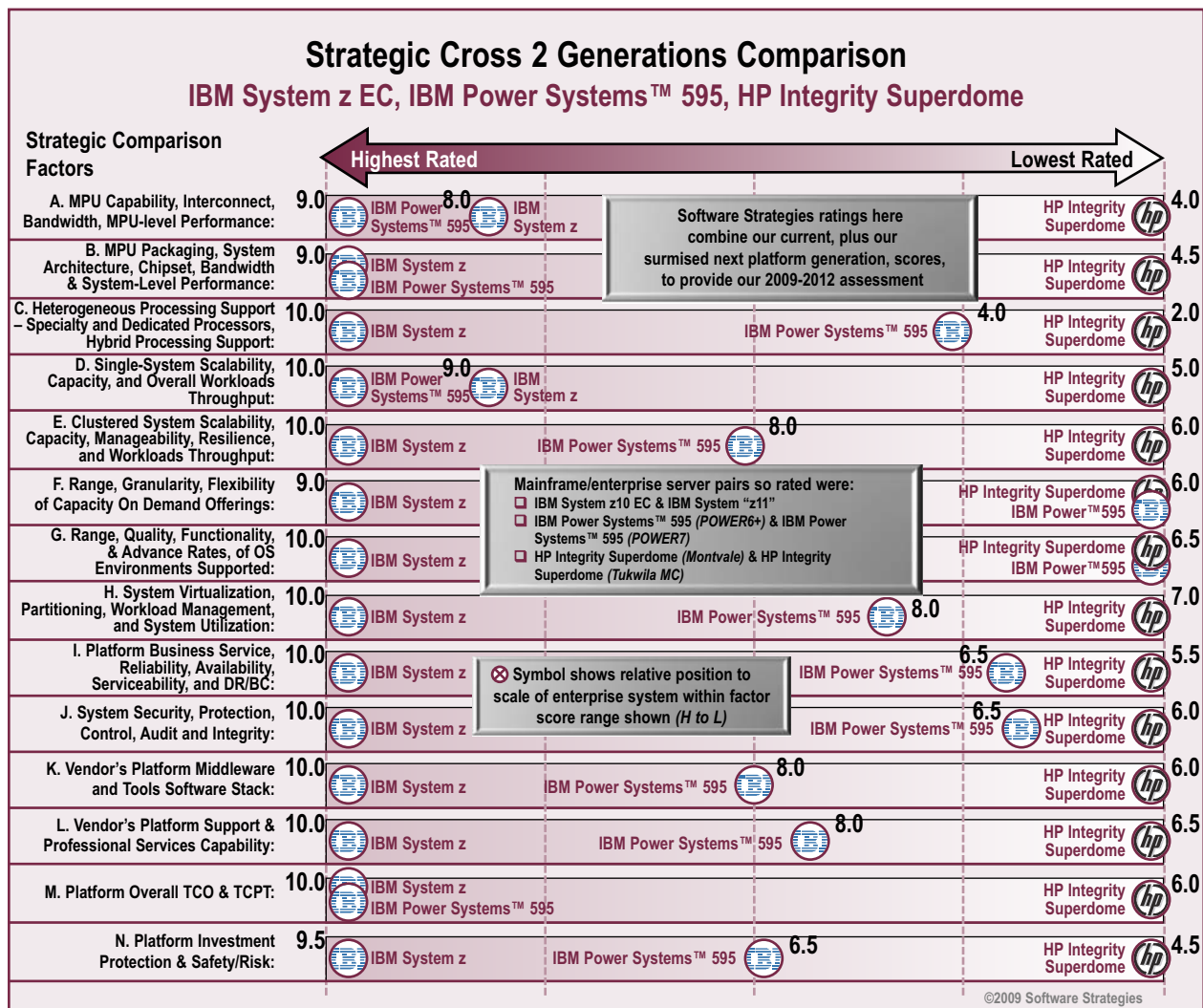


Figure 12: Strategic Cross 2 Generation Comparison – IBM System z EC, IBM Power Systems™ 595, HP Integrity Superdome

The results speak for themselves, with the System z10™ EC in a class of its own, widely ahead of HP Integrity Superdome in most factors, with the rather more similar IBM Power Systems™ 595 RISC-UNIX server also firmly beating the HP platform on key factors, and thus running closer to IBM's System z in our ratings.

*...with the System z10™ EC in a class of its own, widely ahead of HP Integrity Superdome in most factors...*

## Appendix A: The Itanium® MPU – Where and Why it Failed

### Introduction

We assessed the Itanium® story mainly in Section 2, but include further back-up evidence supporting our Section 2 findings and conclusions here in Appendix A.

### Goodbye PA-RISC, Hello Intel – HP Escapes Heavy Server MPU Costs

In 1989, when HP's EPIC work began, the firm first shipped its own-designed/fabricated PA-RISC MPU (*the PA-7000*), beginning a modestly successful RISC MPU family made/used by HP until 2008. PA-RISC gave HP one MPU to unify its HP 3000 mid-range, and mainstream HP 9000 RISC-UNIX, server families, until their respective EOS at end-2003 and end-2008. Although not a top RISC performer, PA-RISC was competitive enough to give HP short UNIX revenue share lead periods early this decade, before IBM pulled ahead. Ironically, the last two PA-RISC MPU-powered HP 9000 generations remained popular up to their EOS, slowing migration to HP Integrity. The many Itanium® delays/setbacks caused this.

When it teamed with Intel from 1994, HP planned to replace the still-young PA-RISC MPUs with the duo's IA-64, first new chips and HP IA-64 systems planned to ship from 1998. PA-RISC would be phased out five years later. HP wanted to exit the overcrowded RISC MPU market, cut its costly and engineer-intensive MPU development, and to divest high-capital HP fabrication facilities where low HP chip volumes gave poor MPU economics. HP hoped to sharply cut enterprise system development/manufacture costs. It would then rely on Intel (*and AMD*) for all MPUs it used in all future HP systems, hoping for big benefits from Intel's chip prowess, multi-\$B fabrication investments, and from lower MPU prices the huge IA-64 sales volumes forecast would bring. If only! This decision doomed PA-RISC to an early grave.

*HP thus completed its desired escape, burning the last bridges from its MPU-designing and chip making capability/history.*

HP's 2002 Compaq buy added complexity to the HP MPU/systems portfolio. In came ex-Digital Alpha-RISC MPU-based AlphaServers, and the Compaq NonStop MIPS-RISC MPU-based systems. Compaq was replacing Alpha-RISC MPUs with Itanium® MPUs, and had sold its Alpha RISC MPU IPR and design team to Intel, before HP took over.

HP later finally transferred its Itanium®/PA-RISC MPU design/development team at Fort Collins, Colorado, across to Intel in 2005. HP thus completed its desired escape, burning the last bridges from its MPU-designing and chip making capability/history. In view of what followed, HP had ample cause to regret this "all-or-nothing" Itanium® bet.

For its part, from 1994 to date, Intel would sink what became \$5B+ of investment into IA-64. This would build what it then expected to be the complete successor to its apparently then "creaking-at-the-seams", but highly-successful IA-32 MPUs, and would give Intel the right MPU engine to dominate all the other higher-end MPU segments IA-64 then targeted.

### High Performance Computing (HPC) – Itanium® Nowhere Today, Share Collapsed

Amongst Intel & HP's strongest Itanium® claims was for the high performance that IA-64's EPIC architecture would provide. The duo also said high IA-64 MPU sales from winning all system segments would bring "Intel economics" with ultra-competitive MPU pricing. Surely by 2008, seven years after the first Itanium® MPU generation, this titan of HPC and volume MPU economics value must by now utterly dominate the important HPC (*supercomputer*) segment? Well no, actually. Itanium® MPU-powered HPC systems numbered just 9 out of the top 500, or 1.8%, on the last TOP500 Supercomputers List ranking, summarized in Figure 5 below.

*Itanium® MPU-powered HPC systems numbered just 9 out of the top 500, or 1.8%, on the last TOP500 Supercomputers List...*

TOP500 Supercomputers List – November 2008 – By Processor Families					
MPU Family	Number of Systems	Systems Share %	Rmax Sum (GF)	Rpeak Sum (GF)	Total Processors
Intel 64 (EM64T)	369	73.80%	8,162,164	13,857,895	1,283,566
IBM Power	60	12.00%	4,343,108	5,625,505	1,062,880
AMD64	60	12.00%	4,029,163	5,458,034	699,613
Intel IA-64- Itanium®	9	1.80%	338,491	398,847	63,696
NEC	1	0.20%	35,860	40,960	5,120
SPARC-all	1	0.20%	18,540	20,643	2,048
Totals	500	100%	16,927,326	25,401,884	3,116,923

Figure A1: TOP500 Supercomputers List – November 2008 – By MPU Families

Hmmm... but surely the high-performance powerhouse Itanium® MPU family (*per Intel & HP*) must still be increasing HPC market share, if it is indeed the performance titan so loudly touted? Well no actually. Intel IA-64 HPC usage peaked at 84 systems, 16.8% of the 11/2004 TOP500 list. Since then, the Itanium® **share has collapsed over nine-fold to the tiny 1.8% share today**. Not quite as bad as Sun SPARC, which is now down to just 0.2%, but a major collapse also.

HPC systems using x64 MPUs (*Intel 64 and AMD-64*) have soared to now power 429, or 85.8%, of the top 500 places in the latest 11/2008 TOP500 Supercomputers List with IBM's Power MPUs splitting the twins in the table above. These three MPU families combined powered 97.8% of the latest List's HPC systems.

Itanium® HPC share collapsed because of uncompetitive performance and price/performance, compared to the faster-paced gains of its Intel/AMD x64 and IBM POWER MPU-based competitors. **So much for years of Intel® Itanium® and HP Integrity HPC claims!** Today, HPC is no longer ever mentioned as an HP Integrity, or Intel® Itanium® MPU, target market.

## Performance Workstations All Abandoned Itanium®, Now a Solid x64 Segment

In the 1980s, performance workstations were a fast-growth segment, used for Computer Aided Design (CAD)/Computer Aided Manufacturing (CAM), high-end publishing, geo-spatial applications, visual effects, and like graphics-rich applications. Workstations then needed “3Ms”- 1 Megabyte of memory, a 1 Megapixel display, and 1 MegaFLOPS performance – well beyond PCs of those days – and typically cost \$10K. New workstation vendors Apollo Computer (1980), Sun Microsystems (1982), and Silicon Graphics, Inc. (SGI) (1981) sprung up, and mini-makers HP and DEC joined the fray. Their early workstations mostly used powerful, good value, Motorola 68000 32-bit CISC merchant MPUs.

The vendors next adopted high-performing RISC MPUs as these emerged. Sun’s Sun 4 (on SPARC RISC), HP’s 9000 (on PA-RISC), SGI (on MIPS RISC), and IBM RS/6000 (on POWER RISC) all offered 32-bit RISC MPU-based, mostly UNIX OS, workstations. These moved up to 64-bit by the mid-1990s, boosting headroom/performance, and held workstation share high-ground through that decade.

From 1994, HP and Intel saw RISC MPU-based performance workstations as a major IA-64 target market. With EPIC’s strong floating point performance, the pair claimed IA-64 MPUs would quickly replace RISC MPUs in this segment. High-volume workstation sales were vital to Itanium® for two reasons. Firstly, high workstation sales would provide the big volumes of Itanium® MPU sales so vital to keeping server MPU prices competitive. Secondly, wide workstation uptake would speed Itanium® software migration, later the crucial barrier impeding the MPU’s success for years.

With hopes high, all Club Itanium vendors launched IA-64 workstations (most in 2001-2003). These were partner HP (HP Workstation zx2000, zx6000, and HP Integrity workstations), SGI (SGI 750, Prism), IBM (IBM IntelliStation Z Pro), Dell (Precision Workstation 730), Fujitsu (Celsius 880), NEC (NEC Express5800/59Wa) and Hitachi (Hitachi FLORA-ex 480), etc. However, the expected Itanium® workstation market never took off, and vendors rapidly killed all these machines, Dell in 2002, IBM in 2003, main Itanium® supporter HP in 2004, and SGI in 2007. In 2005, Microsoft even cancelled its Itanium® workstation Windows OS, a final death-knell. **Itanium® workstations were a business catastrophe**, writing off many \$10Ms of Club Itanium vendor workstation/chipset development costs/inventory. End-customers unfortunate enough to have bought an Itanium® workstation were lumbered with dead-end products.

Instead, workstations migrated from RISC MPUs, to powerful x64 Intel/AMD MPUs that today drive nearly all high-end, PC-style workstations. With perfect x86 software compatibility, widest software portfolios, excellent 32-bit and 64-bit performance, 64-bit addressing headroom (from 2003), high chip sales volumes, and low MPU costs, x64 MPUs proved ideal for all except a tiny few of the most exotic, top-end workstations, killing Itanium® workstation hopes stone dead.

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*...x64 MPUs proved ideal for all except a tiny few of the most exotic, top-end workstations, killing Itanium® workstation hopes stone dead.*

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## Other MPU Evolutions Confounded the Intel/HP Duo’s Itanic Hopes

From their hubris-rich 1994 partnership launch onwards, Intel and HP expected IA-64 would replace Intel’s own dominant high-volume x86 MPU, IBM mainframe, and other CISC MPUs, as well as all the much-younger and then still in-vogue RISC MPUs, in

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*...Intel and HP expected IA-64 would replace Intel’s own dominant high-volume x86 MPU, IBM mainframe, and other CISC MPUs, as well as all the much-younger and then still in-vogue RISC MPUs, in each main computer system market, within a few years.*

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each main computer system market, within a few years. The outcome was far different, completely confounding such hopes. Two major segments where Itanium® failed completely were assessed above. Why such failure? How were the early predictions for Itanium® success so wrong?

The over-riding reason was the unexpected (to the Intel-HP duo) and large-scale later success of two crucial CISC MPU lines, and of one leading RISC MPU architecture, over the 2000 decade.

When HP began EPIC research in 1989, **proprietary Complex Instruction Set Computer (CISC)** MPU architectures still dominated, powering all mainframes, most proprietary minicomputers/mid-range business systems, and all PCs and PC servers, of that time. Observers argued that the IT industry could no longer support so many CISC MPU architectures, and sharp IT industry consolidation has indeed drastically thinned their ranks since.

But two important CISC MPU architectures have thrived strongly in their respective markets, each still holding commanding positions in 2009:

- **Intel/AMD x64:** The hugely successful, 2003/2004 x86 AMD and Intel moves to 64-bit extended “x64” architecture enabled these CISC MPUs to extend their dominance of industry-standard servers, workstations, and high-end PCs up-scale, with rapid advances, as well as outstanding price/performance from huge unit sales volumes. Far from running out of headroom, as Intel and HP projected when they launched IA-64 (*expecting it to supersede x86*), **x64 MPUs went from strength-to-strength over the last six years**. They advanced more quickly than Itanium®, offered better value, and can now also even power effective, medium to large scale-up SMP systems (<32-socket) that eat deeply into a high-end server segment the partners long-expected Itanium® MPU-powered enterprise systems would solidly capture.
- **IBM System z CISC MPUs:** This successful proprietary CISC MPU leader moved up to IBM's much-extended, 64-bit z/Architecture MPUs from 2000 onwards. IBM has delivered five on-schedule, new generations of powerful 64-bit IBM CISC z MPUs and System z mainframes, each co-optimized, since late-2000. These enabled resurgent market success, won many new workloads, and drove the soaring capacity growth the System z platform has enjoyed this 2000 decade. (*See Section 4 for our System z10™ assessment.*) IBM System z MPUs advanced strongly alongside, and have shared units, features, concepts, and process technologies with IBM's winning POWER RISC MPUs (*see below*) that dominated UNIX server markets for most of this decade.

Also in 1989, new **Reduced Instruction Set Computer (RISC)** MPU architectures had just emerged (*based on early IBM, and 1980s university, research*), promising simpler MPUs with fewer instructions, most hardwired, and so bringing higher performance than CISC designs at lower MPU costs. Vendors delivering RISC MPUs/systems included Sun SPARC (*from 1987*), HP PA-RISC (*from 1989*), IBM POWER RISC (*from 1991*), MIPS MIPS-RISC (*from 1985*), and Dec Alpha-RISC (*from 1992, first 64-bit*), to name/date the more important. RISC MPUs quickly dominated the fast-growth workstation segment (*Sun, Apollo, HP, IBM, etc.*) as discussed above. RISC MPUs advanced to full 64-bit architectures by the mid-1990s. Over that decade, RISC MPUs powered the surging RISC-UNIX server wave (*Sun, HP, IBM, Pyramid, Sequent, Digital Equipment, etc.*). These swept away proprietary CISC mini-computers, and scaled-up to enterprise server level by the late 1990s. These RISC systems gave excellent raw compute performance, strong price/performance, and faster advances from CMOS MPU technology gains, but lacked the RAS, QoS, virtualization, security, automation, and manageability strengths of the mainframe. RISC-UNIX revenues mushroomed to become the largest server segment, peaking at around \$27B p.a. (2004).

- **IBM POWER4/POWER4+POWER5/POWER5+/POWER6, and POWER7RISC:** In 2001, after five years of intense development, IBM struck its decisive first blow for RISC server and MPU dominance. It first shipped high-end p Series servers (*the famous p690 Regatta*) based on the storming POWER4 dual-core 64-bit RISC server MPU, a dramatic leap forward, and far the highest-performing 64-bit MPU then. This was a full five years before Intel managed to deliver a dual-core version of Itanium®, Montecito, in 2006. The POWER4 MPU was deeply integrated into an optimized system architecture, using advanced, mainframe-style MCM packaging, a high-bandwidth on-die distributed switch interconnect, and with advanced RAS support on board. IBM executed well, with mostly on-time schedule delivery/deployment of successive POWER4+ (2002-2003), POWER5 (2004-2005), POWER5+ (2005-2006-on), and currently POWER6/POWER6+ (2007-2009) MPU generations powering all IBM System p and i servers, now renamed IBM Power Systems™. These **IBM POWER MPUs have stayed well or far ahead of all competing 64-bit RISC or EPIC server MPUs** in MPU and system performance, often on price/performance too, in systems architecture integration, with pioneering virtualization features, highest bandwidth, and more advanced RAS features, since 2001. IBM Power™ servers posted far the largest number of leading industry performance benchmark results over this period, vastly outstripping HP Integrity's limited wins. IBM also seized a commanding revenue share lead in the UNIX market as a direct result; surely the acid test.

The unexpected (*to Intel and HP*) successes of the two CISC MPU architectures above, the mid-1990s on RISC-UNIX systems growth decade, and the last eight years of dominant performance leadership by IBM POWER MPU-based UNIX servers, completely confounded the duo's high early ambitions for Itanium®. In fact, Itanium® MPU-powered servers (*nearly all from HP*) were rarely or barely competitive with best-of-breed IBM RISC-UNIX systems, running well behind this leader for most time-periods from 2001 to 2009.

## Itanium® Chipsets an Entry Barrier

To build Itanium® MPU-based systems, a suitable system chipset is needed to interface MPUs to system memory, to make all needed system interconnections, and to integrate I/O controllers, etc. A new system chipset for enterprise servers costs from several \$10Ms upwards to design, develop, debug, and for the set's chips to be fabricated. Designing a new chipset, especially one offering differentiating enterprise features, is a lengthy, challenging system and semiconductor design and validation task requiring high-order system design skills and expertise. Little open market in Itanium®-supportive chipsets developed, in contrast to the good range available for x86/x64 servers and workstations. Intel provided two early low-end Itanium® chipsets, the 2001 460GX for Merced and the 2002 E8870 for early Itanium® 2 MPUs with the 400MHz. FSB, but offered no newer chipsets since then.

HP has produced two generations of low-end, and two generations of high-end, HP Itanium® chipsets to date, discussed in Section 3, and is likely to make at least another generation high-end chipset for the next Tukwila MC socket/generation HP Integrity servers. NEC, Fujitsu, SGI, and Hitachi each manufactured their own Itanium® chipsets, used in their current systems. But with their tiny Itanium® server volumes, 5% of 2008 units sold between all the non-HP vendors, it seems unlikely these Club Itanium firms could again invest in new-generation chipsets. Indeed, a decision not to do so was likely in part to have been behind Unisys' recent move to an all-Xeon® MPU-based enterprise server strategy, and to dropping Itanium®.

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*Intel for years has sought a more common server platform for both Itanium® and Xeon® EX MPUs in similar multiprocessor server hardware.*

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Intel for years has sought a more common server platform for both Itanium® and Xeon® EX MPUs in similar multiprocessor server hardware. Both of Intel's next, high-end MPUs share the new QPI interconnect, and several other common features – for example, Intel VT virtualization support – as this platform convergence slowly increased.

The next steps, per Intel's 2009 public roadmaps, are the Boxboro MC Server Platform, comprising the next Itanium® Tukwila MC chip and Intel Boxboro MC I/O chipset (*details not known*), both now due to ship in Q1 2010. This platform also brings a new Itanium® socket to also be used on the following two Itanium® generations as well. (*Reducing system vendor development costs.*)

On the Xeon® side, the current high-end Intel® Xeon 7400 Series-based EXpandable Platform (EX) Server Platform (*Caneland*) will be followed by Q1 2010 production of Intel's new Boxboro EX Server Platform. This introduces the impressive, new, <8 core, Nehalem micro-architecture MPU (*code-named Nehalem-EX*), and new Boxboro EX (<8 socket) chipset. This flagship high-end Xeon® EX system platform will be a formidable competitor to Itanium® Tukwila MC/Boxboro in enterprise servers. Commonality between the new Boxboro MC and Boxboro EX chipsets as yet remains unclear. However, such increased platform commonality/convergence will significantly ease/facilitate a more graceful Intel/HP exit from Itanium® in 2-3 years time.

## Other Itanium® Vendors Win <5% 2008 Units – Other Majors Abandon

Intel and the ISA make much play about the other (*than dominant HP*) system vendors building Itanium®-based systems, now just high-end RISC and mainframe CISC replacement aimed, but unit sales by these vendors are insignificant. The remaining Itanium® vendors (*dwindling number*), and their 2009 Itanium® systems and other server offerings, are:

- **NEC:** NEC Express5800/1000 (*1- to 32-way*) Itanium®, since 2002. NEC also uses Itanium® MPUs to power its i-PX9000 replacement for the NEC ACOS mainframes (*Japan only*). But NEC recently delivered its ultra-competitive "Monster-Xeon" scalable enterprise servers, engineered jointly with Unisys, which both now sell; NEC as its Express5800/A1160 and Unisys as its ES7000 Model 7600R. These large, x64 Xeon® EX ("*Dunnington*") MPU powered, cell-based an SMP-like systems currently support <64 or 96 cores, using NEC's MX5800 chipset. See also our Unisys analysis below.
- **Fujitsu:** Fujitsu PRIMEQUEST (*1- to 32-way*) Itanium® from 2005. But these compete directly against Fujitsu's own main PRIMEPOWER (*SPARC64-MPU*), and extensive SPARC Enterprise (*also marketed by Sun*) server ranges, which are much more important to the firm. Recent company statements have emphasized that Fujitsu also now plans increased usage of x64 processors in forthcoming Fujitsu server platforms.
- **SGI:** Altix 4000 (*1 to 2,048-way*) shared memory HPC system. Long-troubled supercomputer/workstation vendor just entered Chapter 11 bankruptcy again, to be bought out for just \$25M by Rackable Systems (*April 2009*). Was still offering its Altix 4000 Itanium®-based system, but pushing x64-based clusters harder, before this buyout.
- **Hitachi:** BladeSymphony 1000 (*1- to 8-way*) mainly for Japan/Asia.
- **Groupe Bull:** NovaScale (*1- to 32-way*) from 2002. Bull legacy mainframe replacement, sell tiny volumes. Bull also resells much higher numbers of rebadged IBM Power™ RISC-UNIX servers.

Most of these other Itanium® vendors have heavier investments, and make larger efforts, on their other server platforms. Major system vendors abandoning Itanium® completely, after building and selling systems on the MPU platform, were:

- **IBM:** In an early, serious credibility blow for Itanium®, top Tier 1 server vendor IBM abandoned its Itanium® server and workstations lines in 2005, after shipping the scalable x455 mid-range server, having engineering (*at great cost*) two generations of IBM X Architecture (*Summit*) chipsets in two versions that supported both Itanium® and x86/x64 MPUs. IBM led in high-end x64 servers with its modular, scale-up IBM X Architecture Xeon®-powered, mid- to high-end servers from 2001 through four X-Architecture chipsets/generations to date.
- **Dell:** Another serious blow also fell in 2005, when Tier 1 high-volume PC/ISS server specialist Dell also abandoned Itanium®, after poor sales of its first (*and only*) Dell PowerEdge 7250 (<4-way) server and workstation. This devastating Dell decision killed Intel's main hopes of high-volume workstation and ISS server Itanium® sales outside of HP.

- **Unisys:** Especially interesting is Unisys' experience. Most active proprietary mainframe vendor (*ClearPath*) after IBM, but never a RISC-UNIX player, Unisys pioneered scale-up Intel® Xeon®-based enterprise servers with its ES7000 line from 2001, partnering Microsoft. Most of these Unisys ES7000 cellular multiprocessing, SMP-like, large NUMA systems used Intel® Xeon® x86/x64 MPUs. But Unisys also offered Itanium® MPU-powered ES7000 systems and cell-modules (*some systems could mix Itanium® and Xeon® MP cells*) from 2002 to 2009. At peak, Unisys was winning <25% of ES7000 revenue from Itanium®. But by February 2009, when Unisys announced its latest "Monster Xeon" ES7000 Model 7600R (*co-designed with, and built for Unisys by NEC*), it disclosed that Itanium® sales had plummeted to single-digit %. "*Our customers have voted with their feet and their wallets. In the past twelve months especially, we have seen a dramatic shift from Itanium® to Xeon.*" said Colin Lacey, Systems and Storage VP, Unisys Systems & Technology. Better Xeon® MPU system performance, and especially price/performance, lies behind this switch. Lacey also disclosed extensive Unisys field data had shown that the firm's Xeon®-based ES7000 systems were just as reliable and available as its similar Itanium®-powered systems, demolishing Intel's claim for superior Itanium®-based system RAS. (*Sources 18, 19, and 20, page 76.*)

Abandonment of Itanium® by these three major, experienced system vendors, after each had made significant investments in, and strong efforts to sell, Itanium®-based systems, left HP the only Tier 1 vendor still supporting the Itanium® MPU.

## Appendix B: World-class "Itanic" Truth-bending

### Introduction

In researching this White Paper we looked at two crucial areas that define Itanium®-based system status and ranking in the marketplace. In both cases, we found Club Itanium (*Intel, HP, and their ISA pals*) all quoting and presenting the same (*or similar*) "**extremely misleading" claims/numbers (to put it charitably)** to promote their favorite platform's case. Two examples, on important Itanium® market standing metrics, are briefly untangled below, to illustrate this pattern.

### 1. The Itanium® Platforms ISV Applications Portfolio – Double Counting?

A crucial customer criterion when choosing enterprise server platforms is the breadth and quality of ISV software solutions offered on the platform. HP Integrity servers accounted for 95% of all Itanium® systems sold in 2008, and so are almost synonymous with Itanium® MPU-based platforms as a whole.

Glacially slow global 2001-2005 Itanium®-based server uptake gave little encouragement to ISVs. Most delayed committing the major costs/efforts needed to port/optimize their products natively for Itanium®. To be fully platform-exploitative on HP Integrity, ISVs needed to re-architect, rewrite, optimize, and recompile for Itanium® Architecture, each product/release that they wanted to offer, and to commit to providing years of support – major investments for any ISV. IA-32 software, a huge segment, ran poorly on Itanium® from day one, and still does today, compared to how it performs on current, native x64 hardware. When repeated Intel delays left relative performance uncompetitive, and Itanium® server sales ran far below every IDC forecast, most ISV porting business cases became unviable.

The four different operating system families on HP Integrity further divided platform market potential, forcing ISVs to chose which OS/versions their software should support. Positively, these four OS families each brought their prior ISV portfolios as "OS affinity candidates" for slightly easier Itanium® porting. To cut costs, many ISVs made minimal ports, not fully optimizing their products for the architecture, aiming to list Itanium® versions faster at less cost. However, many of these minimal application ports ran poorly, further hurting the platform's software performance reputation.

Intel and HP (*from around 2004*), with their ISA partners (*from 2006*), made large investments and major efforts to cajole and help ISVs port to HP Integrity (*far dominant Itanium®*) hardware. Strong arm-twisting, large funds, free hardware, porting centers, technical assistance, boot camps, beer and such lubricants, gradually increased the software portfolio.

So surely, by Q2 2009, the years-long Itanium® ISV software famine is now over? A recent Q1 2009 ISA presentation gave the number of Itanium® platform applications as 14,000! The ISA's Web site currently claims "more than 13,000" applications are now available for Itanium® MPU systems, in these words. (*Source 21, page 76, 16.4.2009*):

*"Itanium® Applications: The Itanium® Applications List provides a comprehensive listing of the more than 13,000 Itanium®-based applications currently available for both industry and customer use."*

The ISA's site hosts an impressive-looking, 653-page online PDF table, with 51 product line entries/page. This table thus holds 33,275 product-line entries, over two-and-a-half times the ISA's "13,000 applications" claimed. Hmmm... not like the ISA to under-report anything favorable to their beloved MPU, we thought; and therefore looked closer. Each table line shows ISV firm name, software product name, ISV product version, product status, operating system family, and OS version, supported. For many individual ISV products, a ludicrous up to 50 table line-entries show every offered combination of vendor product version(s), availability status, OS family, OS flavor and release number.



We sample-counted all the entries on 40 full pages of this ISA table. Those page's 2,040 product line entries actually described 489 different real applications. On that sample's ratio, the **ISA's 33,275-line table would contain 7,976 different products, not the 13,000 (or is it 14,000) the ISA claims; a 62.9% overstatement.** Double or triple counting of different OS, OS versions, and/or product releases, of the same real application, is the cause. This is not marketing finesse, those 13,000-14,000 applications Club Itanium claims were blatantly exaggerated!.

No doubt ISA computed those headline numbers thus so that Itanium® could claim it hosted closely-comparable headline numbers to the 12-15,000 applications that leading RISC-UNIX platform vendors (*IBM & Sun*) typically cited for their UNIX servers under Solaris (*Sun*) and AIX & Linux (*IBM*). What a coincidence!

By operating system, HP-UX line-entries were 36.3% of the total table, Linux 36.4%, OpenVMS 15.0%, and Windows 12%, of the total. But for Windows, for example, only 6.9% of all Windows line-entries were products running on the currently still-sold Microsoft Itanium® OS version, Windows Server 2008 for Itanium®-based Systems, so the real Windows applications choice for a new system buyer are a small fraction of the listed total. By the above breakdown ratio, we estimate c. 2,896 different real applications may be offered for HP-UX, the dominant operating system for HP Integrity, far below the numbers claimed for Sun SPARC (*Solaris*) or IBM Power Systems™ (*AIX/Linux/i*).

Another small example of how unreliable the ISA's Itanium® applications table is, we even noted 20 line-entries for products it stated to run under the Tru-64 UNIX OS. The only trouble is that Tru-64 UNIX was never production-released for an Itanium® platform, so how can any applications on this OS fairly be counted? More Club Itanium magic, or just plain tragic? Compaq had been working on a Tru-64 UNIX to Itanium® port before HP's acquisition, but this fell by the wayside in the new hands.

Despite our critique above, a quite substantial portfolio of ISV offerings covering many needs is clearly now available on the HP Integrity platform. However, it is unclear what proportion are fully optimized to best exploit the unique and different Itanium® Architecture. No quality control process, or branded assurance stamp of approval, exists to verify best Itanium® implementation practice has been followed for this listed software, so "caveat emptor" is advised.

Prospective Itanium® platform adopters should therefore exercise extreme caution, and should carefully check out the real availability, and the port/version quality, of every item of ISV software they need in detail.

## 2. Itanium® Systems Revenue – Portrayed as Far Above Real \$B Number

For enterprises considering purchase of Itanium®-based systems (*HP Integrity*), the fourth-ranking enterprise MPU platform, knowing what total system revenue the platform really won over recent years is a crucial, decision-influencing metric. Enterprise users evaluating such investment want an accurate view of how widely the market adopted the platform they are considering, measured by platform revenues in recent years. All the more important that accurate dates on this crucial metric should therefore be presented.

Major server market analyses from both main providers – IDC and Gartner – use net factory-gate server hardware revenue metrics to measure real server hardware revenues to vendors on a consistent, comparable, stable measure over time, over platforms, and over geographies. Vendor formal accounts, annual reports and segment breakdowns, also often show accurate, validly-recognized system hardware revenues. By company law, the latter, if quoted, must be accurate.

Club Itanium stalwarts Intel, HP, and the ISA, each use similar (*Intel-origin*) bar charts purporting to show "total Itanium® platform/system revenue" steeply growing from 2002 to 2008. A recent Q1 2009 ISA version of this chart we assessed, for example, showed this metric at c. \$5.1B (2008), \$4.3B (2007), \$ 3.35B (2006), and \$2.20B (2005).

Gartner credited HP with selling 95% of all Itanium® units, and with winning 90%+ of Itanium® server revenue, in 2008, both figures on rising trends. HP's officially reported, total Itanium®-based systems revenues for its last three full FYs were actually \$2,795M, \$2,274M, and \$1,352M (*From HP 2008, 2007, 2006 10K Returns – accurate on pain of SEC sanctions*), showing slowing growth rates of 22.9%, 68.2%, and 80.3% respectively.

We adjusted these accurate HP Itanium® system revenues so as to compute total market Itanium® system revenues (*with other vendor's shares*). These put the **ISA Itanium® system revenues claimed above at 65%, 65%, and 110% higher than actual-HP-based market Itanium® system revenues** booked in those three years. (*Slightly different year periods are covered, calendar years for the ISA figures, and HP FYs for the HP data.*)

Some measure other than booked, net, current-year Itanium®-system hardware-only revenue was clearly used to construct the similar Club Itanium marketing charts. Whether the chart's originator(s) used list (*MSRP*) sales value (*not actual net after customer discounts and channel costs*), hardware system multi-year deal value (*purchase plus X years of support costs*), or total system (*not only hardware, but software, support and service*) revenue, or some other metric, to reach the totals presented in their charts remains unclear.

**Exaggeration, extreme marketing, or deception? Take your choice.** Seriously misleading to prospective customers for sure, painting an Itanium® servers market revenue picture 65-110% higher than the actuals.

## Appendix C: IBM Mainframe MPU & System Capacity Growth

The IBM System z mainframe underwent the most radical, extensive, and continuing transformation since 1994, when the first CMOS generation G1 S/390 systems were introduced. This dramatic transformation is illustrated by the soaring power of IBM mainframe uniprocessor, and top-end systems, shown in Figures C1 below. and C2 on page 75.

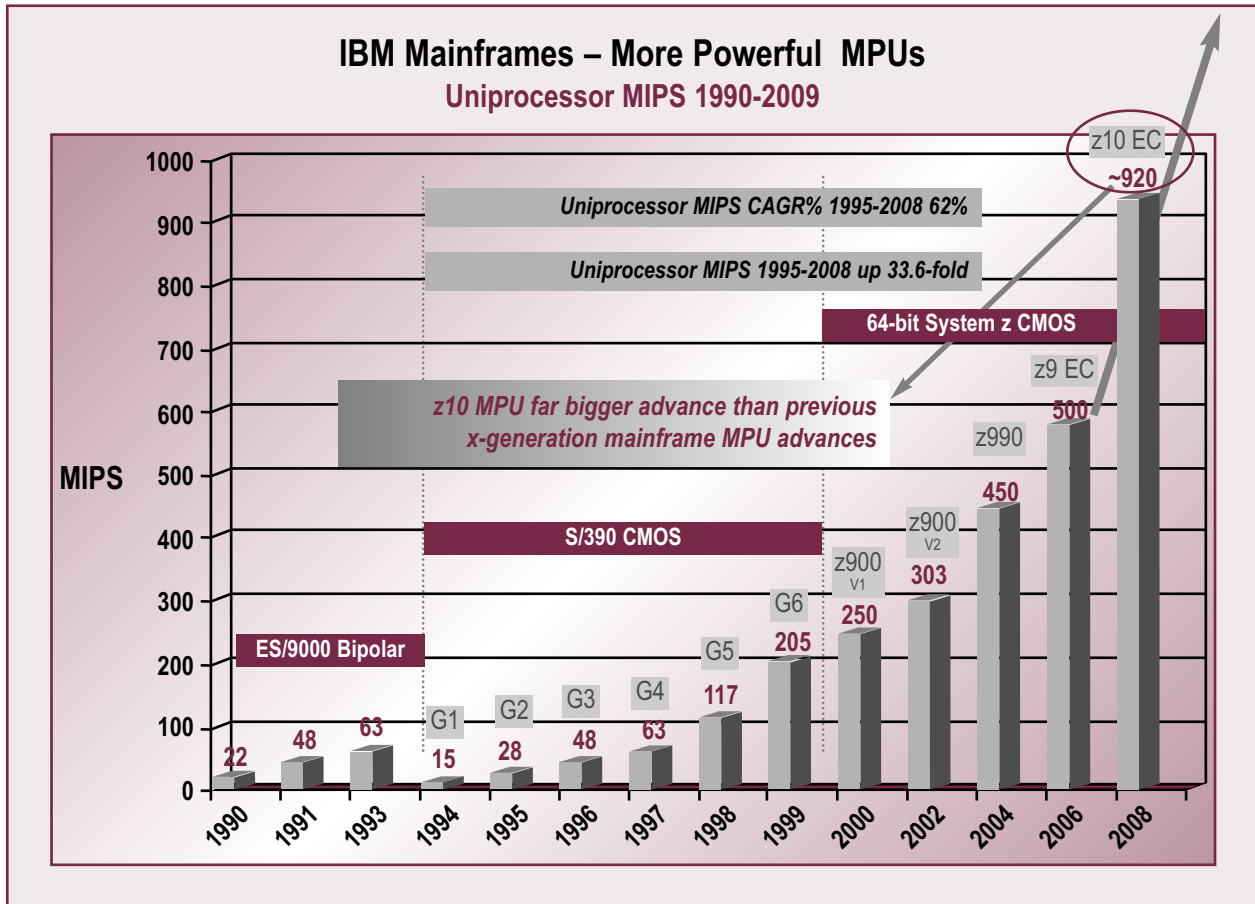


Figure C1: IBM Mainframe More Powerful MPUs – Uniprocessor MIPS 1990-2009

## IBM Mainframe – Maximum Capacity Rockets

### Maximum System MIPS 1990-2009

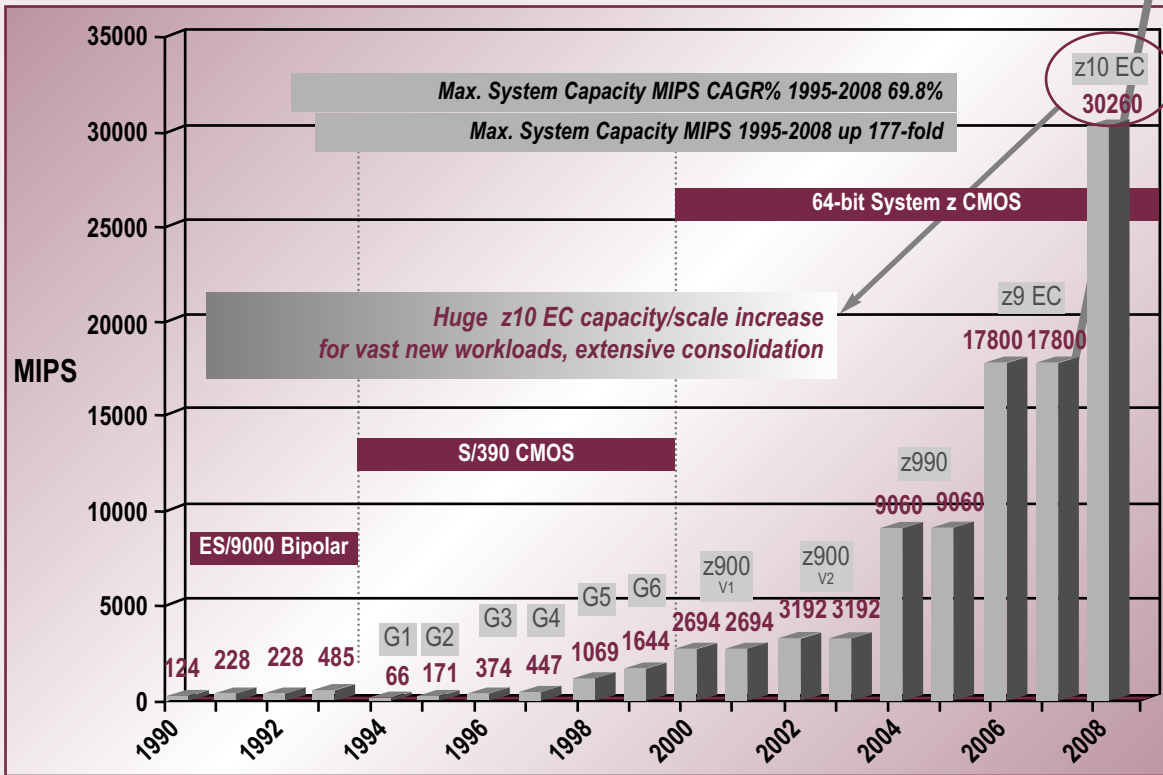


Figure C2: IBM Mainframe Maximum Capacity Rockets – Maximum System MIPS 1990-2009

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7. **“Mass Distributed Server Consolidation – System z Mainframe Linux-on-z/VM Extreme Virtualization far Outclasses Overhyped x86/x64 Approaches.”** White Paper, January 2008, 72 p.p., 27 charts/tables.
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9. **“New System z9 Mainframes Hit Mid-market, Refresh Top End – Powerful New SOA & Data-serving Software Delivers New Enterprise-wide Roles.”** White Paper, July 2006, 60 p.p., 21 charts/tables.
10. **“Spectacular System z9 Mainframes Leap Ahead with Doubled Power, Enterprise Hub Roles – Virtualization, Security, Availability, SOA & Value Advances.”** Enterprise Server Spotlight Report, September 2005, 72 p.p., 28 charts/tables.

## About Software Strategies

Software Strategies is a specialist analyst firm focused on enterprise IT platform strategies and issues. Specialist expertise on mainframes, servers, operating systems, and on middleware software/tools, have been our common threads. Since 1997, we have worked closely with numerous industry leaders, including: IBM; Unisys; Microsoft; Intel; Misys; Fidelity National Information Systems; CA; BMC; Stratus Computers; ICL; NetIQ; and others. Many tens of thousands of Enterprise IT user readers have benefited from our authoritative reports, white papers, and from our presentations at scores of IT events, seminars, and conferences.

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This new White Paper was researched/written by Ian Bramley, Managing Director of Software Strategies, and was published in June 2009. The views expressed are those of Software Strategies alone, and are based on our extensive proprietary mainframe and software research. Ian founded Software Strategies in 1997. He is an experienced enterprise infrastructure analyst, has published scores of popular reports and white papers, and has served as a keynote speaker at many industry events. Previously, he was Director of Enterprise Platforms at Butler Group, and Founder/Chairman of the Enterprise NT Management Forum industry group from 1998 to 2001. Before becoming an analyst, Ian held executive positions with four international software/services vendors over his prior 25-year IT industry career.

