Assessing zSeries & S/390 Processor Capacity

Washington Systems Center
Advanced Technical Support

LSPR Background

zSeries Capacity Planning

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Purpose
To demonstrate, through measurement, zSeries & S/390 processor capacity running various SCP's and associated workload environments

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Large Systems Performance Reference

Technical Bulletin SC28-1187 (available via Internet)

- Processor capacity planning background
- Metrics for expressing processor capacity
- zSeries & S/390 workload environments
- Using LSPR data
- Validating a new processor capacity expectation
- LSPR ITR ratios for zSeries processors

LSPR document and data from the Internet
LSPR Background

1. A set of representative SCP/workload environments
   - SCP's: z/OS, z/VM, and Linux
   - Workloads: Batch ← Online

2. A methodology that focuses on processor capacity
   - No significant external constraints
   - Equivalent (reasonably high) processor utilization

3. A metric to communicate the results
   - ITR (Internal Throughput Rate)
   - Transactions or Jobs per processor busy second
Focus is on processor capacity, without regard to

- External resources, including . . .
  - Central storage
  - Expanded storage
  - Channels
  - DASD devices
  - Operator activities

- Special features, such as . . .
  - Vector processing
  - ADMF
  - DB2 Sort Assist
  - Compression
  - Encryption

Capacity is represented by ITR values depicting each processor in its best light. Therefore, ratios between ITR values provide reasonable capacity relationships for capacity planning purposes.
The **LSPR** Advantage

**Workloads exploit**

- **SCP** (z/OS, z/VM, Linux, etc.)
  - JES2, VTAM, DFSMS, RACF, RMF/SMF
- **Application Subsystems**
  - CICS, DB2, IMS, WebSphere
- **Access Methods**
  - VSAM, RSAM, QSAM, BDAM
- **Program Products**
  - ASSEMBLER, COBOL, FORTRAN, PL/1
  - DFSORT, GDGMM, ISPF, PL/1, SLR, SCRIPT
- **Transactions / Jobs**
  - Includes a broad mix of activities
  - Realistic end-user / initiator count
  - Representative inter-arrival times
**LSPR Workloads**

**z/OS**
- **CB-L**  Commercial batch - long, CPU-intensive jobs
- **CB-S**  Commercial batch - short, I/O-intensive jobs
- **WASDB**  WebSphere applications and DB2 data base
- **OLTP-W**  Web enabled access to CICS/DB2 database
- **OLTP-T**  Traditional IMS Data Systems online workload

**z/VM**
- **CMS**  CMS interactive user workload
- **WASDB/LVm**  WebSphere under Linux as many small guests

**Linux**
- **WASDB/L**  WebSphere under Linux
- **EAS-AS/L**  SAP Application server
LSPR Capacity Metrics

- **ETR**
  - **External Throughput Rate**
  - Bears direct relationship to work done
  - Computed as work ÷ elapsed time
  - Characterizes capacity of the entire processing system

- **ITR**
  - **Internal Throughput Rate**
  - Bears direct relationship to work done
  - Computed as work done ÷ processor busy time
  - Characterizes capacity of the processor itself

- **ITRR**
  - **Internal Throughput Rate Ratio**
  - Statement of one processor's capacity relative to another
  - The LSPR bottom-line
System #1: "the better system"

1650 Seconds
Elapsed Time

Processor Time
990 Seconds (60%)

Wait Time
Work, Storage, I/O

System #2: "the better processor"

2000 Seconds
Elapsed Time

Processor Time
800 Seconds (40%)

Wait Time
Work, Storage, I/O
Provides a methodology for comparing **System Capacity**

- System is measured at/near a fully-loaded operating level
- Any resource is a potential capacity inhibitor, including
  - Central Processor
  - Memory (C-store and E-store)
  - Channels, CU's and I/O devices
  - TP network
  - Operator actions
- A response time criteria is commonly used to define when the system is saturated

**ETR**

*External Throughput Rate*

Actual work done ÷ elapsed time
Actual Work Done ÷ Processor Busy Time

Provides a methodology for comparing **Processor Capacity**

- Processor is the only capacity inhibitor
  - Resources such as memory, channels, DASD, etc., are adequate to support the workload being measured
  - Minimal CPU is consumed managing resource constraints
- Processors are measured at equal utilization
- Processors are measured at reasonably high utilization
  - Batch is measured (start to end) at/near 100% utilization
  - Online is measured (steady-state) at 90% utilization
**ITR / ETR Relationship**

Utilization = \( \frac{\text{Processor Busy Time}}{\text{Elapsed Time}} \)

ETR = \( \frac{\text{Units-of-Work}}{\text{Elapsed Time}} \)

ITR = \( \frac{\text{Units-of-Work}}{\text{Processor Busy Time}} \) = ETR / Utilization

*Assessing zSeries & S/390 Processor Capacity*
LSPR Measurement Example

Measurement Steps

1. Approximate user count to achieve target processor utilization
2. Setup system and restore data to startup condition
3. Logon estimated number of users (staggered over time)
4. Add/drop users to achieve target processor utilization
5. Allow system to achieve steady state
6. Measure for period deemed to be a repeatable sample
7. Analyze monitor data for problems/bottlenecks
## LSPR Measurement Example

**z/OS with OLTP-W**

<table>
<thead>
<tr>
<th>Measured data</th>
<th>2064-2C2</th>
<th>2064-2C4</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elapsed seconds</td>
<td>1,201.30</td>
<td>900.78</td>
<td></td>
</tr>
<tr>
<td>Processor seconds</td>
<td>1,072.16</td>
<td>828.63</td>
<td></td>
</tr>
<tr>
<td>Transaction count</td>
<td>201,374</td>
<td>298,609</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Calculated data</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Utilization</td>
<td>89.25 %</td>
<td>91.99 %</td>
<td></td>
</tr>
<tr>
<td>ETR</td>
<td>167.630</td>
<td>331.500</td>
<td>1.98</td>
</tr>
<tr>
<td>ITR</td>
<td>187.821</td>
<td>360.365</td>
<td>1.92</td>
</tr>
</tbody>
</table>
### Absolute ITR Values

**z/OS LSPR Workloads as of 05/13/2003**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Features</th>
<th>CB-L</th>
<th>CB-S</th>
<th>WASDB</th>
<th>OLTP-W</th>
<th>OLTP-T</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>zSeries 900 Turbo</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2064-2C1</td>
<td>1W</td>
<td>0.12748</td>
<td>3.92286</td>
<td>253.601</td>
<td>97.610</td>
<td>196.468</td>
</tr>
<tr>
<td><strong>2064-2C2</strong></td>
<td>2W</td>
<td>0.25277</td>
<td>7.06646</td>
<td>489.024</td>
<td>187.821</td>
<td>377.053</td>
</tr>
<tr>
<td>2064-2C3</td>
<td>3W</td>
<td>0.37557</td>
<td>10.07036</td>
<td>720.555</td>
<td>275.406</td>
<td>549.791</td>
</tr>
<tr>
<td><strong>2064-2C4</strong></td>
<td>4W</td>
<td>0.49588</td>
<td>12.93456</td>
<td>948.196</td>
<td>360.365</td>
<td>714.681</td>
</tr>
<tr>
<td>2064-2C5</td>
<td>5W</td>
<td>0.61371</td>
<td>15.65907</td>
<td>1,171.945</td>
<td>442.700</td>
<td>871.725</td>
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<tr>
<td>2064-2C6</td>
<td>6W</td>
<td>0.72906</td>
<td>18.24387</td>
<td>1,391.804</td>
<td>522.408</td>
<td>1,020.921</td>
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<tr>
<td>2064-2C7</td>
<td>7W</td>
<td>0.84192</td>
<td>20.68898</td>
<td>1,607.771</td>
<td>599.492</td>
<td>1,162.271</td>
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<td>2064-2C8</td>
<td>8W</td>
<td>0.95230</td>
<td>22.99439</td>
<td>1,819.847</td>
<td>673.950</td>
<td>1,295.774</td>
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<td>2064-2C9</td>
<td>9W</td>
<td>1.06019</td>
<td>25.16010</td>
<td>2,028.032</td>
<td>745.783</td>
<td>1,421.429</td>
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<tr>
<td>2064-210</td>
<td>10W</td>
<td>1.16559</td>
<td>27.18611</td>
<td>2,232.326</td>
<td>814.990</td>
<td>1,539.238</td>
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<tr>
<td>2064-211</td>
<td>11W</td>
<td>1.26851</td>
<td>29.07243</td>
<td>2,432.729</td>
<td>881.572</td>
<td>1,649.200</td>
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<tr>
<td>2064-212</td>
<td>12W</td>
<td>1.36895</td>
<td>30.81905</td>
<td>2,629.240</td>
<td>945.528</td>
<td>1,751.314</td>
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<tr>
<td>2064-213</td>
<td>13W</td>
<td>1.46690</td>
<td>32.42597</td>
<td>2,821.861</td>
<td>1,006.859</td>
<td>1,845.582</td>
</tr>
<tr>
<td>2064-214</td>
<td>14W</td>
<td>1.56236</td>
<td>33.89319</td>
<td>3,010.590</td>
<td>1,065.565</td>
<td>1,932.003</td>
</tr>
<tr>
<td>2064-215</td>
<td>15W</td>
<td>1.65535</td>
<td>35.22071</td>
<td>3,195.428</td>
<td>1,121.645</td>
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<tr>
<td><strong>2064-216</strong></td>
<td>16W</td>
<td>1.74584</td>
<td>36.40854</td>
<td>3,376.375</td>
<td>1,175.100</td>
<td>2,081.304</td>
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<tr>
<td><strong>zSeries 990</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2084-301</td>
<td>1W</td>
<td>0.20000</td>
<td>6.17591</td>
<td>408.637</td>
<td>153.050</td>
<td>303.443</td>
</tr>
<tr>
<td>2084-302</td>
<td>2W</td>
<td>0.38975</td>
<td>11.08934</td>
<td>777.099</td>
<td>294.670</td>
<td>582.525</td>
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<tr>
<td>2084-303</td>
<td>3W</td>
<td>0.57570</td>
<td>15.77285</td>
<td>1,138.765</td>
<td>431.510</td>
<td>849.637</td>
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<tr>
<td>2084-304</td>
<td>4W</td>
<td>0.75784</td>
<td>20.22642</td>
<td>1,493.636</td>
<td>563.569</td>
<td>1,104.779</td>
</tr>
<tr>
<td>2084-305</td>
<td>5W</td>
<td>0.93617</td>
<td>24.45007</td>
<td>1,841.710</td>
<td>690.847</td>
<td>1,347.950</td>
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<tr>
<td>2084-306</td>
<td>6W</td>
<td>1.11069</td>
<td>28.44378</td>
<td>2,182.989</td>
<td>813.345</td>
<td>1,579.151</td>
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<tr>
<td>2084-307</td>
<td>7W</td>
<td>1.28140</td>
<td>32.20757</td>
<td>2,517.471</td>
<td>931.063</td>
<td>1,798.381</td>
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<tr>
<td>2084-308</td>
<td>8W</td>
<td>1.44831</td>
<td>35.74142</td>
<td>2,845.158</td>
<td>1,044.000</td>
<td>2,005.640</td>
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<tr>
<td><strong>2084-309</strong></td>
<td>9W</td>
<td>1.61141</td>
<td>39.04535</td>
<td>3,166.049</td>
<td>1,152.157</td>
<td>2,200.929</td>
</tr>
</tbody>
</table>
How **LSPR** Data Can Be Used

1. **Determine relative capacity** for a potential new processor, to that of a currently installed processor, based on the SCP/workload environment

2. **Scale relative capacity** to any single processor's assumed (**MIPS**) rating (generally the currently installed processor would be used)

3. **Define a mix of workloads** to represent the current production workload, providing a tailored capacity expectation for potential new processors

4. **Predict processor life** assuming workload growth rates for each of the various production workload components

5. **Assess capacity for workload consolidation** when planning to merge various workload components running on different processors onto a single processor

6. **Analyze workload metrics** for the LSPR workloads and assesses the effects of changing them (e.g.; CPU intensity and inter-arrival time) on the number of users that could be supported.
Developing an **LSPR** Mixed-Workload Capacity Relationship

Formula to compute LSPR capacity ratio for a mixed-workload

A *Harmonic Mean* calculation

\[
\frac{1}{\left( \frac{\% \text{ CB-L}}{\text{CB-L ITRR}} + \frac{\% \text{ CB-S}}{\text{CB-S ITRR}} + \frac{\% \text{ WASDB}}{\text{WASDB ITRR}} + \frac{\% \text{ OLTP-W}}{\text{OLTP-W ITRR}} + \frac{\% \text{ OLTP-T}}{\text{OLTP-T ITRR}} \right)}
\]
**Mainframe Capacity Growth**

Maximum Capacity for a Single OS Image
MIPS rating for Average Workload (LSPR-Mix)

- **Processor Generation**
  - H5
  - G1
  - G2
  - G3
  - G4
  - G5

<table>
<thead>
<tr>
<th>Code</th>
<th>Biploar</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>H5</td>
<td>510</td>
<td></td>
</tr>
<tr>
<td>G1</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>176</td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>405</td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>506</td>
<td></td>
</tr>
<tr>
<td>G5</td>
<td></td>
<td>1183</td>
</tr>
</tbody>
</table>

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**Assessing zSeries & S/390 Processor Capacity**

*CPSTools - 03/2004*
Mainframe Capacity Growth
Maximum Capacity for a Single OS Image
MIPS rating for Average Workload (LSPR-Mix)

Processor Generation

<table>
<thead>
<tr>
<th>Generation</th>
<th>Biploar</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>H5</td>
<td>510</td>
<td></td>
</tr>
<tr>
<td>G1</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>176</td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>405</td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>506</td>
<td></td>
</tr>
<tr>
<td>G5</td>
<td>1,183</td>
<td>1,779</td>
</tr>
<tr>
<td>G6</td>
<td></td>
<td>3,401</td>
</tr>
<tr>
<td>Z900</td>
<td></td>
<td>5,208</td>
</tr>
<tr>
<td>Z990</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Changes across IBM Processor Families that Affect Capacity

<table>
<thead>
<tr>
<th>Bipolar</th>
<th>CMOS</th>
<th>G5</th>
<th>z990</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>H5</strong></td>
<td><strong>G4</strong></td>
<td>Faster cycle time</td>
<td>Faster cycle time</td>
</tr>
<tr>
<td>Slow cycle time</td>
<td>Fast cycle time</td>
<td>More hardware logic</td>
<td>More hardware logic</td>
</tr>
<tr>
<td>Complex hardware logic</td>
<td>Hardware / uCode logic</td>
<td>G4 plus ...</td>
<td>G5 plus ...</td>
</tr>
<tr>
<td>Super scalar</td>
<td>Sequential decode</td>
<td>More sophisticated HSB</td>
<td>Super scalar</td>
</tr>
<tr>
<td>Branch history table</td>
<td>In-order execution</td>
<td>L1 - 256KB</td>
<td>Multiple inst per cycle</td>
</tr>
<tr>
<td>Instruction prefetch</td>
<td>High speed circuits</td>
<td>L2 - 2x4MB private</td>
<td>2nd level TLB</td>
</tr>
<tr>
<td>Multiple decode</td>
<td>High speed buffer</td>
<td></td>
<td>64-bit addressing</td>
</tr>
<tr>
<td>Multile E-units</td>
<td>L1 - 64KB</td>
<td></td>
<td>Up to 4 books (32 CPs)</td>
</tr>
<tr>
<td>Out-of-order execution</td>
<td>L2 - 4x768KB private</td>
<td></td>
<td>More sophisticated HSB</td>
</tr>
<tr>
<td>High speed buffer</td>
<td>L2.5 - 2MB</td>
<td>L1 - per CP</td>
<td></td>
</tr>
<tr>
<td>L1 - 2x128KB</td>
<td></td>
<td>256KB instruction</td>
<td></td>
</tr>
<tr>
<td>L2 - 2x4MB shared</td>
<td></td>
<td>256KB data</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>L2 - per book</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>32MB shared</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LPAR-mode only</td>
<td></td>
</tr>
</tbody>
</table>

**zSeries Capacity Planning**

**CPSTools - 03/2004**
**MIPS as a Processor Metric**

- **Millions of Instructions Per Second**
- Meaningless Indicator of Performance
- A *ball-park* (average) indicator of processor capacity
- No correlation to actual instruction rate
- Implies some type of *universal scale*, loosely associated with actual Instruction Execution Rate (*IER*)
- A *single-number metric*, which is insensitive to workload

Capacity is dependent on workload type and partition configuration

Actual capacity can vary +/- 20% or more from relationships determined via MIPS tables
### MIPS Table

#### Relative Capacity

**10-Way Processors**

<table>
<thead>
<tr>
<th>Processor</th>
<th>MIPS (Thousands)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9672-RY5</td>
<td>446</td>
</tr>
<tr>
<td>9672-YX6</td>
<td>1,069</td>
</tr>
<tr>
<td>9672-ZX7</td>
<td>1,427</td>
</tr>
<tr>
<td>2064-210</td>
<td>2,287</td>
</tr>
<tr>
<td>2084-310</td>
<td>3,596</td>
</tr>
</tbody>
</table>

**MIPS Table**

- **Consultant MIPS**

**zSeries Capacity Planning**

CPSTools - 03/2004
Assessing zSeries & S/390 Processor Capacity

Relative Capacity
10-Way Processors
z/OS V1R4

LSPR

CB-L  CB-S  WASDB  OLTP-W  OLTP-T

MIPS (Thousands)

Relative Capacity

9672-RY5  9672-YX6  9672-ZX7  2064-210  2084-310

G4  G5  G6  z900  z990

zSeries Capacity Planning  CPSTools - 03/2004
Relative Capacity
1-Way Processors
z/OS V1R4

- CB-L
- CB-S
- WASDB
- OLTP-W
- OLTP-T

MIPS

Relative Capacity

G4  G5  G6  z900  z990

9672-R15  9672-R16  9672-Z17  2064-2C1  2084-301
Factors That Affect Processor Capacity Relationships

Architecture

*zArchitecture* (including *S/390*)
The only architecture covered by LSPR

Hardware Design

Each *zArchitecture* (*S/390*) processor family has its own unique internal design
Factors That Affect Processor Capacity Relationships

**Hardware**

- Basic processor cycle time
- OPCODE efficiency
- High Speed Buffer (HSB) design
- Multi-Processor (N-way) efficiency
- Special hardware / microcode features
Factors That Affect Processor Capacity Relationships

Software

- CPU time per transaction / job
- % Supervisor or % Problem state
- I/O rate per second or per unit-of-work
- Working set size
- Etc . . .
Factors That Affect Processor Capacity Relationships

Software

- Instruction set usage
  - OPCODE frequency and sequencing
- Storage reference patterns
- Dispatch rate
- Use of special features
## Factors That Affect Processor Capacity Relationships

### Software
- Instruction set usage
- Storage reference patterns
- Dispatch rate
- Use of special features

Varies by:
- SCP/workload environment

### Hardware
- OPCODE efficiency
- HSB design
- N-way efficiency
- Special hardware / microcode

Varies by:
- Processor family design
Relative Capacity
1-Way Processors
OS/390 V2R10

LSPR

G5 Relative Cycle Time

CBW2  CB84  TSO  CI/DB2  IMS

G4  G5

9672-R15  9672-R16

1.35

Assessing zSeries & S/390 Processor Capacity
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Relative Capacity
10-Way Processors
OS/390 V2R10

- CBW2
- CB84
- TSO
- CI/DB2
- IMS

G5 Relative Cycle Time
1.35

G5
G4

9672-RY5
9672-RX6

zSeries Capacity Planning

CPSTools - 03/2004
High Speed Buffer Effect
3090-180J vs 3090-180S

Relative Capacity

FPC1  CBW2  CB84  TSO  CICS  DB2  IMS

180S (HSB = 128K)  180J (HSB = 256K)
High Speed Buffer Effect
3090-600J vs 3090-600S

Relative Capacity

FPC1  CBW2  CB84  TSO  CICS  DB2  IMS

600S (HSB = 128K)  600J (HSB = 256K)
Assessing zSeries & S/390 Processor Capacity

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N-Way Efficiency
G4 (CMOS)
OS/390 V1R1

Relative Capacity

1 2 3 4 5 6 7 8 9 10

Number of CPs

1 2 3 4 5 6 7 8 9 10

CBW2
CB84
TSO
CICS
DB2
IMS
Assessing zSeries & S/390 Processor Capacity

LSPR

N-Way Efficiency
G6 (CMOS)
OS/390 V2R4

Relative Capacity
10
9
8
7
6
5
4
3
2
1

Number of CPs
1
2
3
4
5
6
7
8
9
10

- CBW2
- CB84
- TSO
- CI/DB2
- IMS
 Assessing zSeries & S/390 Processor Capacity

N-Way Efficiency
z990 (CMOS)
z/OS V1R4

Relative Capacity

Number of CPs

CBW2
CB-S
WASDB
OLTP-W
OLTP-T

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Factors Affecting Processor Capacity Relationships

Any given zArchitecture (or S/390) processor's capacity and performance potential is dependent on . . .

- that processor's underlying design
- how the SCP/workload environment interacts with that design
# Scope of DP Workloads

<table>
<thead>
<tr>
<th>BATCH</th>
<th>ONLINE</th>
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<tbody>
<tr>
<td>JOB or JOB-STEP</td>
<td>Unit of Work</td>
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<tr>
<td>VERY LARGE</td>
<td>CPU Time per Dispatch</td>
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<td>LOWER</td>
<td>I/O Intensity</td>
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<td>INFREQUENT</td>
<td>Supervisor Services Requests</td>
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<td>VERY LOW</td>
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<td>LOW</td>
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<td>VERY EFFICIENT</td>
<td>N-Way Exploitation</td>
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<tr>
<td>NOT DOMINANT</td>
<td>PRIVOPs and Branching</td>
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<td>Storage Reference Patterns</td>
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<tr>
<td>VERY HIGH</td>
<td>High Speed Buffer Hit Ratio</td>
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<td>DOMINANT</td>
<td>RANDOM</td>
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<tr>
<td>LESS EFFICIENT</td>
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<td>VERY SMALL</td>
<td>HIGHER</td>
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<td>FREQUENT</td>
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<tr>
<td>RELATIVELY HIGH</td>
<td>HIGH</td>
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<tr>
<td>RANDOM</td>
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</tbody>
</table>

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Scope of **LSPR** Workloads

**BATCH**
- JOB or JOB-STEP

**ONLINE**
- TRANSACTION

**z/OS:**
- CB-L
- WASDB
- OLTP-W
- OLTP-T
- CB-S

**z/VM:**
- WASDB/LVm
- CMS

**Linux:**
- EAS-AS/L
- WASDB/L
How Do I Relate My Workload to LSPR?

Some general considerations

- Never focus solely on the LSPR workload that provides the best-case capacity relationship
- Always be aware of the LSPR workload with the worst-case capacity relationship
- For batch, don't use CB-L or CB-S independently without a specific reason; start with a mix of ¾ CB-L and ¼ CB-S
- For online workloads, factor in some CB-L when transactions are more than trivial (normally the case for today's environments)
- Capacity ratios are particularly sensitive to workload when G1 - G4 is involved as the "from" processor. Also, when z990 is "to" processor.
- Request help from IBM to determine which LSPR workload primitives should be considered, and how to best interpret resulting capacity relationships
- Use the predefined workload mixes available in zPCR and PCRW tools
Scope of **LSPR** Workloads

**BATCH**

- JOB or JOB-STEP

**ONLINE**

- TRANSACTION

**z/OS Mixes:**

- LoIO-Mix
- TM-Mix
- TD-Mix
- TI-Mix

**CB Mixes:**

- CB-L
- CB-MIx
- CB-S
General Capacity Observations

Workload Component vs Overall Workload
(An Example: "B" = 2.0 x "A")
General Capacity Observations

Processor Loading
Effect on Job or Transaction TCB Time

Perceived as Less Capacity
Perceived as More Capacity

Relative TCB Time

Daytime
Nighttime

zSeries Capacity Planning

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Assessing Processor Capacity

Accuracy vs Cost

Highest

Customized Benchmark

Accuracy

LSPR
Benchmarks

MIPS
Tables

Lower

Cost associated with making a processor decision

$$$$$$$