Processor Capacity Planning:

LSPR Workload Sensitivities
Processor Performance: Most Influential Factors

- Processor Design
  - Cycle time
  - Memory subsystem
    - high speed buffer (HSB)
    - latency
    - bandwidth
  - Logic
    - hardware vs. millicode
    - execution order
    - branch prediction
    - special features
  - Number of engines

- Workload Characteristics
  - Reference pattern
    - transaction size
    - I/O rate
    - multiprogramming level
  - Code
    - instruction mix
    - instruction sequence
    - branch characteristics
  - Common tasks/functions
  - LPAR Configuration
Processor Performance Example: Cycle Time Change

- **RX5**
  - Cycle time: 3.1 ns
  - Memory subsystem: same
  - Logic: same
  - Number of engines: same

- **RY5**
  - Cycle time: 2.7 ns
  - Memory subsystem: same
  - Logic: same
  - Number of engines: same
Processor Performance Example: Memory Subsystem Change

- **RY5**
  - Cycle time: 2.7 ns
  - L1: 64k
  - L2: 768k / 3CPs non-shared
  - L3: cross-point switch design

- **RX6**
  - Cycle time: 2.4 ns
  - L1: 256k
  - L2: 4mb / side non-shared
  - L3: storage controller design
  - Logic improvements
    - more hardware
    - branch history table
Workload<->Memory Subsystem Effects

MIPS versus i/L1 miss by LSPR workload
10way Processors

Instructions per L1 miss

MIPS

G3
G4
G5
H5
Workload<->Memory Subsystem Effects

MIPS versus i/L2 miss by LSPR workload
10way Processors
Processor Performance Example: Logic Change

- **9X2**
  - Cycle time: 7.1 ns
  - L1: 128k i and 128k d
  - L2: 4mb / side shared
  - L3: storage controller design
  - multiple decode, prefetch
  - sophisticated branch history

- **RY5**
  - Cycle time: 2.7 ns
  - L1: 64k
  - L2: 768k / 3 CPs non-shared
  - L3: cross-point switch design
  - sequential decode
  - millicode
Processor Performance Example: Number of engines change

- **R55**
  - Cycle time: same
  - Memory subsystem: same
  - Logic: same
  - Number of engines: 5

- **R75**
  - Cycle time: same
  - Memory subsystem: same
  - Logic: same
  - Number of engines: 7
## Processor Design Comparison

<table>
<thead>
<tr>
<th></th>
<th>Cycle Time</th>
<th>L1</th>
<th>L2</th>
<th>L2.5</th>
<th>L3 Access</th>
<th>Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>G2</td>
<td>12</td>
<td>16k</td>
<td>384k/CP non-shr</td>
<td>-</td>
<td>xpt-switch</td>
<td>millicode + hardware</td>
</tr>
<tr>
<td>G3</td>
<td>6.5,5.9</td>
<td>32k</td>
<td>256k/CP non-shr</td>
<td>2mb</td>
<td>xpt-switch</td>
<td>millicode + hardware</td>
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<tr>
<td>G4</td>
<td>3.3,3.1,2.7</td>
<td>64k</td>
<td>768k/3CP non-shr</td>
<td>2mb</td>
<td>xpt-switch</td>
<td>millicode + hardware</td>
</tr>
<tr>
<td>G5</td>
<td>2.4,2.0</td>
<td>256k</td>
<td>4mb/side non-shr</td>
<td>-</td>
<td>stg-cntlr</td>
<td>more hdw branchn hst</td>
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<tr>
<td>H5</td>
<td>7.1</td>
<td>128k i 128k d</td>
<td>4mb/side shared</td>
<td>-</td>
<td>stg-cntlr</td>
<td>multi-decode ++ branchn hst</td>
</tr>
</tbody>
</table>
Upgrade to Next CMOS Generation

G2 to G3
RX3 to R54

G2 to G3
RX3 to RX4
Upgrade to Next CMOS Generation

G3 to G4
R54 to R55

LSPR Workload

G3 to G4
R54 to RX5

LSPR Workload

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1
Upgrade to Next CMOS Generation

G4 to G5
RX5 to R56

G4 to G5
RX5 to RX6

LSPR Workload

Capacity Ratio

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1

LSPR Workload

Capacity Ratio
Upgrade Bipolar to CMOS

H5 to G4
952 to R55

H5 to G4
952 to RX5

Capacity Ratio

LSPR Workload

Capacity Ratio

LSPR Workload

TSO
CICS
DB2
IMSDS
CB84
MIX
CBW2
FPC1
Upgrade Bipolar to CMOS

H5 to G5
9X2 to R56

H5 to G5
9X2 to RX6

LSPR Workload
Upgrade Number of Engines

G4
R55 to R75

G4
R55 to RX5

LSPR Workload

Capacity Ratio

0 0.5 1 1.5 2

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1

LSPR Workload

Capacity Ratio

0 0.5 1 1.5 2

TSO  CICS  DB2  IMSDS  CB84  MIX  CBW2  FPC1
LSPR Workload Capacity Ratios: Sensitive to type of upgrade

- Add engines within processor family
  - Generally similar ratios
  - Memory-subsystem-light workloads can have slightly higher ratios
- Majority of improvement from cycle time reduction
  - Generally similar ratios
  - Memory-subsystem-light workloads can have higher ratios
- Majority of improvement from enhanced memory subsystem
  - Wide range in ratios
  - Memory-subsystem-light workloads will have lower ratios
- Majority of improvement from logic enhancements
  - Likely to be somewhat variable
- Balanced improvements in all areas
  - Generally similar ratios
## Current and Future Upgrade Sensitivities

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
<th>Major Difference(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H5</td>
<td>G5, G6</td>
<td>cycle time, mem-subsys+, logic</td>
</tr>
<tr>
<td>G4</td>
<td>G5, ..., G6, G7</td>
<td>memory-subsystem+++</td>
</tr>
<tr>
<td>G5</td>
<td>G6</td>
<td>cycle time</td>
</tr>
<tr>
<td>G6</td>
<td>G7</td>
<td>cycle time, mem-subsys, logic</td>
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