CICS V5 Performance

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CICS TS for z/OS Performance Test Lead

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April 27 – May 1 | The Venetian – Las Vegas, NV

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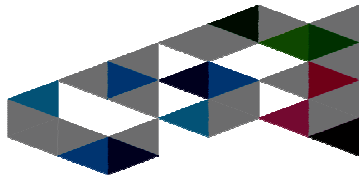
Performance is based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput or performance that any user will experience will vary depending upon many factors, including considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed. Therefore, no assurance can be given that an individual user will achieve results similar to those stated here.



Agenda

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Release-Release (V5.1)

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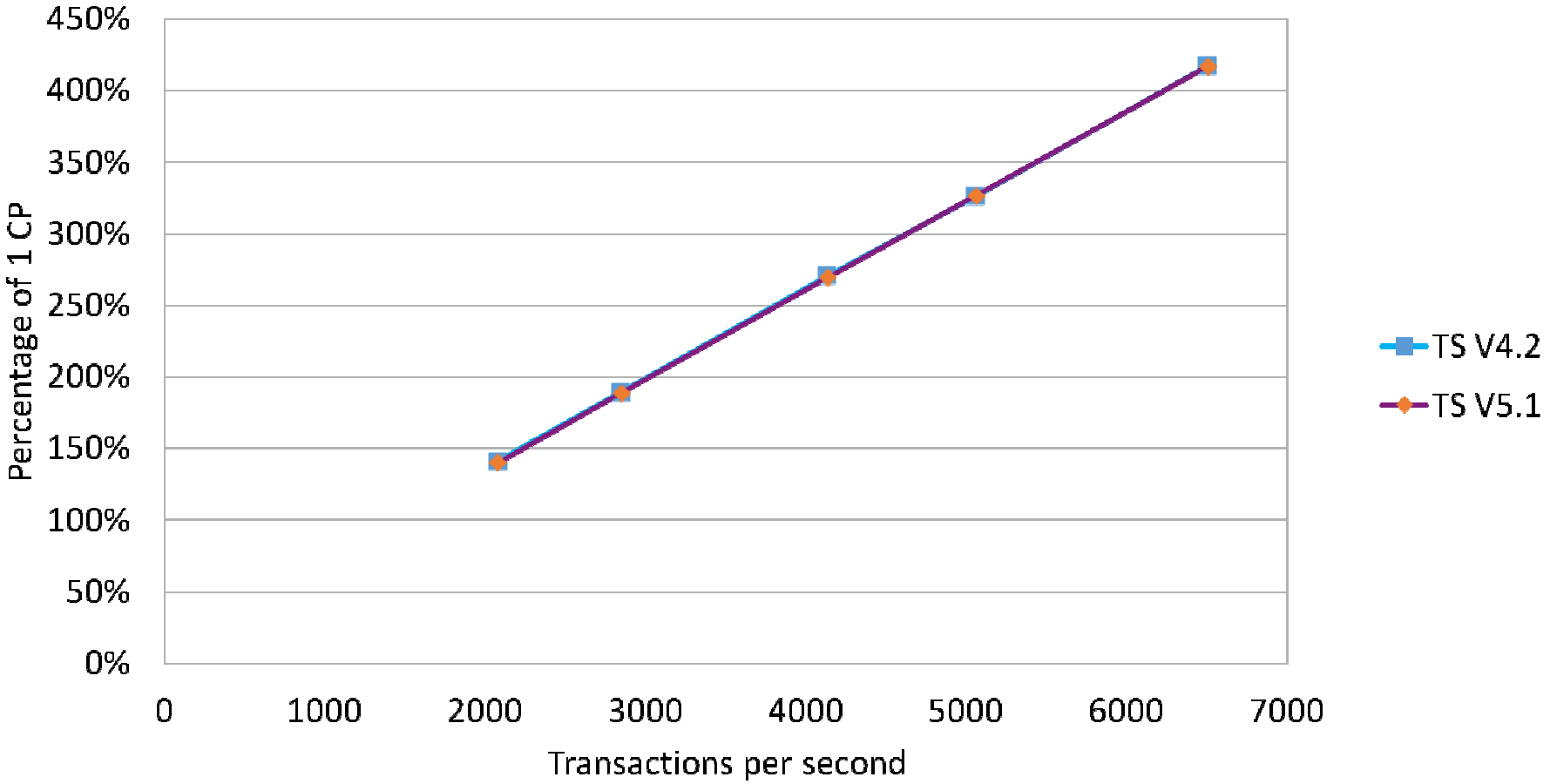
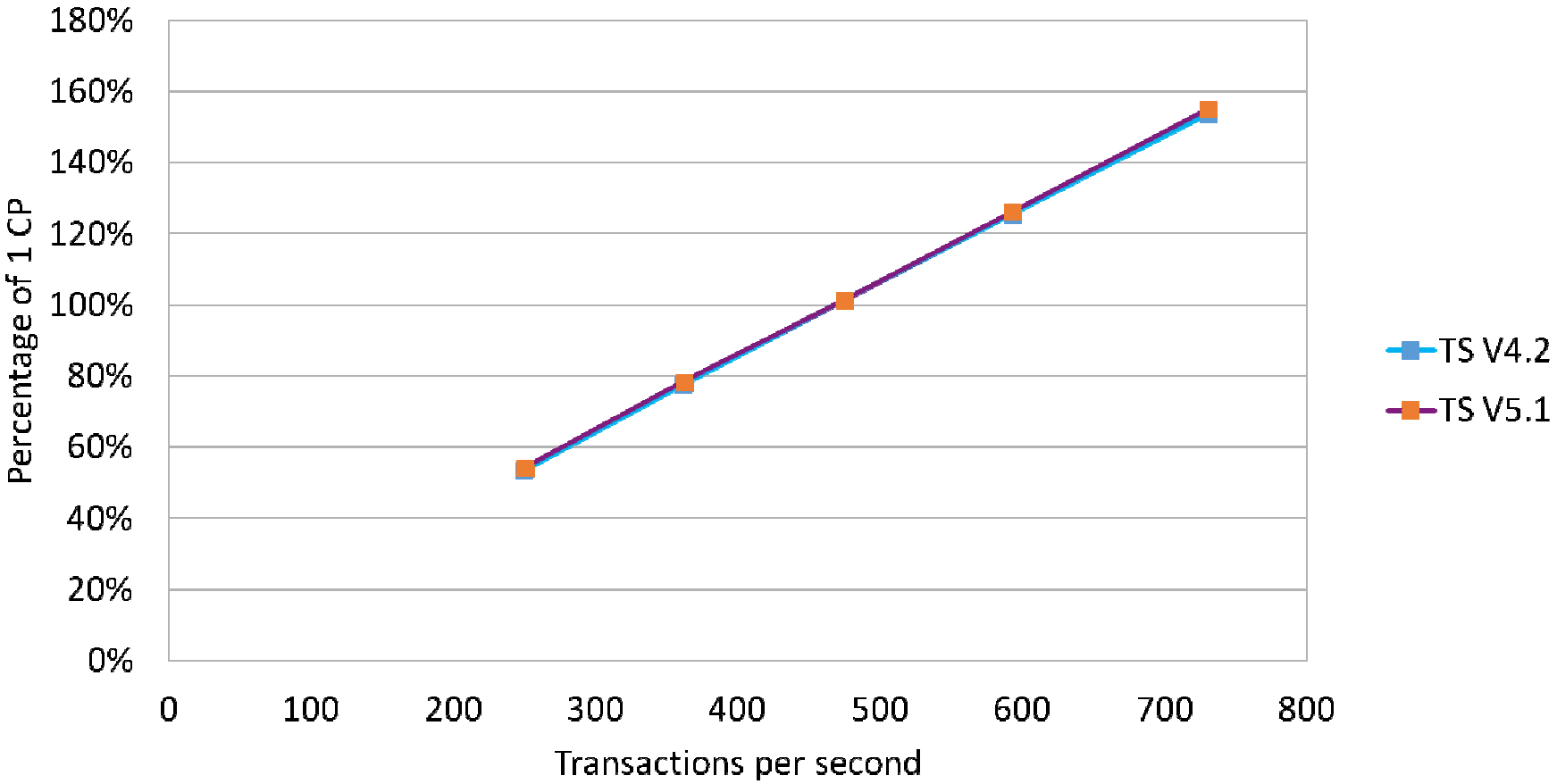
DSW Workload – CPSM Dynamic Routing



CICS TS V4.2
Average CPU / tran = 0.657ms

CICS TS V5.1
Average CPU / tran = 0.654ms

RTW Workload – Single Region



CICS TS V4.2
Average CPU / tran = 2.130ms

CICS TS V5.1
Average CPU / tran = 2.143ms

Virtual Storage Constraint Relief

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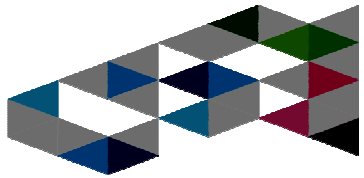
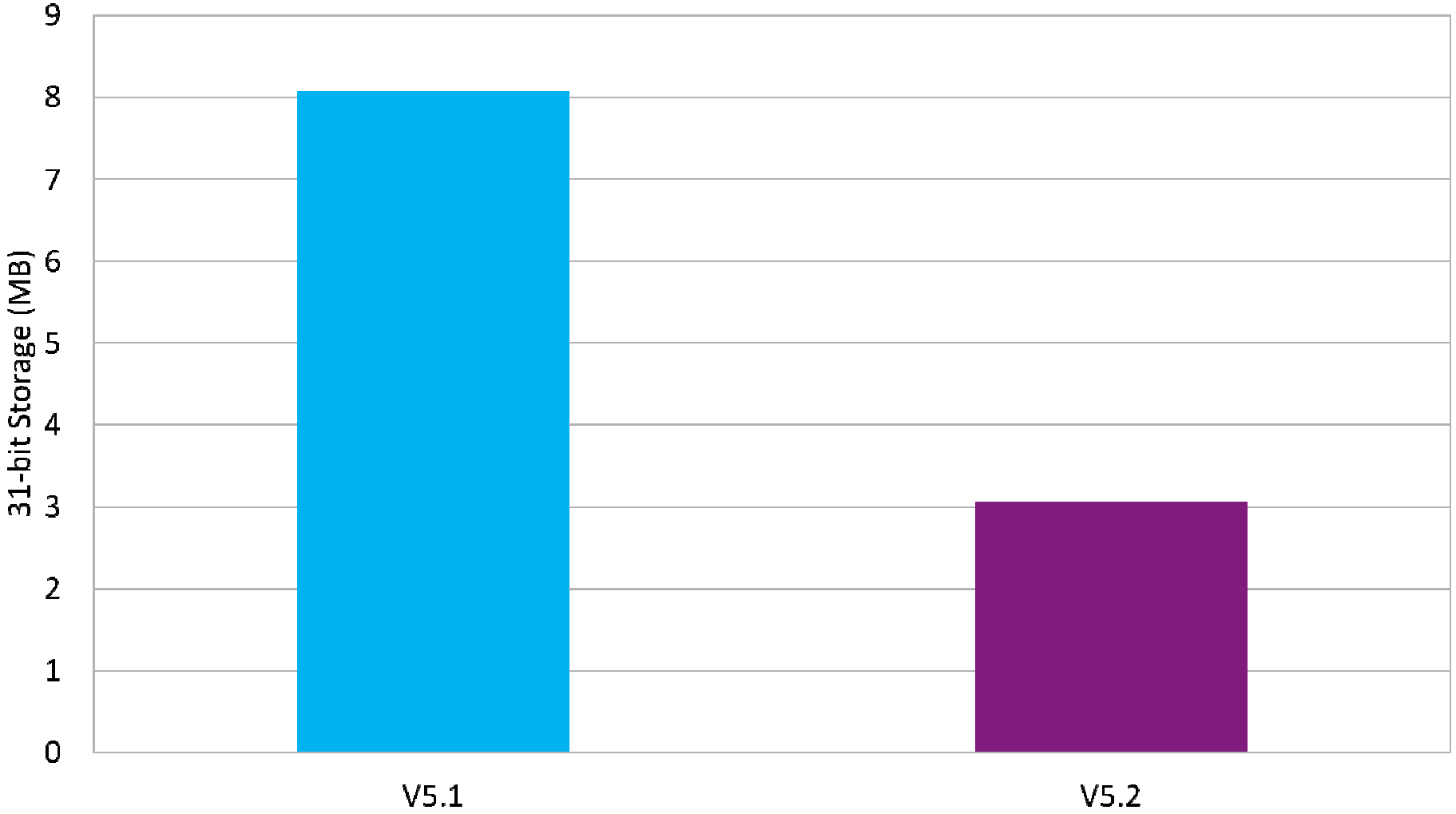
AMODE(64) Application Support – V5.1

- Cache large amounts of data above the bar
  - EXEC CICS GETMAIN64 / FREEMAIN64
- Applications can pass data in 64-bit storage using channels
  - EXEC CICS PUT64 CONTAINER / GET64 CONTAINER
- EXEC CICS LINK / LOAD / XCTL / RETURN
  - AMODE(64) ↔ AMODE(31) ↔ AMODE(64) ↔ AMODE(24)
- Non-LE assembler only



WebService Provider 31-bit Storage – V5.2



Threadsafe

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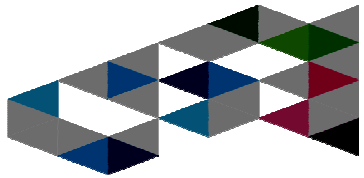
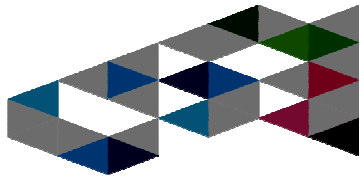
PROGRAM CONCURRENCY Recap

- We run CICS with STGPROT=YES
- My application ...
  - … runs USER key
  - … is threadsafe
  - … makes DB2 calls
- How do I maximise time spent on an Open TCB?



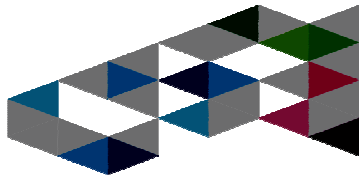
CICS TS V4.1 TCB Switching

STGPROT	Exec key	CONCURRENCY	API	Initial TCB	DB2 or MQ command	Threadsafe command	Non-threadsafe command
Yes/No	(any)	QUASIRENT	CICS	QR	QR → L8 → QR	no change	no change
		THREADSAFE		QR	L8	no change	QR
No	(any)	THREADSAFE	OPEN	L8	no change	no change	L8 → QR → L8
Yes	CICS	THREADSAFE	OPEN	L8	no change	no change	L8 → QR → L8
Yes	USER	THREADSAFE	OPEN	L9	L9 → L8 → L9	no change	L9 → QR → L9



CICS TS V4.2+ TCB Switching

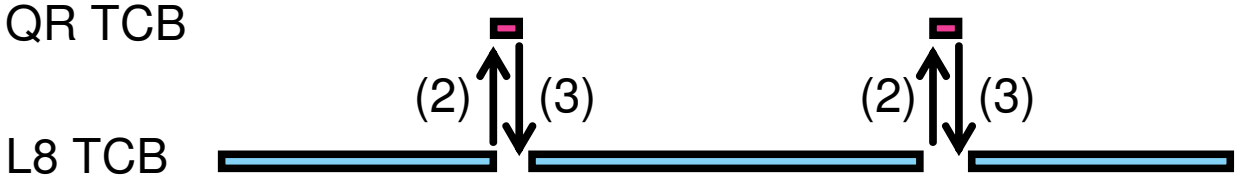
STGPROT	Exec key	CONCURRENCY	API	Initial TCB	DB2 or MQ command	Threadsafe command	Non-threadsafe command
Yes/No	(any)	QUASIRENT	CICS	QR	QR → L8 → QR	no change	no change
		THREADSAFE		QR	L8	no change	QR
		REQUIRED		L8	no change	no change	L8 → QR → L8
No	(any)	THREADSAFE	OPEN	L8	no change	no change	L8 → QR → L8
		REQUIRED		L8	no change	no change	L8 → QR → L8
Yes	CICS	THREADSAFE	OPEN	L8	no change	no change	L8 → QR → L8
		REQUIRED		L8	no change	no change	L8 → QR → L8
Yes	USER	THREADSAFE	OPEN	L9	L9 → L8 → L9	no change	L9 → QR → L9
		REQUIRED		L9	L9 → L8 → L9	no change	L9 → QR → L9



Threadsafe Transient Data Commands (V5.1)

V4.1 – CONCURRENCY(THREADSAFE)

V4.2 – CONCURRENCY(REQUIRED)

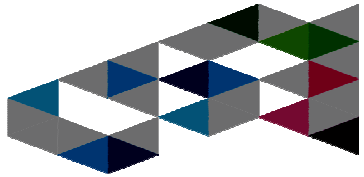


V5.1 – CONCURRENCY(REQUIRED)

(1) TCB switch due to DB2 call

(2) TCB switch due to EXEC CICS WRITEQ TD command

(3) TCB switch back to L8 due to CONCURRENCY(REQUIRED)



Threadsafe Transient Data Commands (V5.1)

```
             Avg     Avg     Avg     Avg     Avg     Avg     Avg
Tran     #Tasks Response User CPU   QR CPU  KY8 CPU DSCHMDLY TD Total RMI DB2
             Time    Time    Time    Time    Count   Count    Time
TDQ1       5938  .011942  .006967  .004597  .002370    302     150  .001626
```

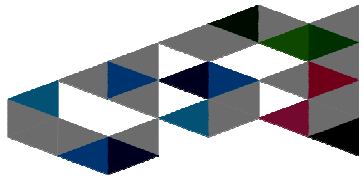
V4.1
QR = 4.60ms
L8 = 2.37ms
302 TCB switches

```
             Avg     Avg     Avg     Avg     Avg     Avg     Avg
Tran     #Tasks Response User CPU   QR CPU  KY8 CPU DSCHMDLY TD Total RMI DB2
             Time    Time    Time    Time    Count   Count    Time
TDQ1       5992  .011393  .006875  .000212  .006663    306     150  .001420
```

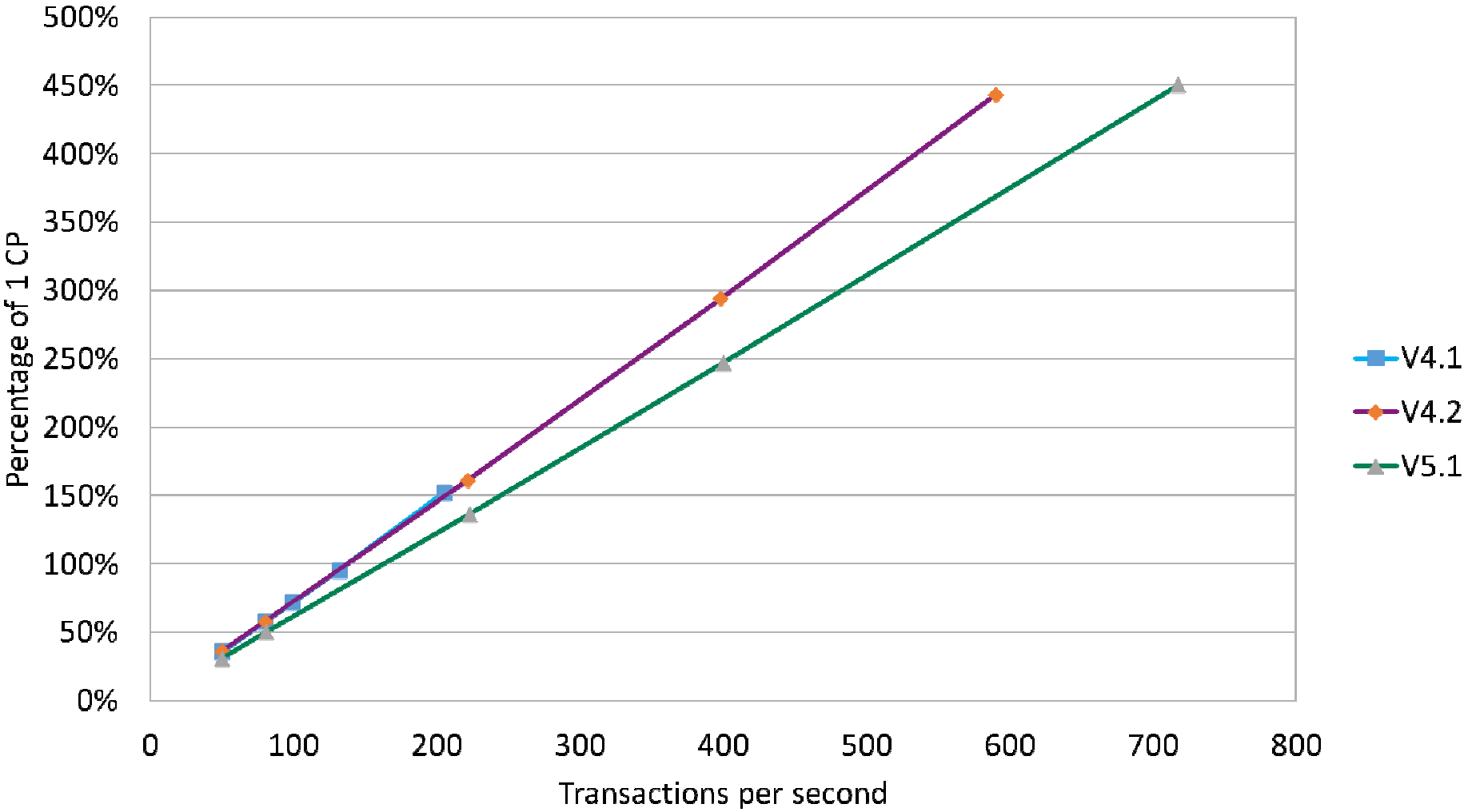
V4.2
QR = 0.21ms
L8 = 6.66ms
306 TCB switches

```
             Avg     Avg     Avg     Avg     Avg     Avg     Avg
Tran     #Tasks Response User CPU   QR CPU  KY8 CPU DSCHMDLY TD Total RMI DB2
             Time    Time    Time    Time    Count   Count    Time
TDQ1       6000  .006805  .006195  .000026  .006169      8     150  .001147
```

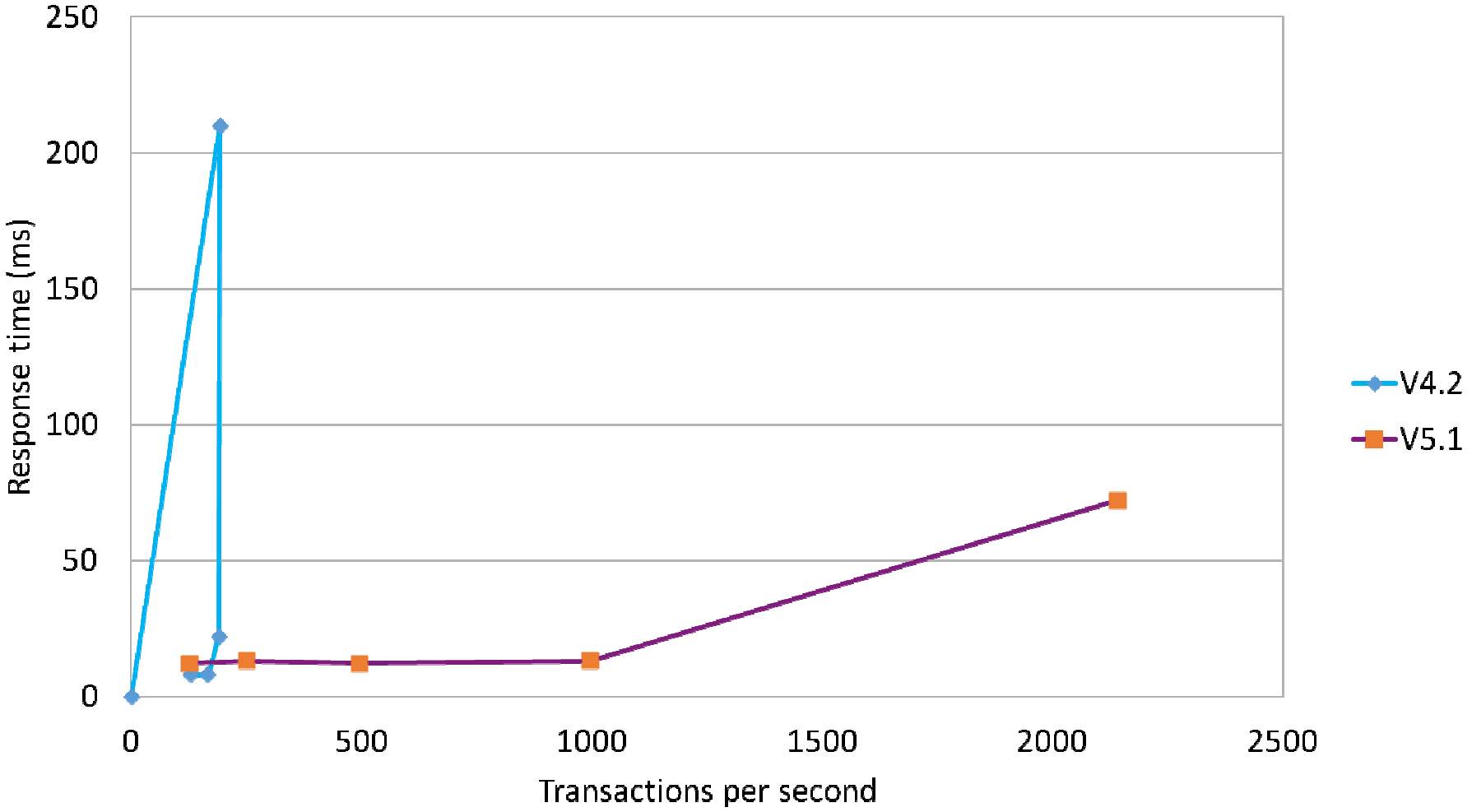
V5.1
QR = 0.03ms
L8 = 6.17ms
8 TCB switches



Transient Data Mixed with DB2

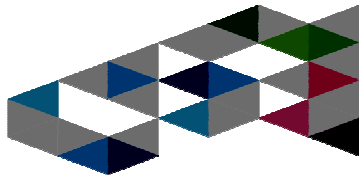


Physical Program Loads V4.2 vs V5.1



IPIC Function-Shipping

- V4.2 – Mirror task uses Open TCB
- V5.1 – Originating task uses Open TCB
- Function-ship performance
  - Response times comparable to XCF
  - Response times better than LU6.2
  - Better throughput achievable than LU6.2



Java

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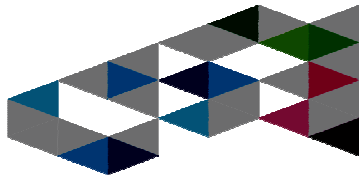
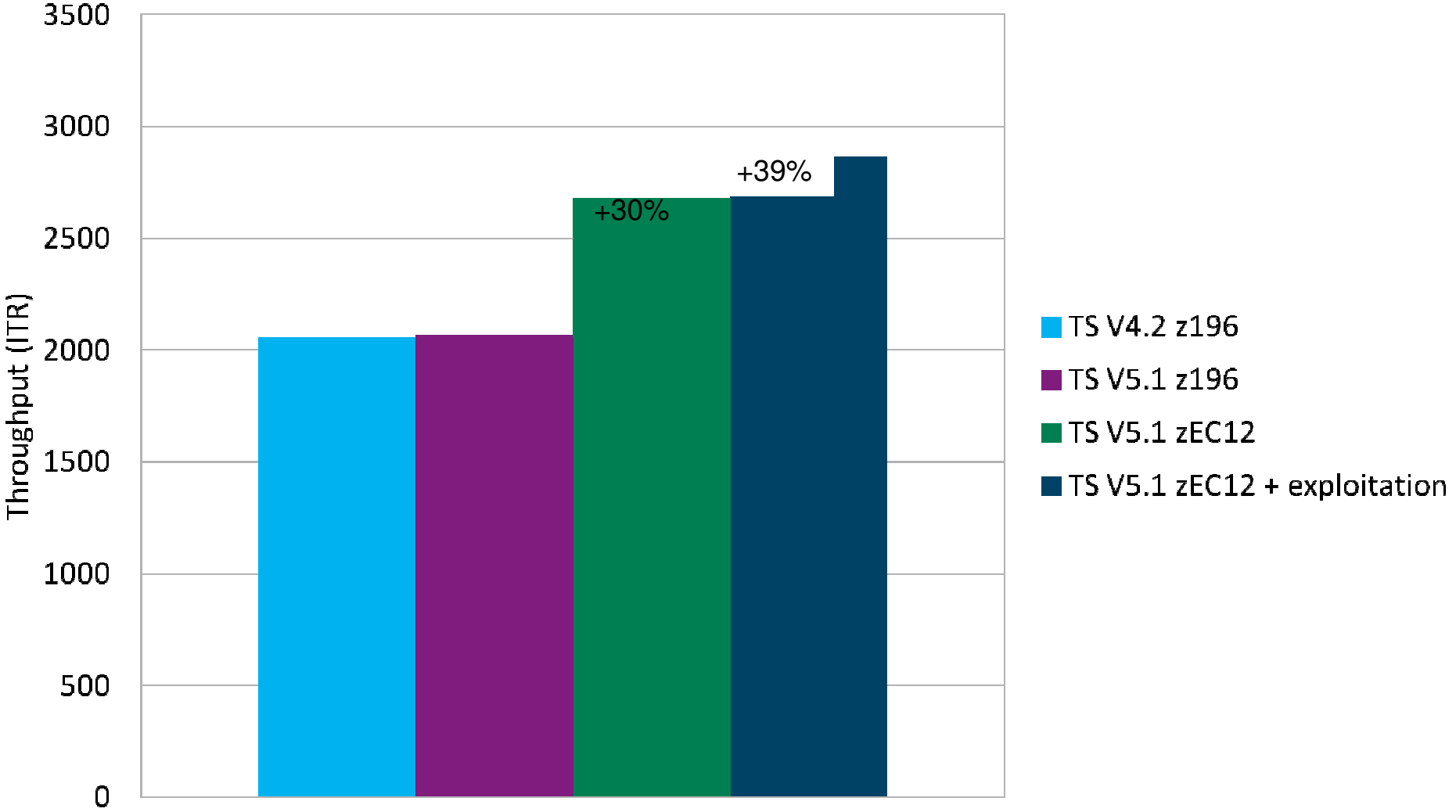
Exploitation of Latest Java Versions

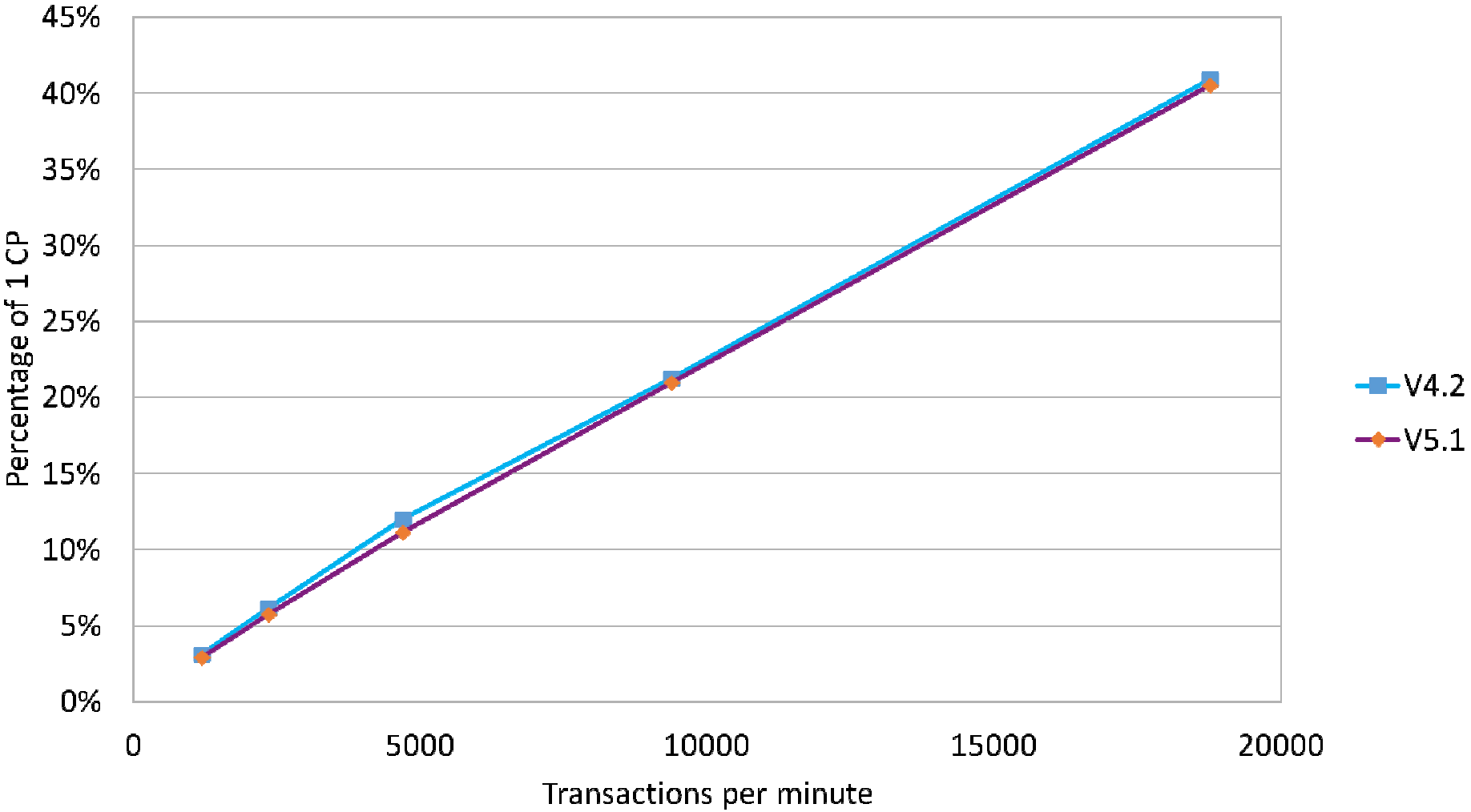
- CICS TS V4.2 – Java™ 6
  - First CICS support for 64-bit JVM
- CICS TS V5.1 – Java 7
  - Improved out-of-the-box performance on zEC12
  - With exploitation, even greater performance
- CICS TS V5.2 – Java 7 & Java 7.1
  - 2GB page support
  - Data access acceleration API
  - SMC-R support
  - zEDC support



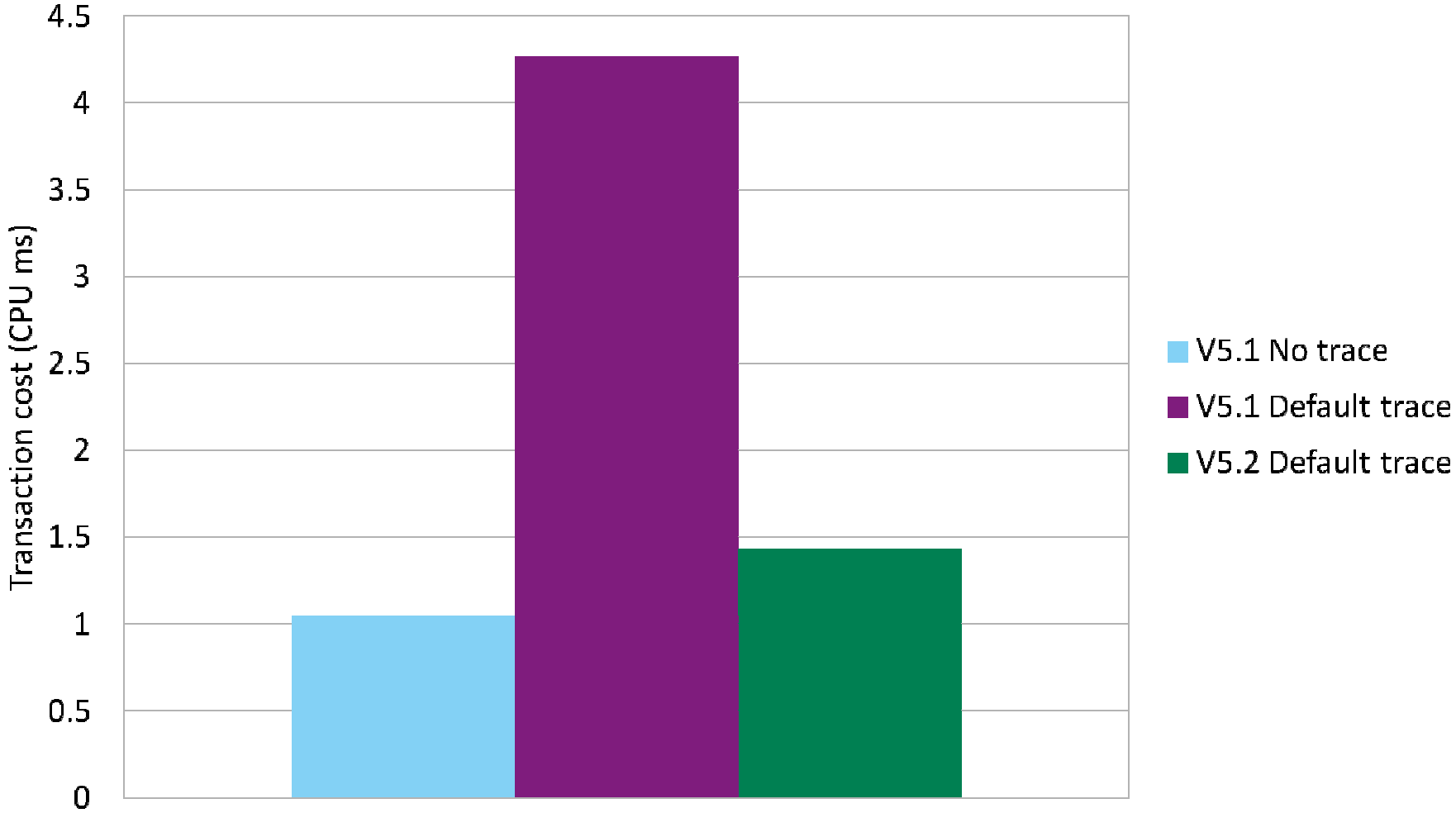
zEC12 Exploitation with Java 7 – V5.1



JDBC Calls From T8 TCB – V5.1



JCICS 120 File Read Operations – V5.2



Improved Instrumentation

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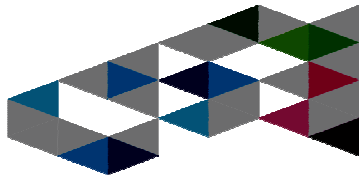
Notable Metrics Enhancements

- Transaction wait times
- zAAP / zIIP transaction CPU time
- Transaction performance related to region load
- Inbound SSL cipher code
- Default value of RMI data collection option changed to YES



CICS Performance Analyzer

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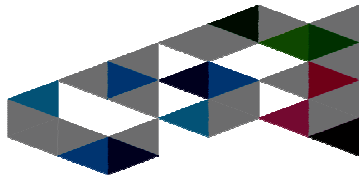
CICS Performance Analyzer – V5.2

- Performance alerts in HDB
- Significant enhancements in CICS Explorer plugin



CICS Interdependency Analyzer

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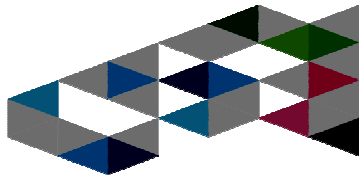
CICS Interdependency Analyzer V5.2

- Optimize the collector
  - Single comparison point 75% reduction in overhead
- Deeper threadsafe analysis
  - Load module scanning
  - CPSM commands
  - MRO vs. IPIC connections



MQ DPL Bridge

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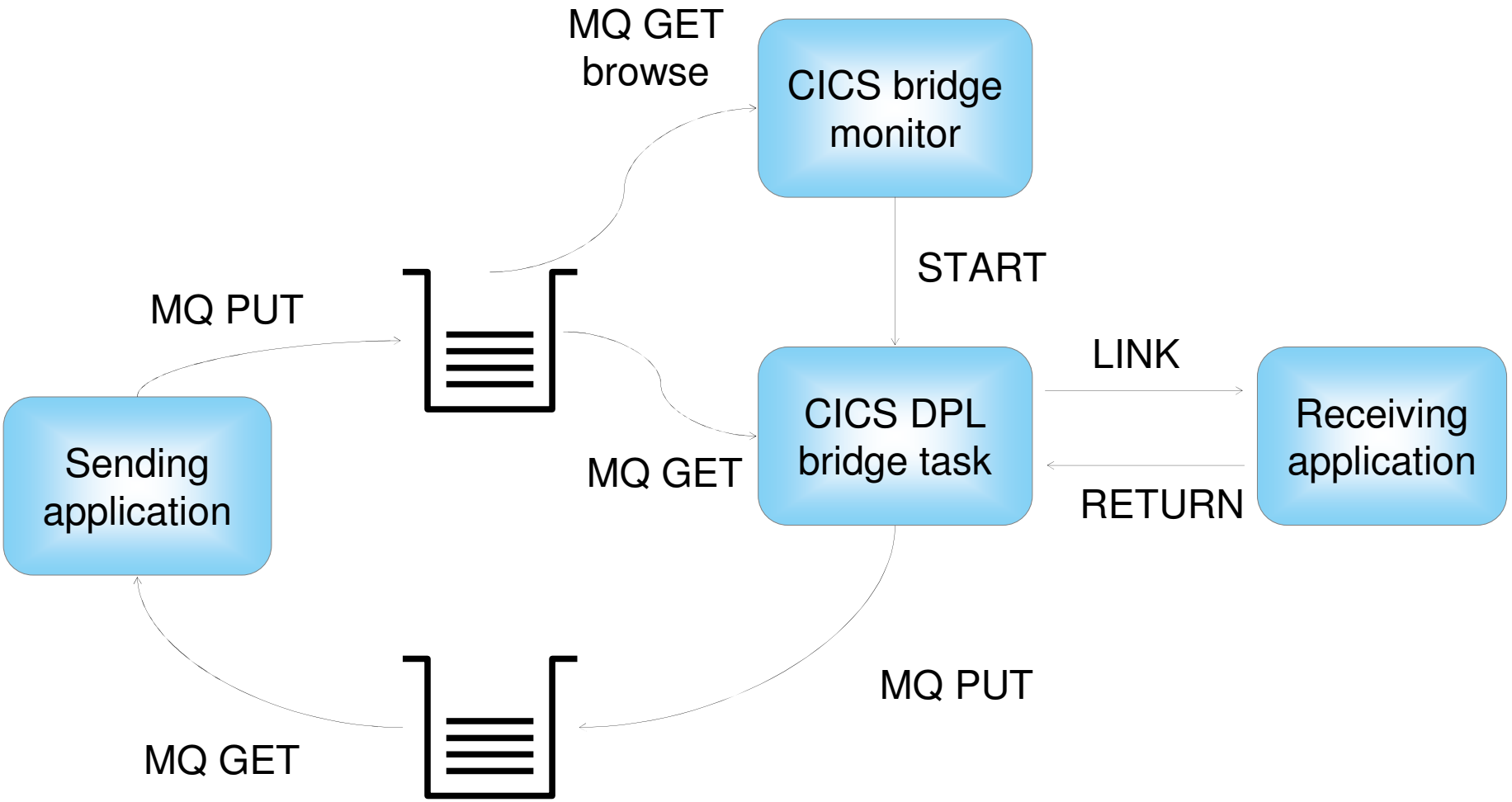
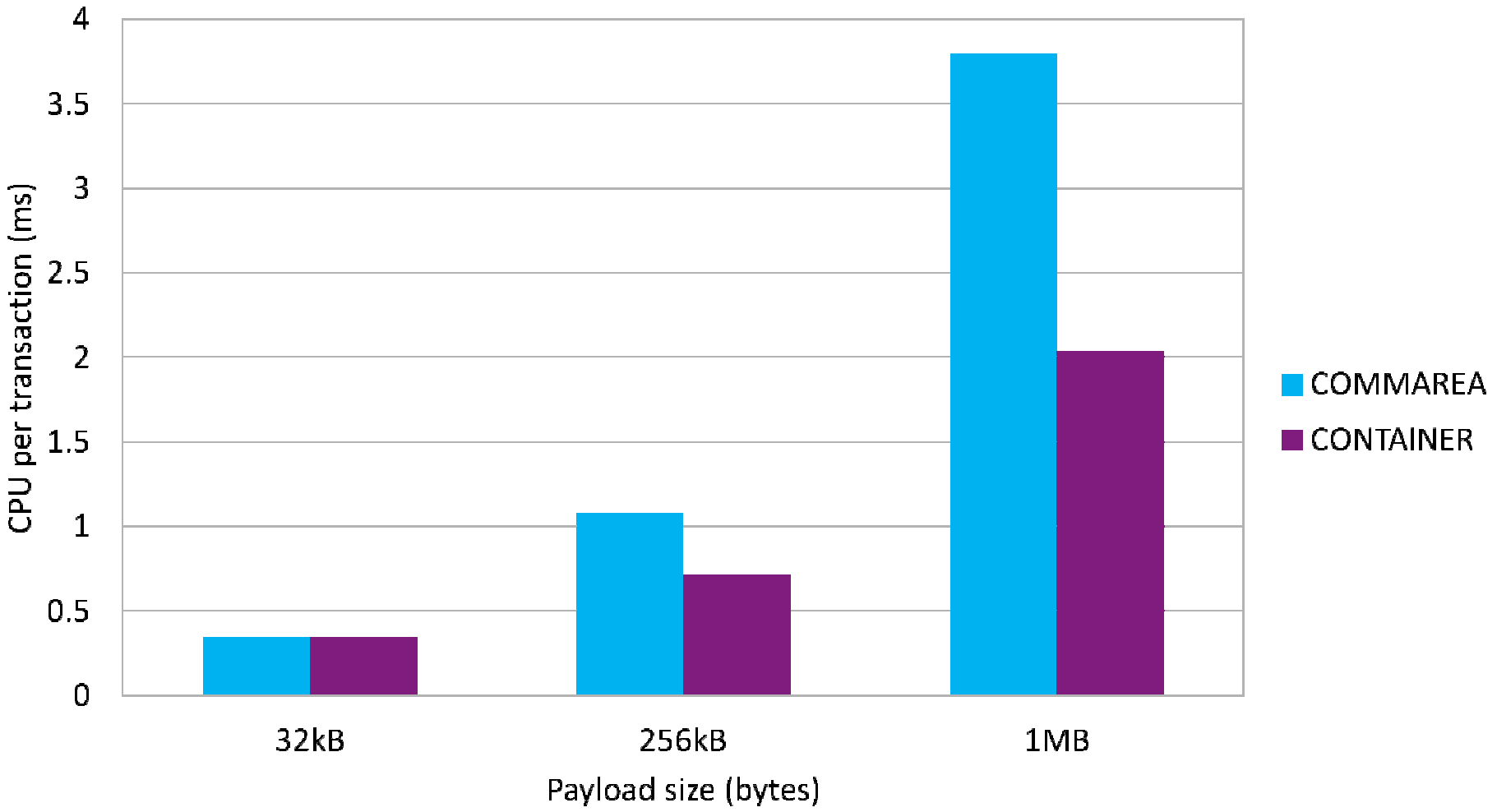
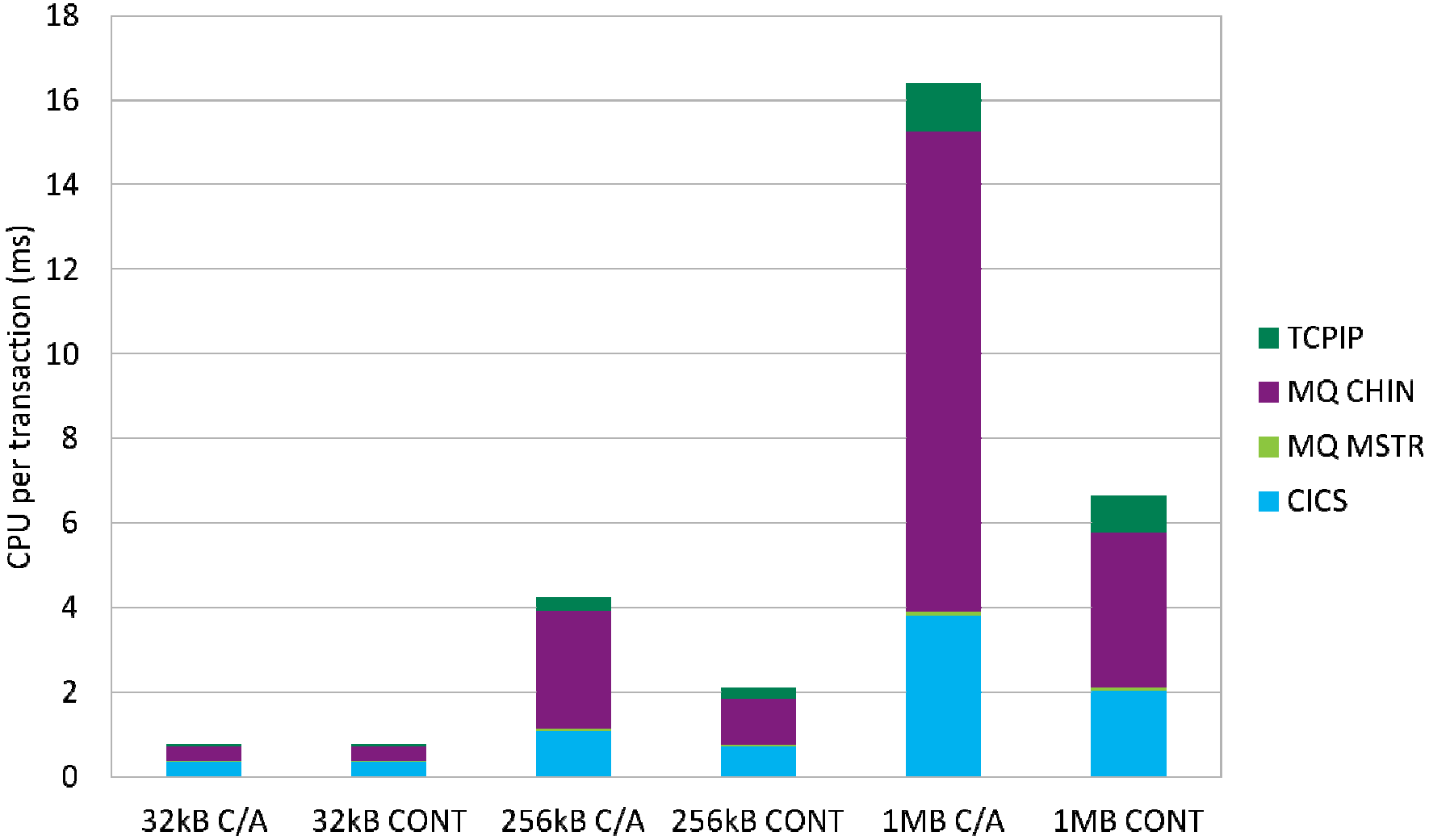
High-Level Outline



MQ DPL Bridge – CICS CPU



MQ DPL Bridge – CICS, WMQ and TCP/IP CPU



SMC-R

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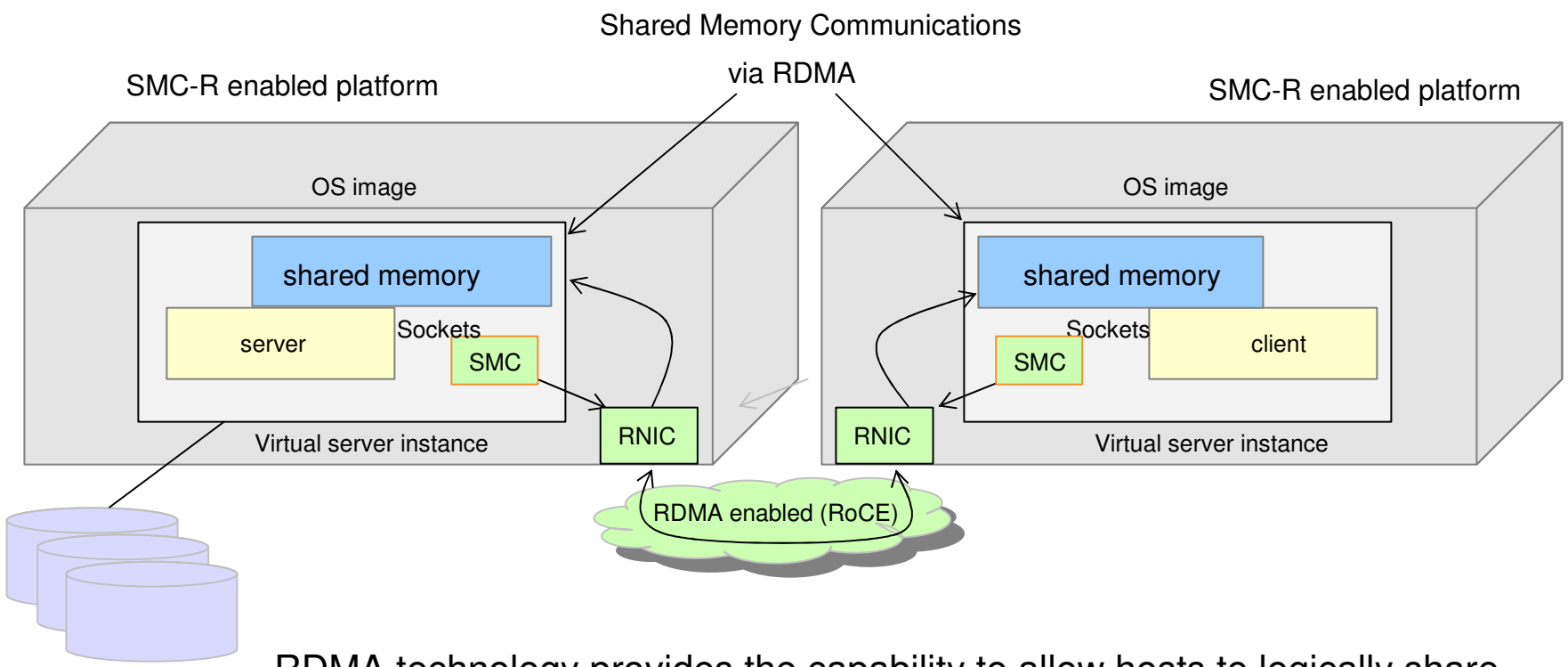
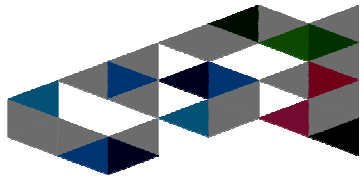
Shared Memory Communications over RDMA

Clustered Systems



RDMA technology provides the capability to allow hosts to logically share memory. The SMC-R protocol defines a means to exploit the shared memory for communications - *transparent* to the applications!



Optimize server to server networking – transparently

Network latency for z/OS TCP/IP based OLTP workloads ***reduced*** by up to ***80%***

Networking related CPU consumption for z/OS TCP/IP based workloads with streaming data patterns ***reduced*** by up to ***60%*** with a *network throughput* increase of up to ***60%***

Shared Memory Communications (SMC-R):

Exploit RDMA over Converged Ethernet (RoCE) to deliver superior communications performance for TCP based applications

Typical Client Use Cases:

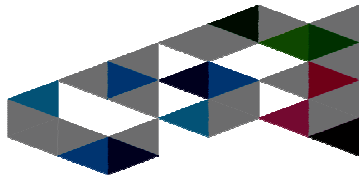
Help to reduce both latency and CPU resource consumption over traditional TCP/IP for communications across z/OS systems

Any z/OS TCP sockets based workload can **seamlessly** use SMC-R without requiring any application changes

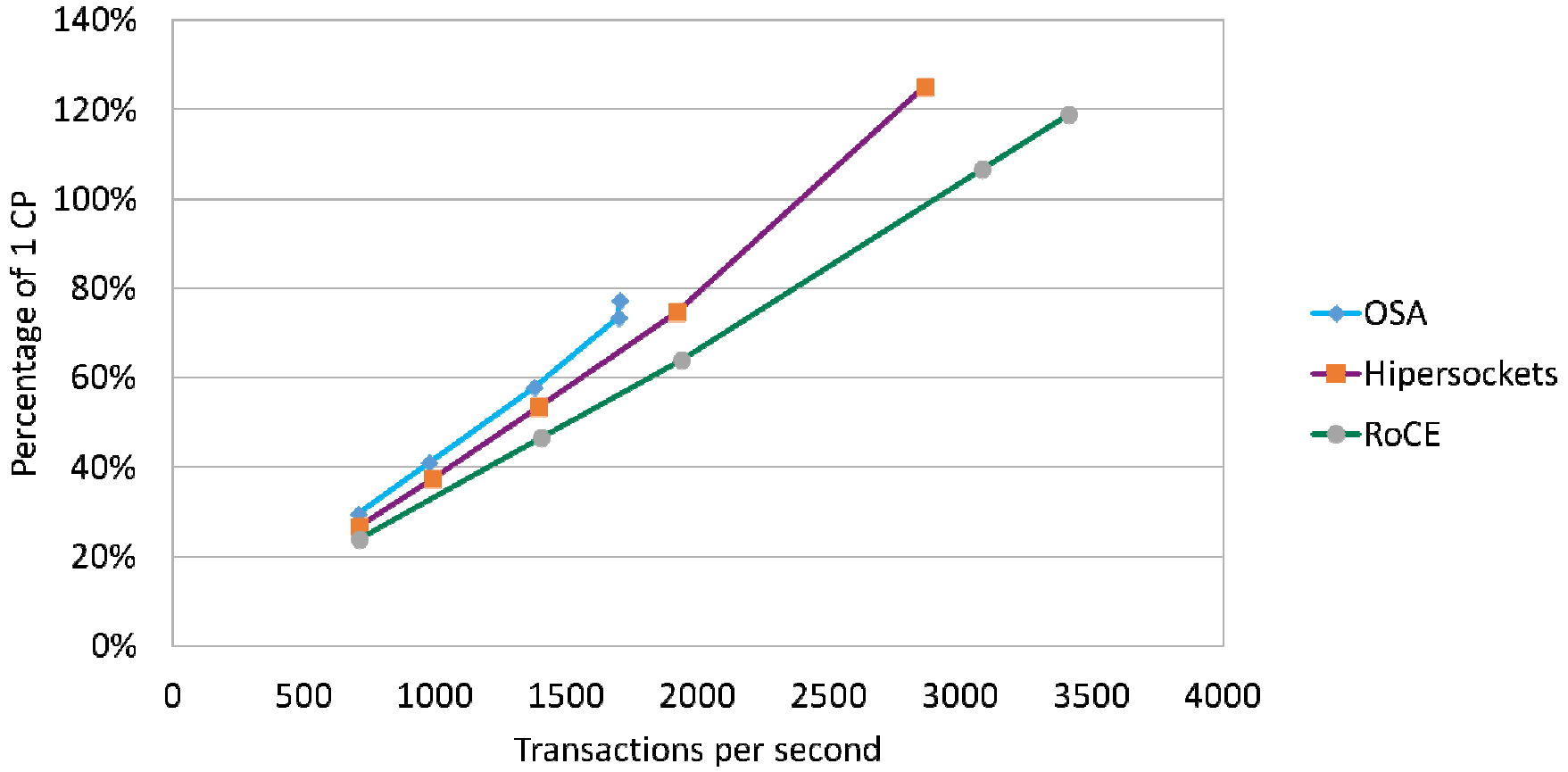
NEW **z/OS V2.1 SMC-R**

NEW **z/VM 6.3 support for guests**

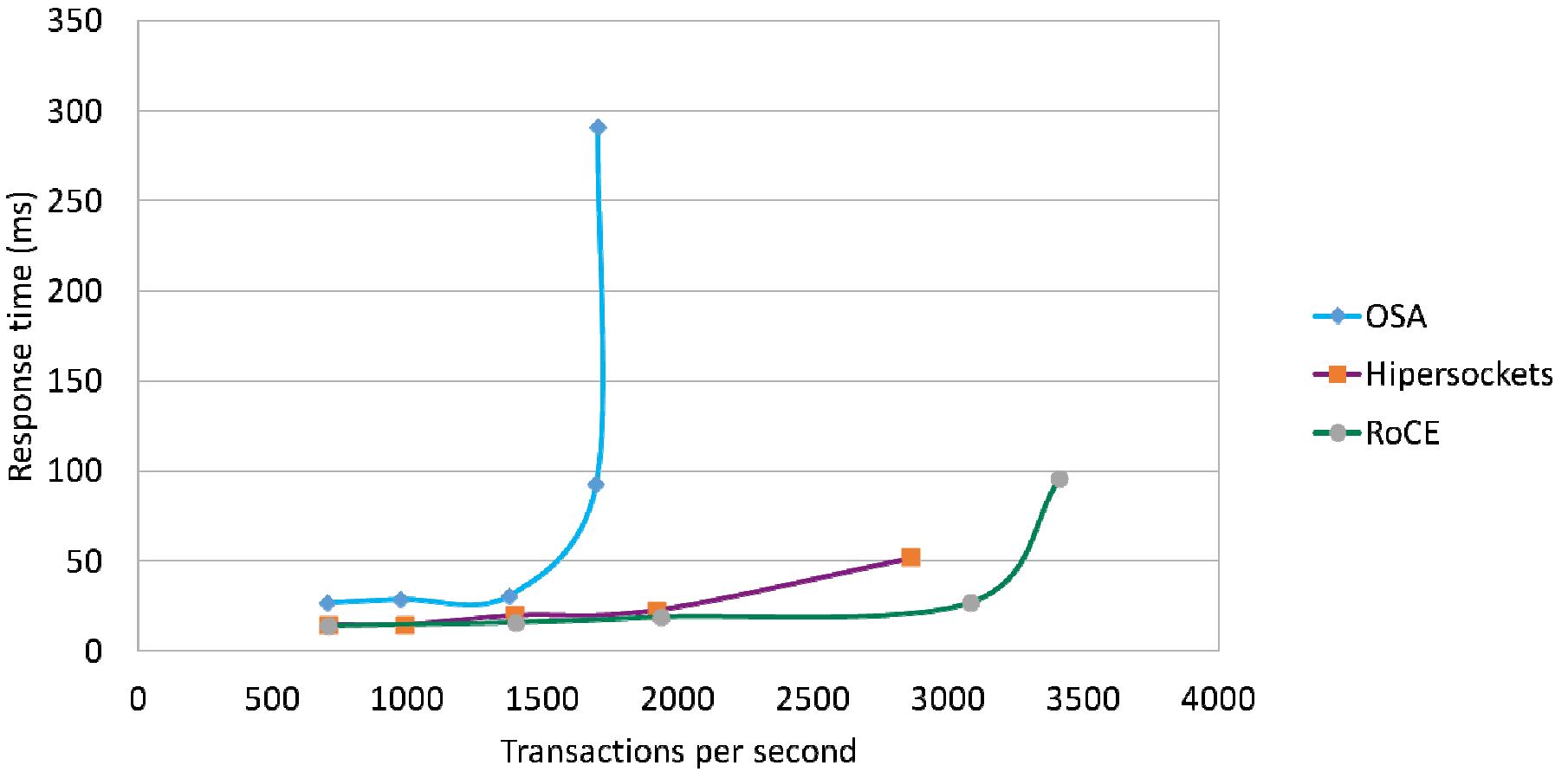
NEW **10GbE RoCE Express**



CICS DPL over IPIC Workload



CICS DPL over IPIC Workload



Workload Consolidation

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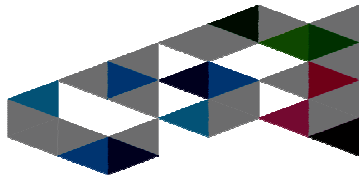
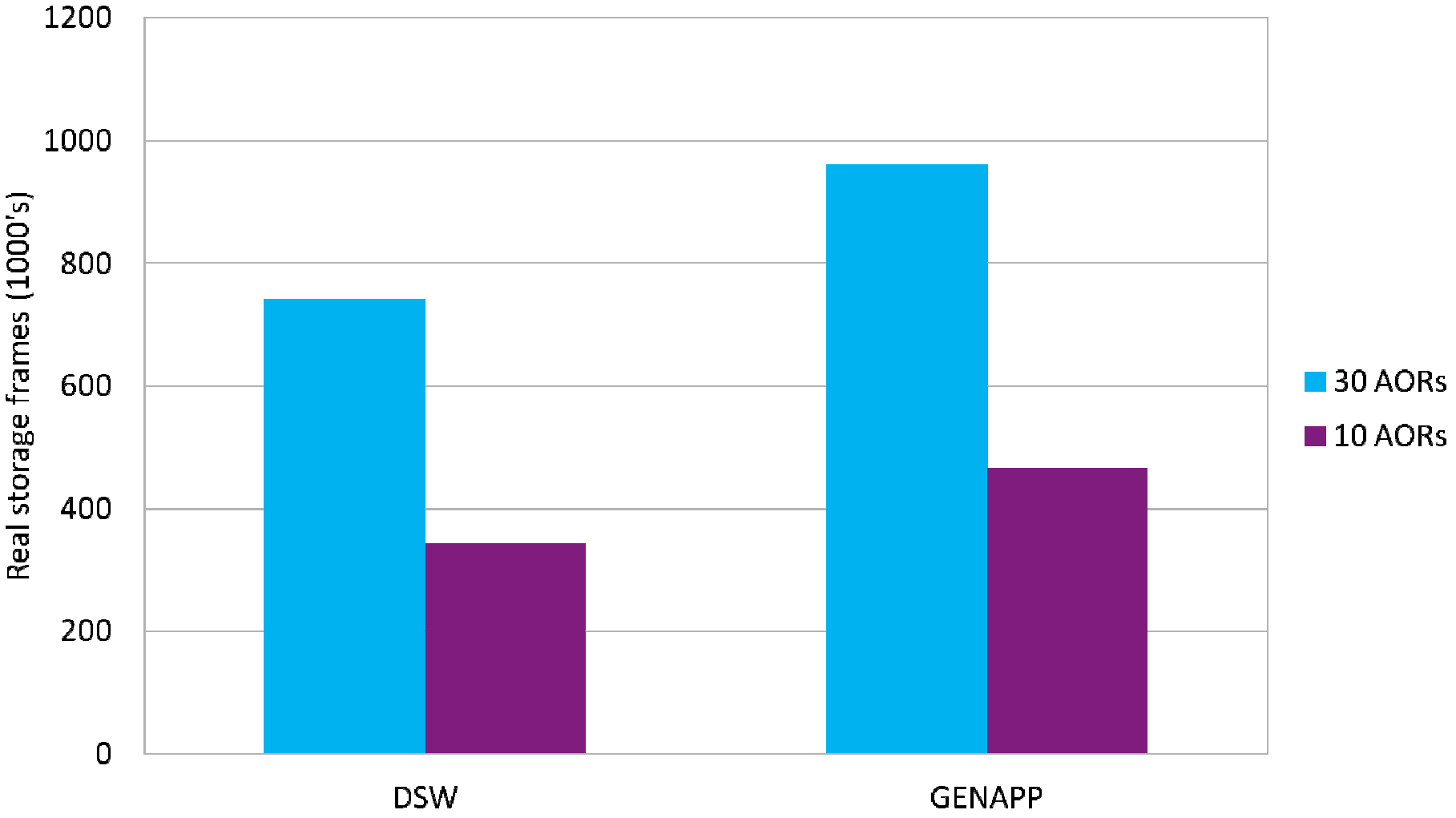
Workload Consolidation

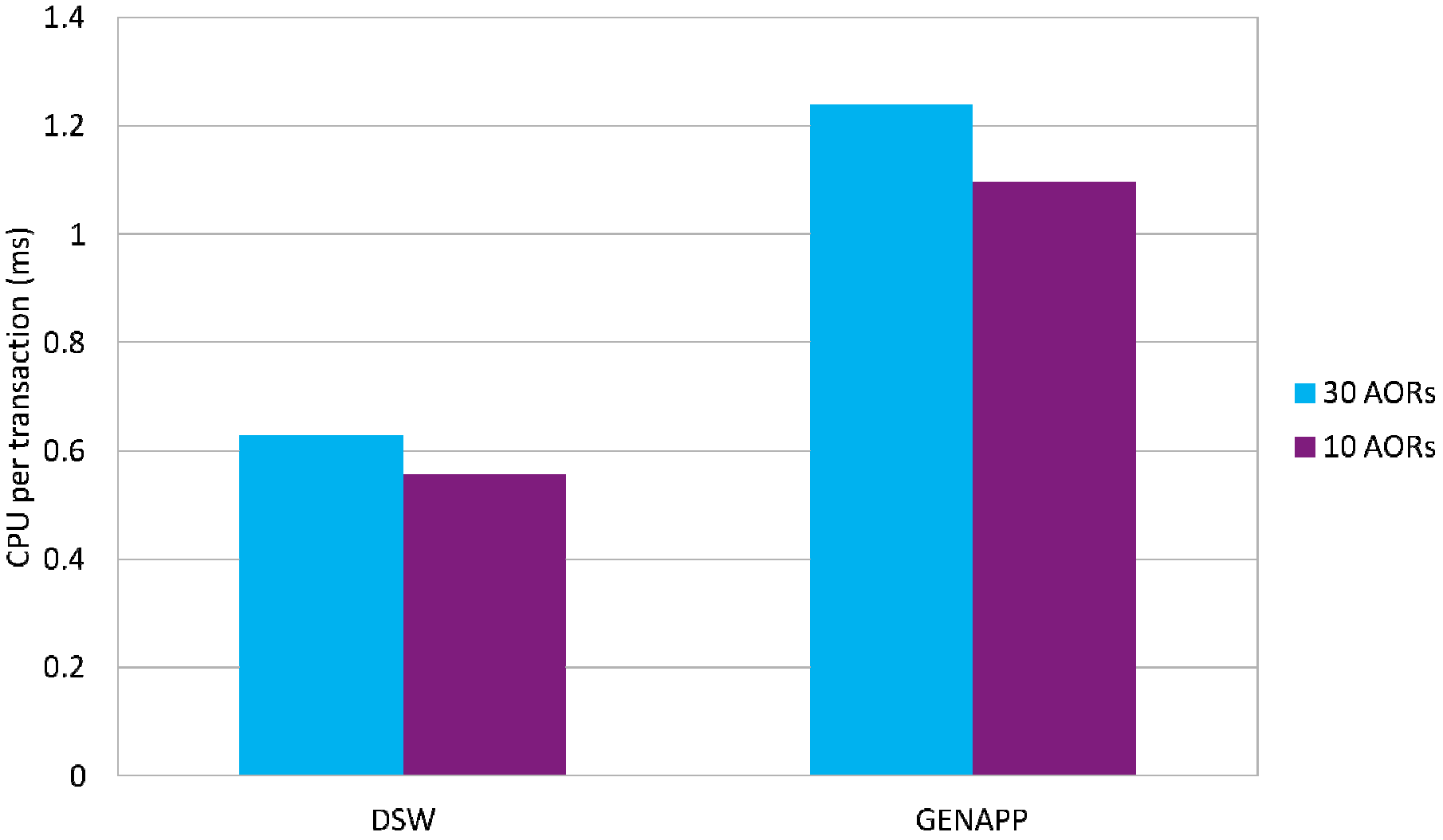
- Run more work through less regions
  - Continual expansion of threadsafe support in V5
  - Further VSCR
  - MXT limit doubled
- Consolidating regions
  - Saves real storage
  - Can save MIPs
  - Saves operational costs



Real Storage Savings



CPU Savings


1.4
1.2
1
0.8
0.6
0.4
0.2
0
CPU per transaction (ms)
DSW
GENAPP
30 AORs
10 AORs

Summary

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Questions?

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Thank You

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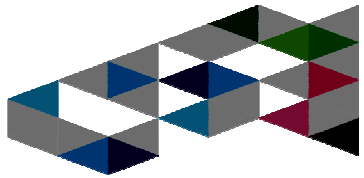

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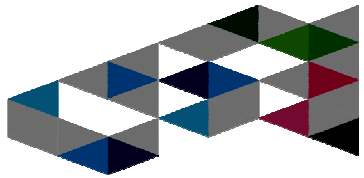

Measurement Process (Backup)

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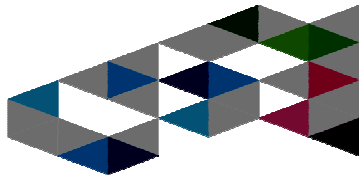
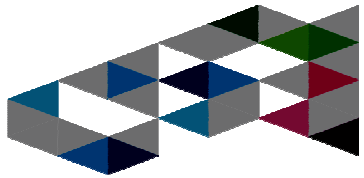
Environment

- Hardware
  - z196 2817-779 model M80
  - LPAR with up to 16 dedicated CPs
    - See each benchmark description for number of CPs actually used
  - Separate LPAR with 4 dedicated CPs for Network driver
  - DASD DS8800
  - Internal Coupling Facility with ICP links
- Software
  - z/OS 1.13
  - CICS TS V4.2
  - CICS TS V5.1



Measurement Process

- Overnight automation on dedicated LPAR
- 5 RMF intervals recorded
- Various transaction rates
- Total CICS address space accumulated
- Divided by transaction rate to give CPU/tran
- Average CPU/tran over 5 intervals compared
- Any difference analysed using Hardware Instrumentation (HIS)



Release-Release (V5.1) (Backup)

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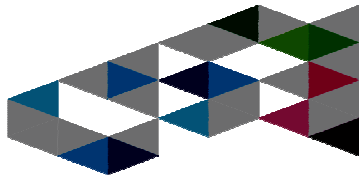
DSW Workload – Static routing

- COBOL/VSAM
- All transactions routed from 2 TORs to 2 AORs
- All FILE requests are Function Shipped to 1 FOR
- 50% of transactions issue FC requests
- All FC requests are VSAM LSR
- Average of 6 requests per transaction (all transactions)
- 69% Read, 10% Read for Update, 9% Update,11% Add , 1% Delete
- 16 CPs - 5 CICS regions



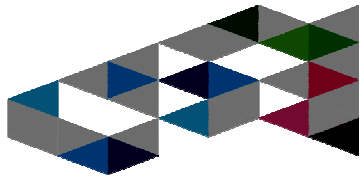
DSW Workload – Static routing

ETR	CICS %	ms/tran	LPAR %
2498.52	75.86%	0.304	6.78%
2928.69	88.35%	0.302	7.79%
3543.47	104.08%	0.294	9.09%
4428.34	129.16%	0.292	11.13%
5944.91	168.58%	0.284	14.34%

CICS TS V4.2
Average CPU / tran = 0.295ms

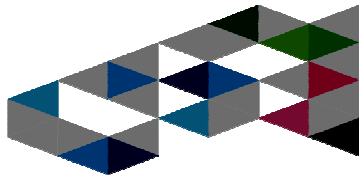
ETR	CICS %	ms/tran	LPAR %
2496.35	77.55%	0.311	6.89%
2939.62	87.18%	0.297	7.65%
3532.10	102.29%	0.290	8.86%
4425.48	126.17%	0.285	10.80%
5948.50	166.52%	0.280	14.07%

CICS TS V5.1
Average CPU / tran = 0.292ms



DSW Workload – CPSM Dynamic Routing

- COBOL/VSAM
- All transactions routed from 4 TORs to 30 AORs via CPSM
- 50% of transactions issue FC requests
- All TS requests are TS Shared
- All FC requests are VSAM RLS
- Average of 6 requests per transaction (all transactions)
- 69% Read, 10% Read for Update, 9% Update, 11% Add, 1% Delete
- 8 CPs - 34 CICS regions



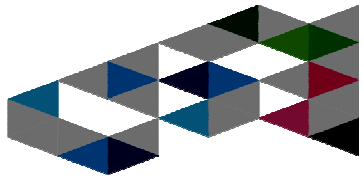
DSW Workload – CPSM Dynamic Routing

ETR	CICS %	ms/tran	LPAR %
2071.61	141.20%	0.681	21.05%
2842.02	189.11%	0.665	27.85%
4128.25	270.70%	0.655	39.41%
5047.36	326.08%	0.646	47.24%
6493.98	417.16%	0.642	60.21%

CICS TS V4.2
Average CPU / tran = 0.657ms

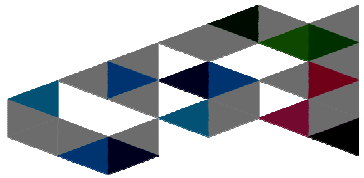
ETR	CICS %	ms/tran	LPAR %
2074.87	139.91%	0.674	20.87%
2846.00	188.55%	0.662	27.78%
4133.39	269.54%	0.652	39.32%
5053.15	326.22%	0.645	47.33%
6501.18	416.92%	0.641	60.25%

CICS TS V5.1
Average CPU / tran = 0.654ms



RTW Workload – Single Region

- COBOL/DB2
- 7 transaction types
- 20 Database tables
- Average 200 DB2 calls per transaction
- 54% SELECT, 1% INSERT, 1% UPDATE, 1% DELETE
- 8% open cursor, 27% fetch cursor, 8% close cursor



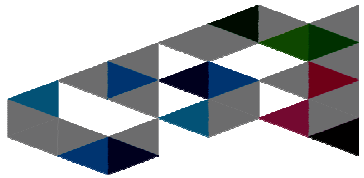
RTW Workload – Single Region

ETR	CICS %	ms/tran	LPAR %
249.69	53.59%	2.146	21.33%
361.55	77.65%	2.147	30.93%
474.66	101.46%	2.137	39.85%
592.37	125.40%	2.116	48.89%
730.20	153.82%	2.106	59.51%

CICS TS V4.2
Average CPU / tran = 2.130ms

ETR	CICS %	ms/tran	LPAR %
249.98	54.19%	2.167	21.63%
361.88	78.35%	2.165	31.26%
474.86	101.42%	2.135	39.74%
592.74	126.14%	2.128	49.20%
729.98	155.06%	2.124	59.98%

CICS TS V5.1
Average CPU / tran = 2.143ms



VSCR
(Backup)

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Virtual Storage Constraint Relief (VSCR)

- 24-bit Virtual Storage Constraint Relief
  - Reduce pressure on below the line storage
  - Provide for greater capacity for workload growth
- 24-bit Virtual Storage Constraint Relief …
  - Control blocks, Modules, and stack storage moved above the line
    - Syncpoint, Transient Data, Journal Control, …
  - Extrapartition Transient Data access method buffers
    - I/O moved from 24-bit to 31-bit
  - Reduce below-the-line storage used by CICS supplied transactions
    - Redefined with TASKDATALOC(ANY)
    - For example …
    - CEMT, CEOT, CESN, CESF, CETR, CMSG, CRTE, CWTO, …
    - CIEP, CSNC, CEDF, and the Mirror transactions …

Virtual Storage Constraint Relief (VSCR) …

- 24-bit Virtual Storage Constraint Relief …

•User Exit Global Work Area

–New GALOCATION parameter on the ENABLE PROGRAM command

–LOC24 → The global work area is in 24-bit storage.

»This is the default location.

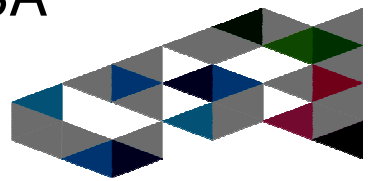
–LOC31 → The global work area is in 31-bit storage.

•COMMAREA on XCTL now in 31-bit

–Only copied to 24-bit if needed by target program

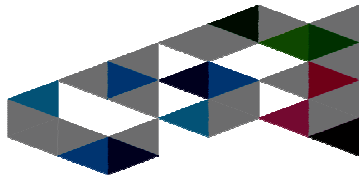
•Language Environment APAR PM57053 (z/OS R13)

–Reduces LE's use of 24-bit CICS storage in the SDSA



Scalability – Greater Use of 64-bit Storage

- Greater Use of 64-bit Storage
- CICS Domain control blocks moved from 31-bit to 64-bit …
  - Console Queue Domain – Selected storage subpools
  - Loader Domain – Selected storage subpools
  - Storage Manager Domain – Additional control blocks moved into 64-bit
- New components exploiting 64-bit storage …
  - e.g. Managed Platform, Application Context
- 64-bit CICS Assembler Application Support – AMODE(64)
  - Non-Language Environment Assembler Programs Only!



64-bit Application Support (Backup)

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- Level 1 bullet
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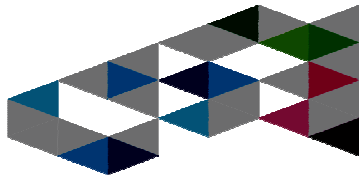


Greater access to 64-bit storage

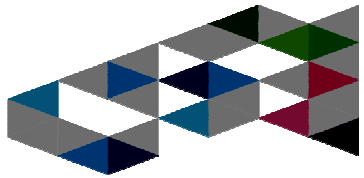
–64-bit CICS Assembler Application Support – AMODE(64)

–Provides application support to access large data objects

–Application can cache large amounts of data above the bar

–Application must copy data into 31-bit storage if used on EXEC CICS API
»For example – when used as the FROM data when writing to a File

–Application can use channels/containers to pass application data
»CICS keeps the container data in 64-bit storage
»CICS passes the data to application in 31-bit or 64-bit storage as appropriate



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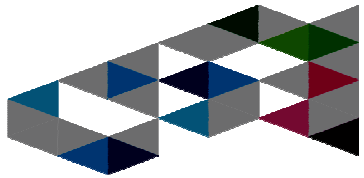
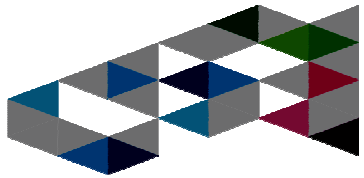


64-bit application support

- 64-bit CICS Assembler Application Support – AMODE(64)
- Non-Language Environment Assembler Programs Only!
- Only the CICS Command Level Programming Interface is supported!
  - No support for CICS Resource Manager APIs …
  - e.g. DB2, WebSphere MQ, IMS DBCTL, etc, …
- Provides Access to Large Data Objects or Data Cache
  - CICS Managed 64-bit Storage – CICS, USER, SHARED …
  - EXEC CICS GETMAIN64 and FREEMAIN64 for 64-bit storage
  - 64-bit Channels and Containers …
  - EXEC CICS GET64 CONTAINER and PUT64 CONTAINER
- EXEC CICS LINK, LOAD, XCTL, RETURN to/from any AMODE
  - AMODE(64) ←→ AMODE(31) ←→ AMODE(64) ←→ AMODE(24)
- AMODE(64) Assembler Programs are NOT supported as …
  - Global or Task User Exit Programs (GLUEs or TRUEs)
  - User Replaceable Programs (URMs



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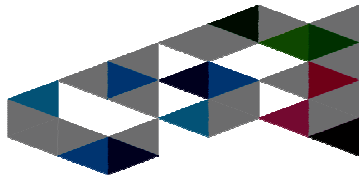
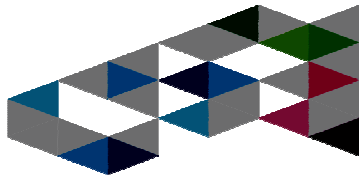


64-bit Containers new API commands

- New in CICS V5.1
  - API commands
    - non-LE AMODE(64) Assembler programs only
  - GET64 CONTAINER
  - PUT64 CONTAINER
  - GETMAIN64
  - FREEMAIN64



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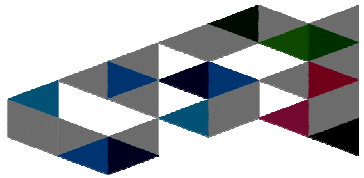


CONTAINER performance tests

- Performance workload 1

–workloads ran on CICS TS V4.2 and V5.1 with non-LE AMODE(31) Assembler programs and CICS TS V5.1 with non-LE AMODE(64) Assembler programs

–workload consisted of simple transactions issuing:

•GETMAIN or GETMAIN64 (size 1 Meg)

•n*PUT CONTAINER or n*PUT64 CONTAINER (GETMAIN'd data is PUT into a container. The value n is altered for each performance run)

•LINK

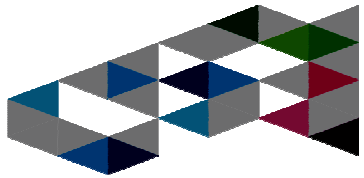
–Linked to program issues:

>n*GET CONTAINER or n*GET64 CONTAINER

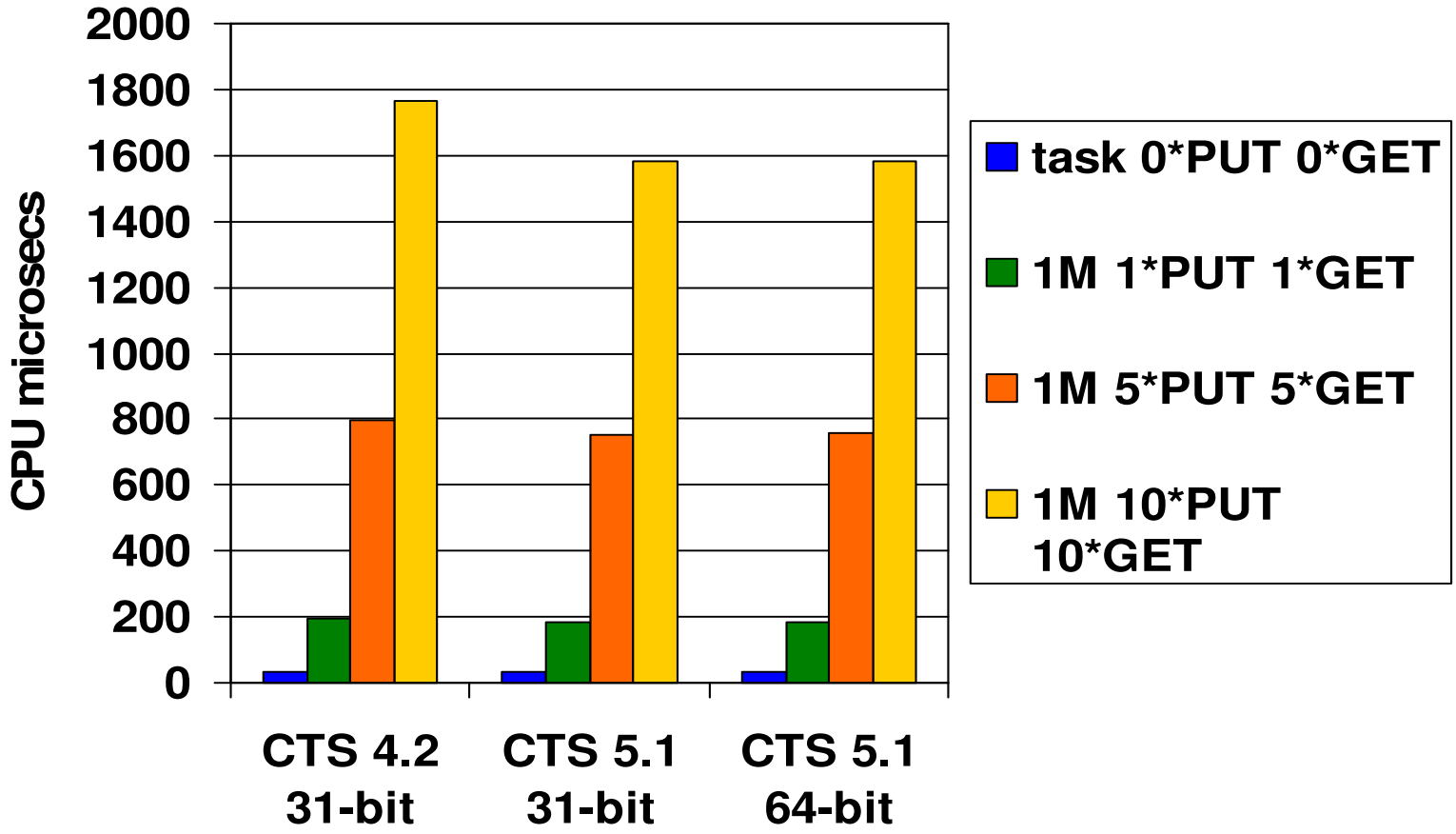
>RETURN

•SEND

•RETURN



CPU costs using CONTAINER commands



Containers – CICS TS V4.2 vs CICS TS V5.1

- Performance workload workloads ran on CICS TS V4.2 and CICS TS V5.1

–workload consisted of simple COBOL transactions issuing:

•GETMAIN (size 1 Meg)

•n*PUT CONTAINER (GETMAIN'd data is PUT into a container. The value n is altered for each performance run)

•LINK

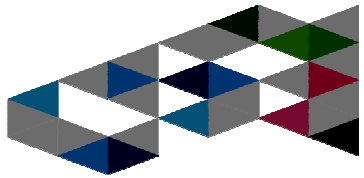
–Linked to program issues:

>n*GET CONTAINER

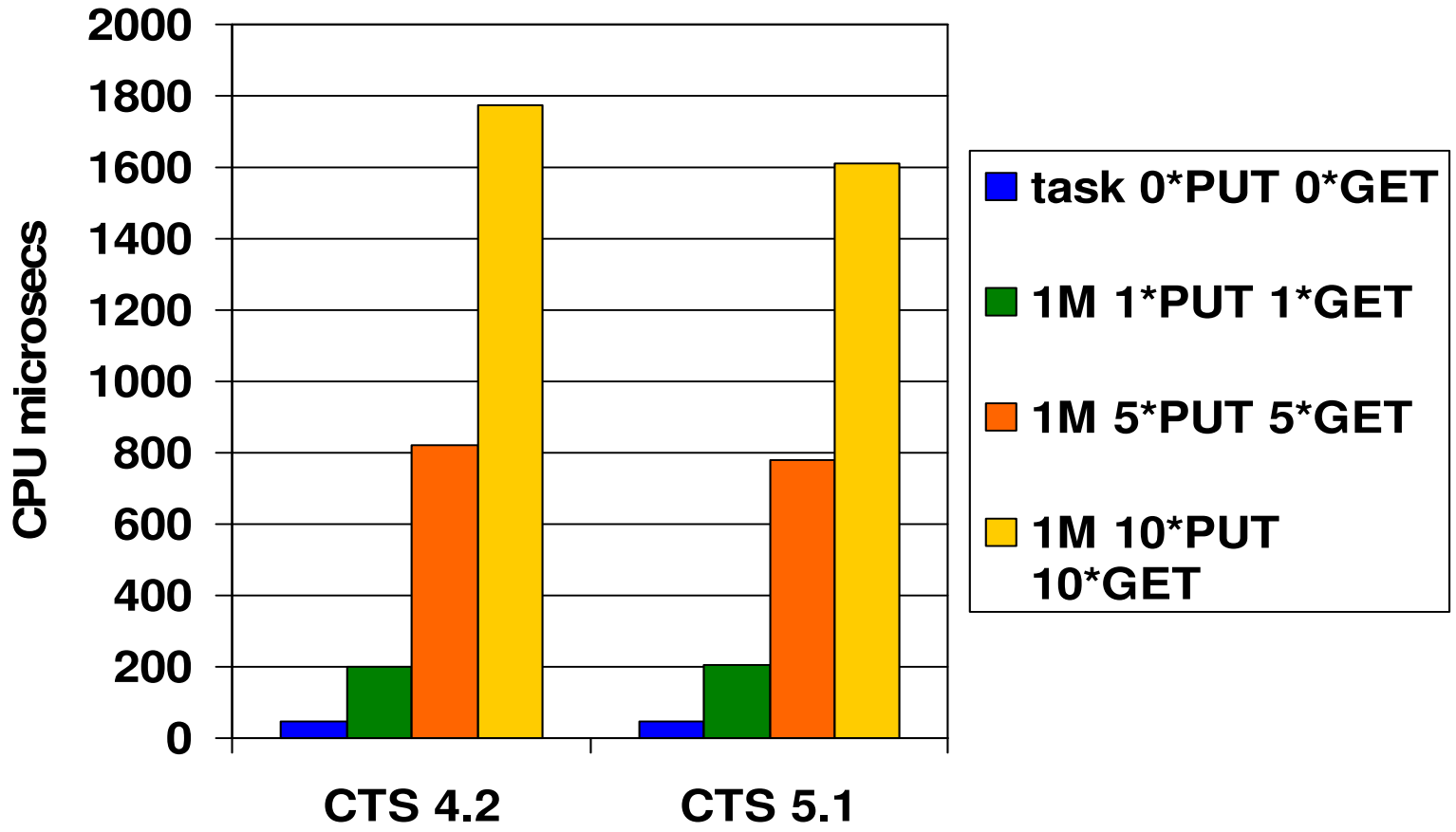
>RETURN

•SEND

•RETURN



CICS TS V4.2 vs CICS TS V51 using Containers



Threadsafe (Backup)

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CONCURRENCY(REQUIRED) - Recap

►My application is USER key, makes DB2 calls, it is threadsafe and I want it to start and stay on a Open TCB. STGPROT=YES

►If I make it API(CICS)

•It starts on the QR ...

•… the first DB2 call puts it on the L8 ...

•… but if it meets a non-threadsafe CICS command it goes back to the QR and stays there until the next DB2 call

►If I make it API(OPEN)

•It starts on an L9 (user key) …

•… but causes TCB switches on each DB2 call (L9 → L8 → L9)

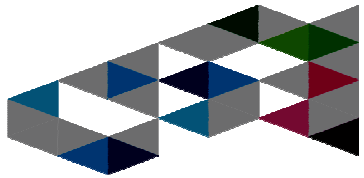
►If I make if API(CICS) and CONCURRENCY(REQUIRED)

•It starts on an L8 …

•… if it meets a non-threadsafe CICS command it goes back to the QR but then immediately returns to L8

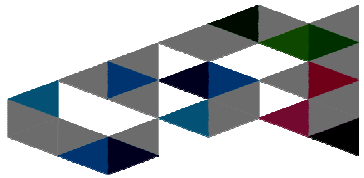
Threadsafe

- Threadsafe Transient Data Commands
  - EXEC CICS READQ TD, WRITEQ TD, and DELETEQ TD
- CICS PROGRAM LOADS
- Function Shipping over IPIC will use an Open TCB
  - Also drive the mirror on open TCB
- JDBC calls do not need to switch to L8 TCB
- Additional SPI commands now threadsafe
  - EXEC CICS SET TASK
  - EXEC CICS INQUIRE and SET TRACEDEST/TRACEFLAG/TRACETYPE



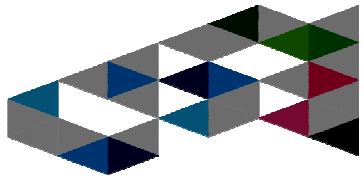
Threadsafe SPI Commands V5.1

- TASK (SET)
- TRACEDEST (INQUIRE / SET)
- TRACEFLAG (INQUIRE / SET)
- TRACETYPE (INQUIRE / SET)



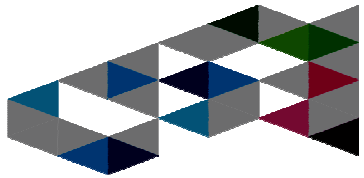
Threadsafe SPI Commands V5.2

- MONITOR (INQUIRE / SET)
- STATISTICS (EXTRACT / INQUIRE / SET)
- PROGRAM (INQUIRE / SET / DISCARD)
- TRANSACTION (INQUIRE / SET / DISCARD)
- SYSTEM (INQUIRE / SET)
- DISPATCHER (INQUIRE / SET)
- MVSTCB (INQUIRE)



Program Load (V5.1)

- When running on an open TCB and a CICS program load is requested there is no longer a TCB switch to the RO TCB
  - EXEC CICS LINK, LOAD, XCTL, …
- CICS RO TCB will still be used for …
  - CICS program LOADs when NOT running on an Open TCB
  - DFHRPL and LIBRARY Dataset Management
- Updated Loader global statistics
  - New statistics on RO TCB program load requests
  - Load time recorded by module
- Benefits …
  - Reduced contention for the single CICS RO TCB
  - Reduced pathlength – RO TCB switch eliminated
  - Significantly increased potential CICS program LOAD capacity



Java
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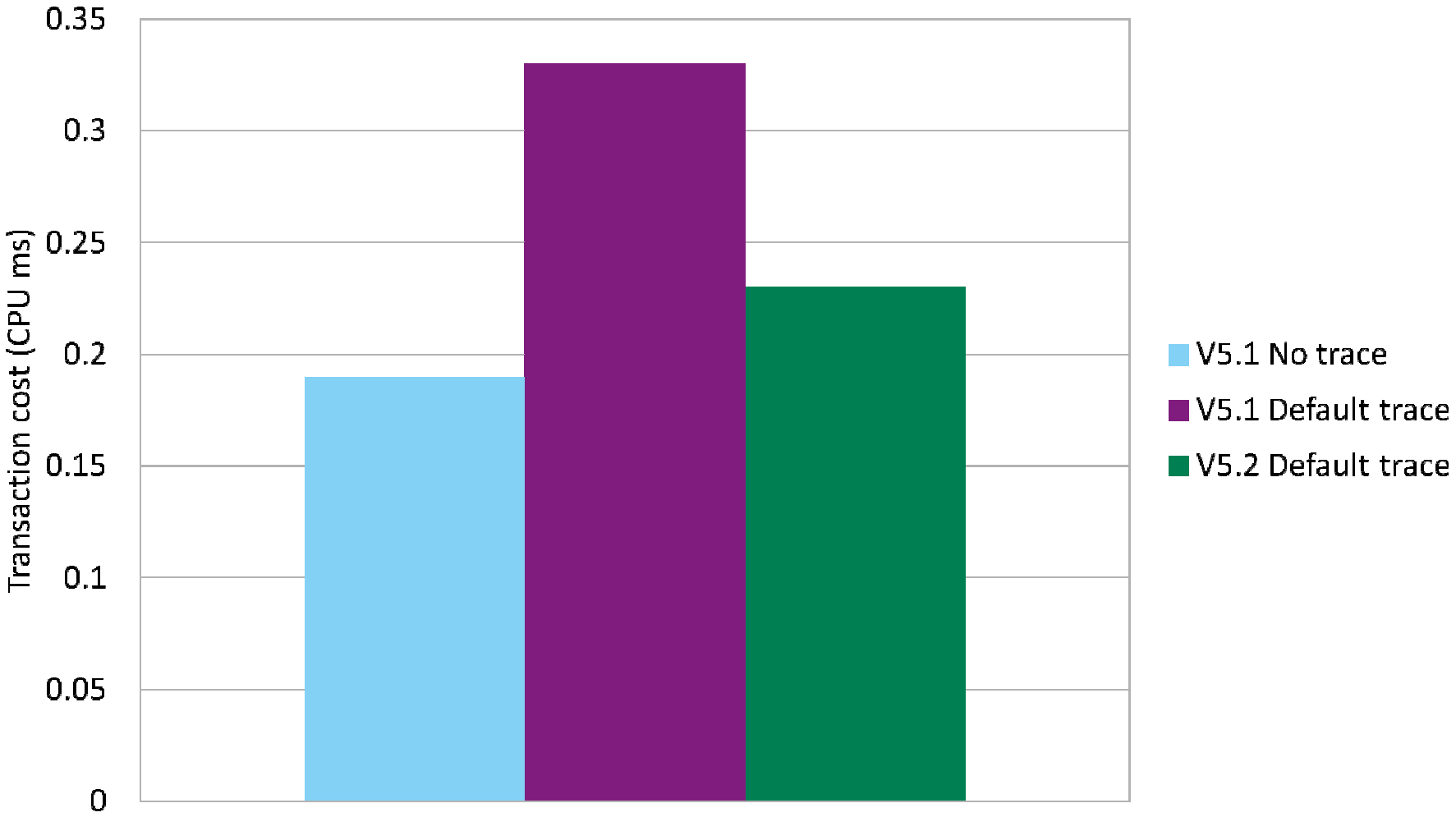
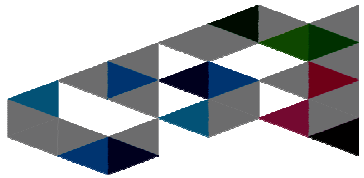
CICS Java Hello World Sample



jdbc calls without switching to L8 TCB

CICS release	Avg User CPU time (ms)	Avg QR CPU time (ms)	Avg T8 CPU time (ms)	Avg L8 CPU time (ms)	Avg TCB switch count
V4.2	4.374	0.310	2.907	1.157	300
V5.1	4.230	0.322	3.844	0.064	202

- Using same jdbc application as previous slide
- Overall transaction CPU reduced
- Task switches reduced
- jdbc calls shifted from L8 to T8 TCBs



Improved Instrumentation (Backup)

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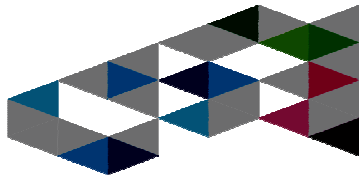
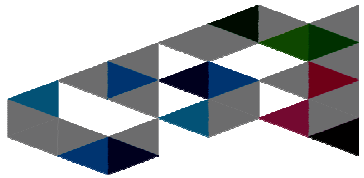
Instrumentation – Wait analysis

- Improved transaction Wait times
  - MRO/ISC Allocate Waits
  - IPIC Allocate Waits
  - RO TCB and SO TCB Mode Delays
  - Intrapartition and Extrapartition TDQueue Lock Waits
    - TDIPLOCK TDEPLOCK
  - File Control Exclusive Control Waits
    - (Previously only in stats)
  - VSAM File String Waits
    - (Previously only in stats)



Instrumentation …

- zIIP/zAAP speciality processor transaction CPU time
- Physical hardware environment
  - CEC Machine Type and Model ID
    - e.g. 2097-740
- Transaction performance related to CICS region load
  - Current active task count and MXT setting (CURTASKS)
- Policy
  - Policy threshold exceeded count



Instrumentation ….

►Inbound SSL CIPHER code

•Inbound SSL ciphers used are now recorded in SMF 110 CMF performance class records for better performance analysis

►Application Context

•Application name

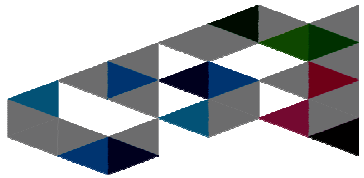
•Platform name

•Operation name

•Major, Minor, and Micro version numbers

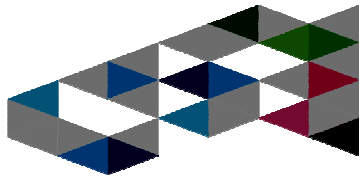
►Monitoring RMI Data Collection Option

•Default changed from RMI=NO to RMI=YES



Instrumentation …

- 64-bit Application Task and Shared Storage Usage
  - Task Storage – CICS-key, User-key, …
    - GETMAIN request count, Storage High Water Mark, …
  - Shared Storage …
    - GETMAIN request count, Bytes GETMAINed, Bytes FREEMAINed, …
- Resource Class data enhancements
  - File entry
    - File Exclusive control conflict wait time
    - VSAM string wait time
- Exception Class data enhancements
  - Storage Waits in GCDSA, GUDSA, and GSDSA

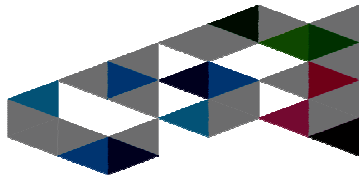


Instrumentation …

- –zAAP/zIIP Specialty Processor Transaction CPU time
- –Existing CMF Performance Class Field …
  - »a) “USRCPUT” → Total CPU time used including Standard CP and zAAP/zIIP times
- –New CMF Performance Class Fields …
  - »b) “CPUTONCP” → Total CPU time on standard CP
  - »c) “OFFLCPUT” → Total Offload CPU time on standard CP (Offload eligible but ran on standard CP)
- –From the new metrics the following can also be derived …
  - »d) Total CPU time on zAAP/zIIP = (USRCPUT – CPUTONCP)
  - »e) Total CPU time on CP that was not offload = (CPUTONCP – OFFLCPUT)
  - »f) Total CPU time offload eligible = (OFFLCPUT + d)
- –Requires …
  - »z/OS R13 APAR OA38409 and IBM System z9 or later

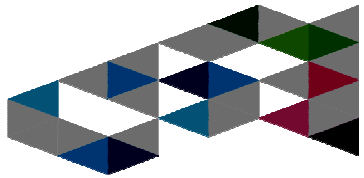
Notable Metrics Enhancements – V5.2

- Timestamp of last user transaction attach
- Timestamp when the MXT limit parameter was last set or changed
- Timestamp of when we last reached the MXT limit
- Indicator that we are still at MXT limit
- Timestamp of last Excess TCB scan
- Timestamp of last Excess TCB scan – No TCB Detached
- Current number of dispatchable tasks
- Peak number of dispatchable tasks
- Average number of dispatchable tasks



Notable Metrics Enhancements – V5.2

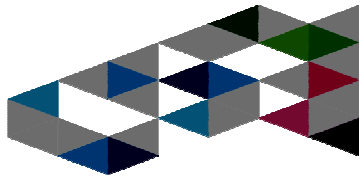
- Level 1 bullet
- Level 1 bullet
  - Level 2 bullet
  - Level 2 bullet
    - Level 3 bullet



New in CICS TS V5.2

- Total number of tasks that waited for a CICS TCB
- Total wait time for the tasks that are currently waiting for a CICS TCB

- Timestamp of when last at ‘at TCB Pool Limit’



Notable Metrics Enhancements – V5.2

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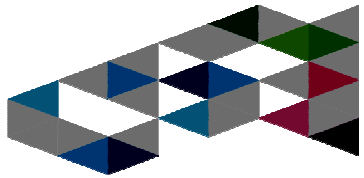
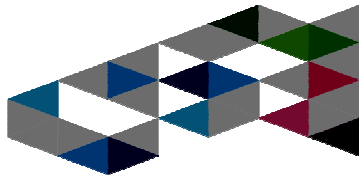


New in CICS TS V5.2

- Number of user transaction completions (#completions)
- Timestamp of last user transaction completion
- Timestamp of last user transaction attach

- Number of system transaction completions
- MXT value at last user transaction attach
- Current user tasks at last user transaction attach

- Rolling average user transaction response time calculated as:- (((current average user response time * #completions) + this response time) / (#completions +1))
- Maximum user transaction response time



CICS Performance Analyzer (Backup)

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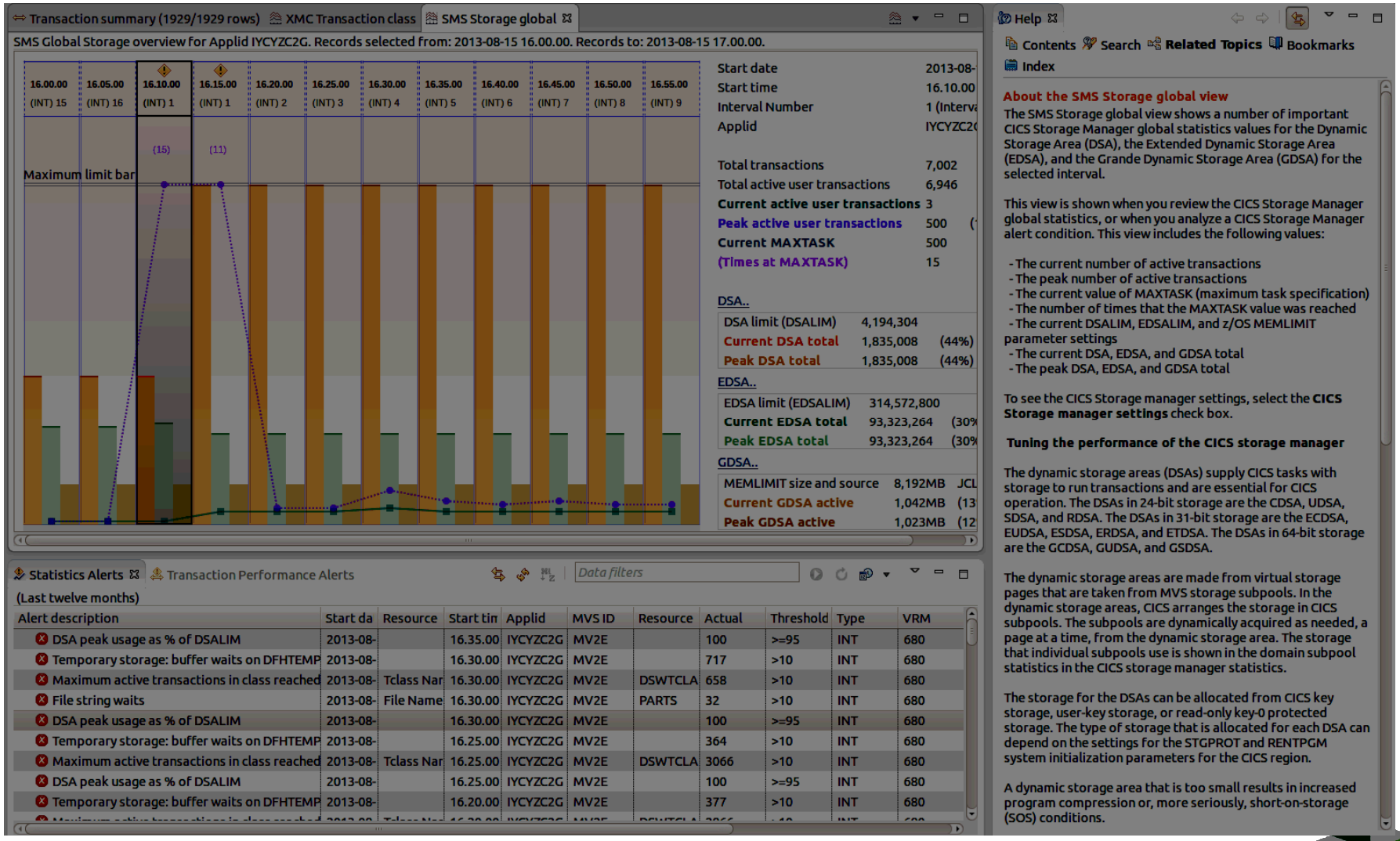
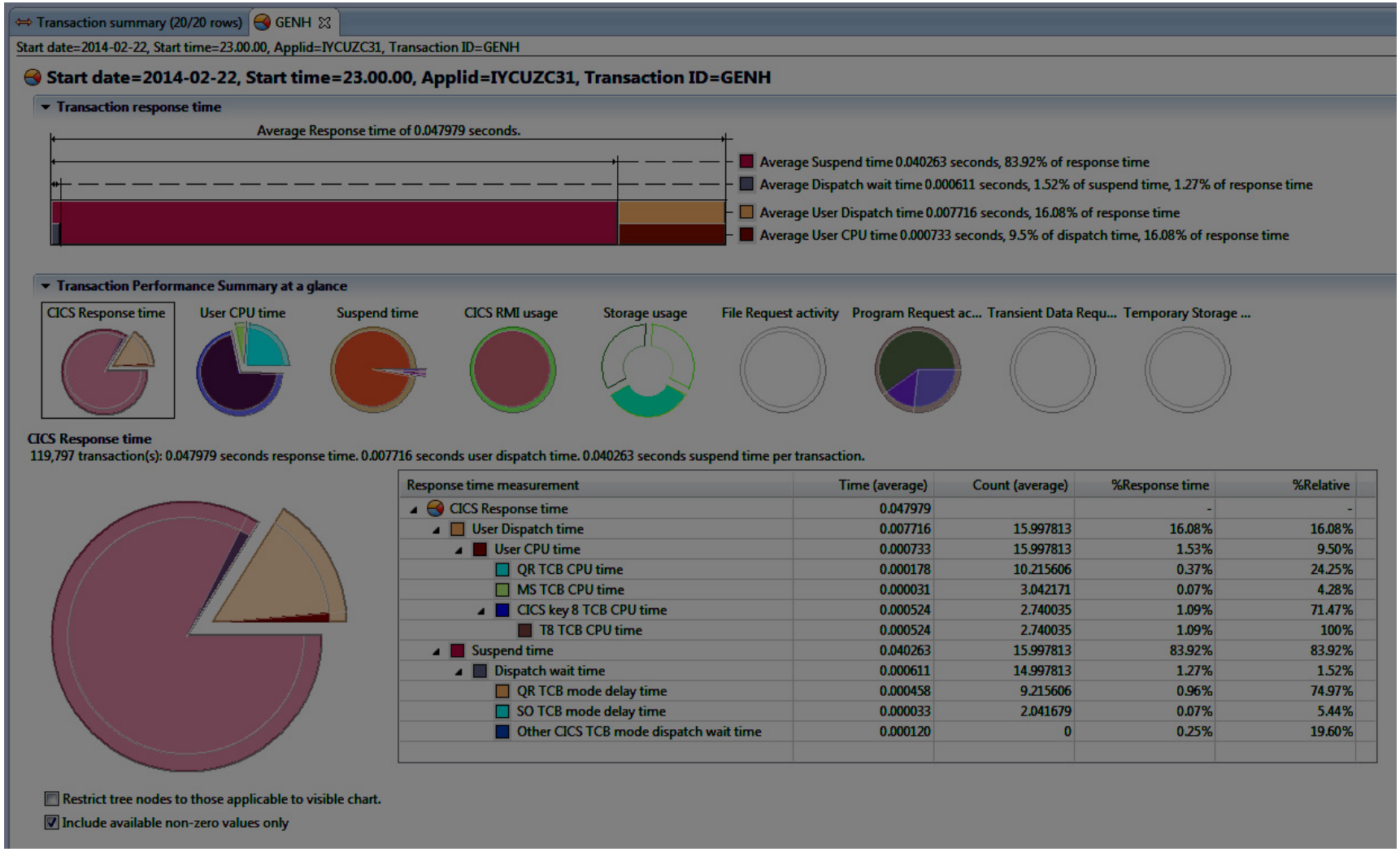
Performance Alerts

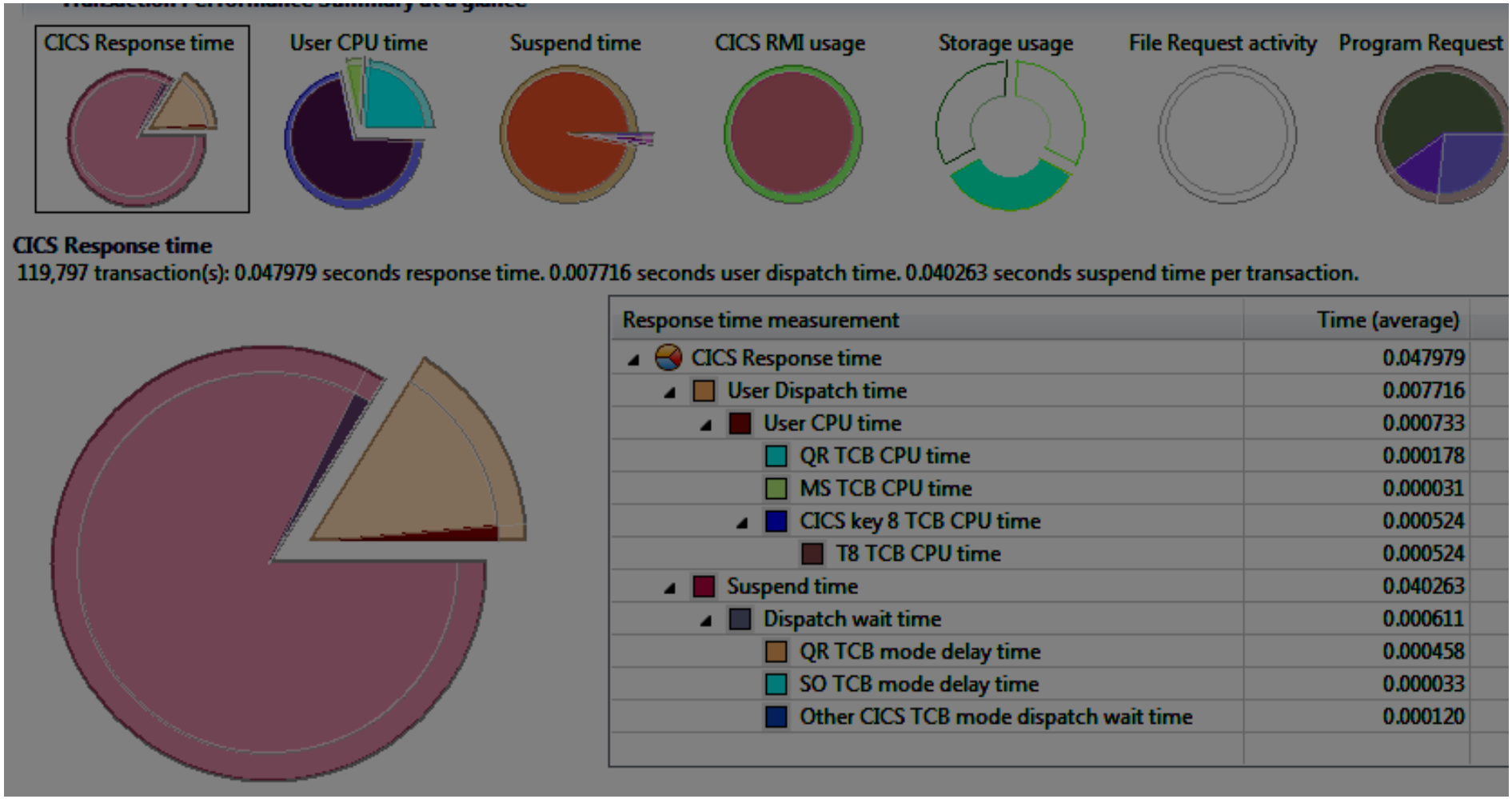


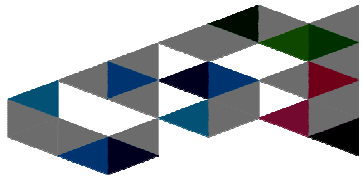
CICS Performance Analyzer – High level



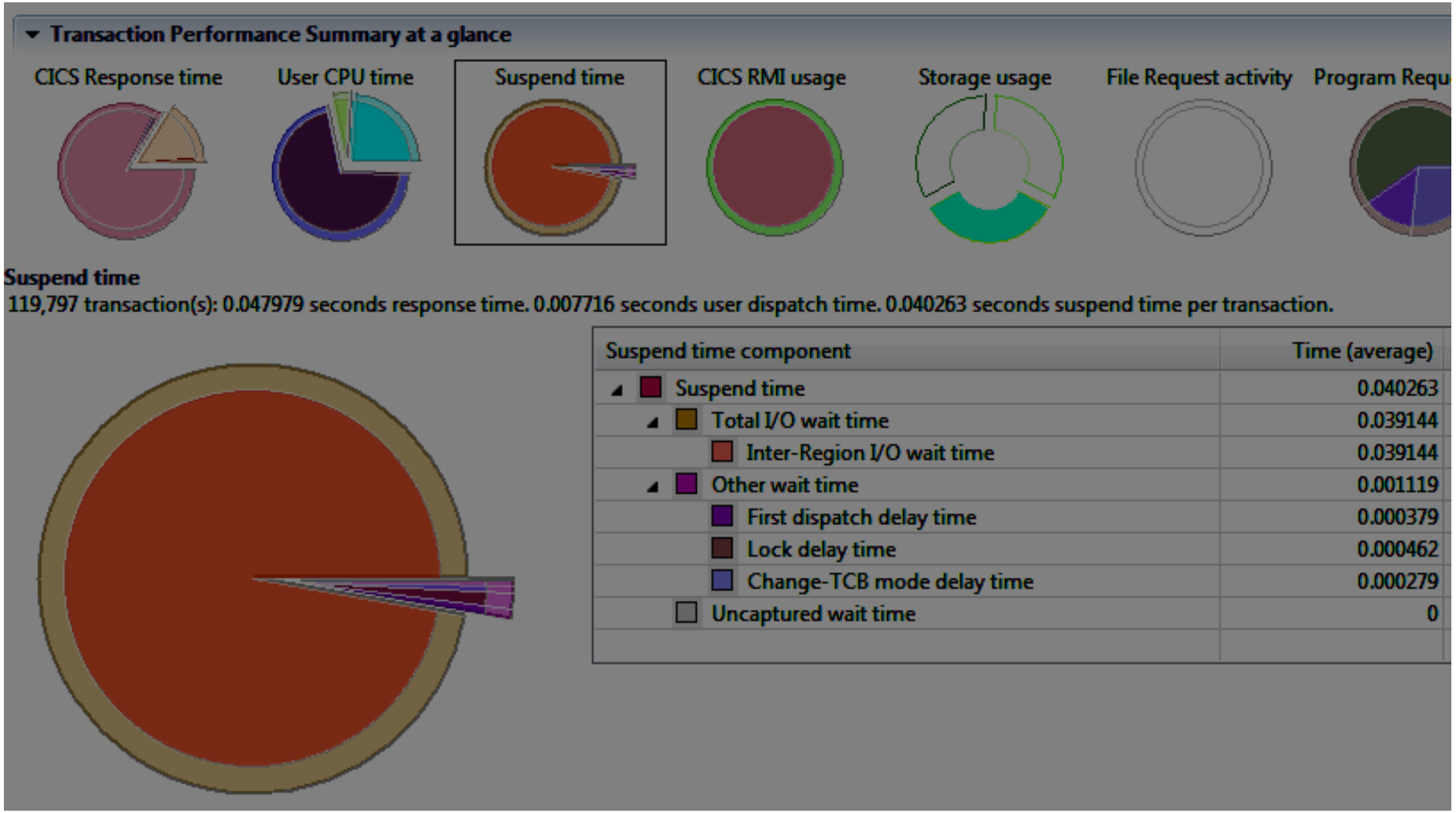
Response time measurement	Time (average)	Count (average)	%Response time	%Relative
CICS Response time	0.047979		-	-
User Dispatch time	0.007716	15.997813	16.08%	16.08%
User CPU time	0.000733	15.997813	1.53%	9.50%
QR TCB CPU time	0.000178	10.215606	0.37%	24.25%
MS TCB CPU time	0.000031	3.042171	0.07%	4.28%
CICS key 8 TCB CPU time	0.000524	2.740035	1.09%	71.47%
T8 TCB CPU time	0.000524	2.740035	1.09%	100%
Suspend time	0.040263	15.997813	83.92%	83.92%
Dispatch wait time	0.000611	14.997813	1.27%	1.52%
QR TCB mode delay time	0.000458	9.215606	0.96%	74.97%
SO TCB mode delay time	0.000033	2.041679	0.07%	5.44%
Other CICS TCB mode dispatch wait time	0.000120	0	0.25%	19.60%

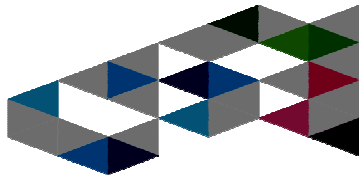
CICS Performance Analyzer – Response Time



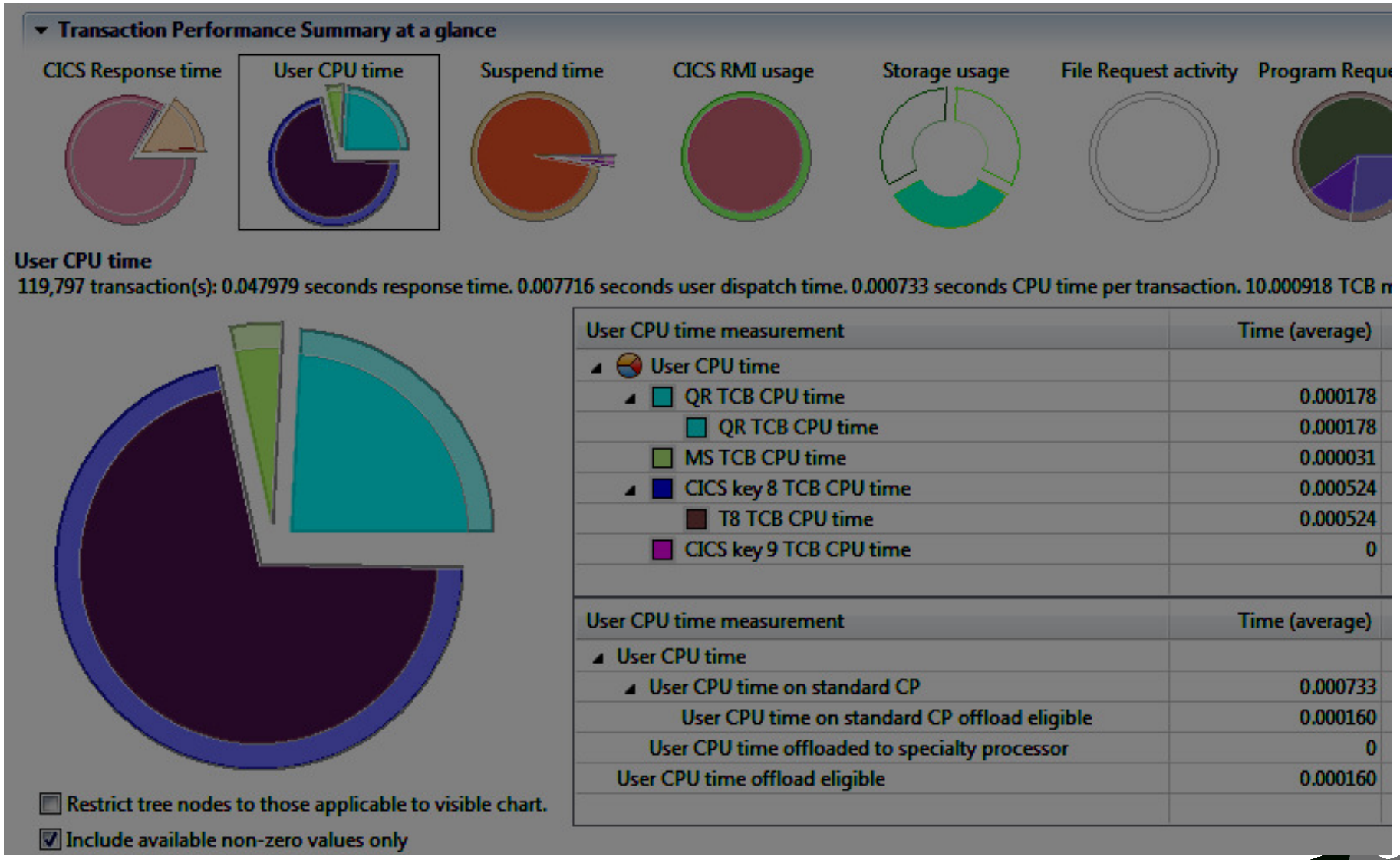


CICS Performance Analyzer – Suspend Time

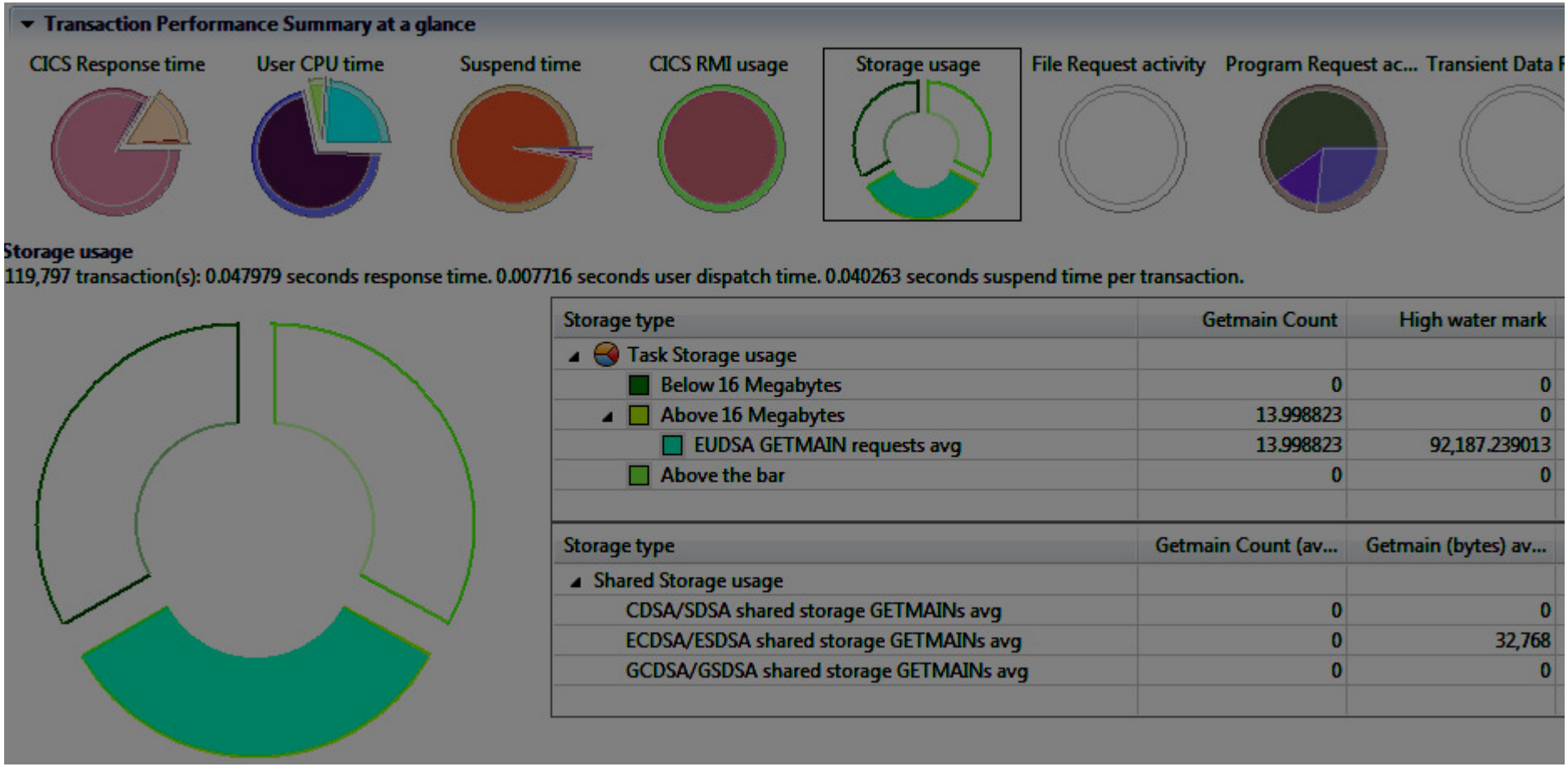


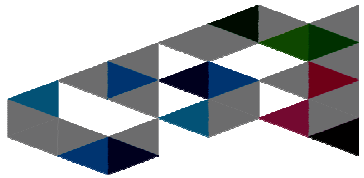


CICS Performance Analyzer – CPU Time

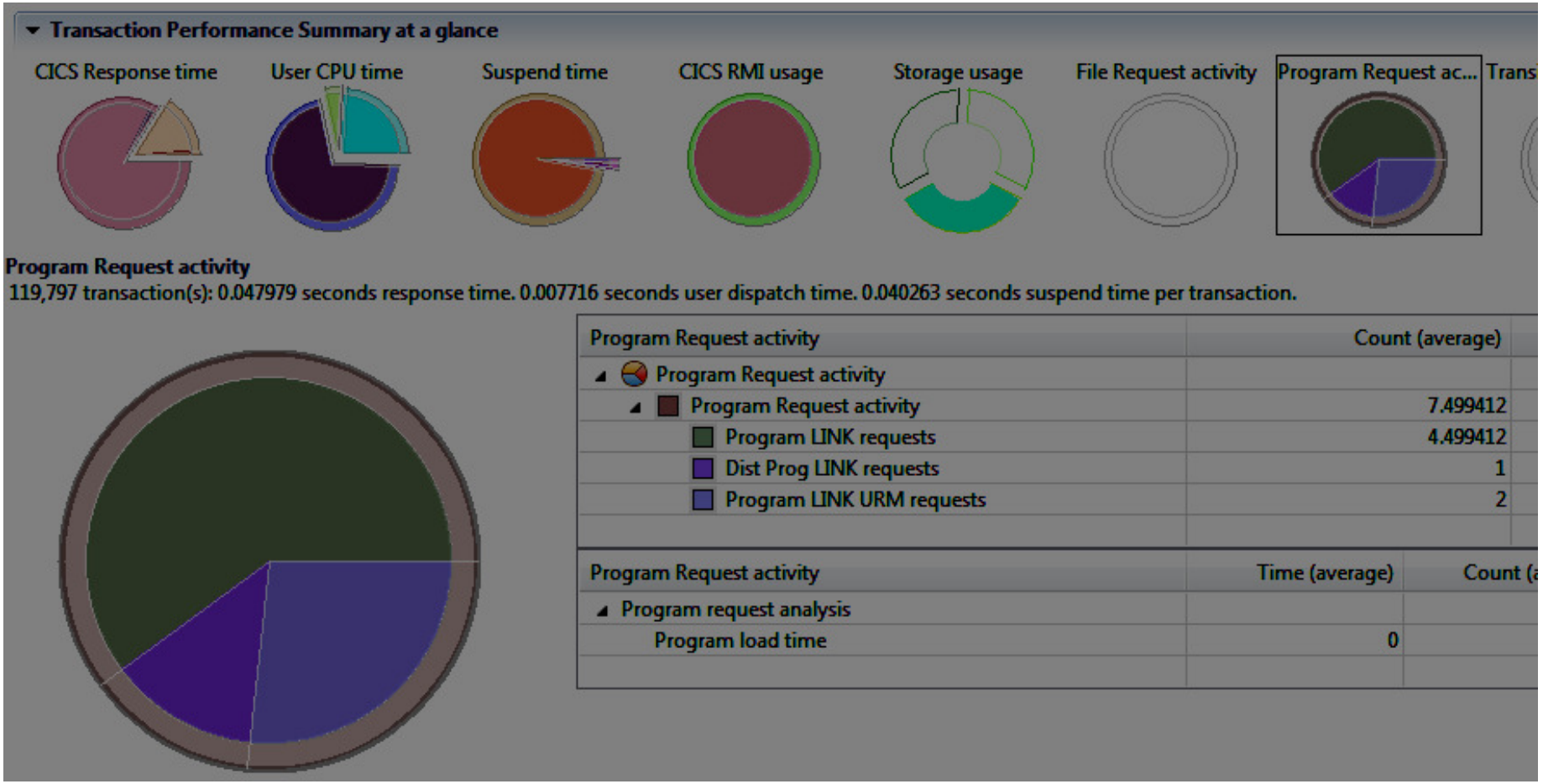


Performance Analysis – Storage Usage (New!)





Performance Analysis – Program Usage (New!)



MQ DPL Bridge (Backup)

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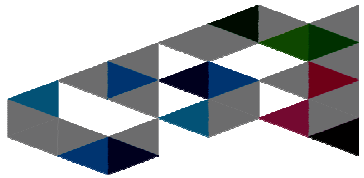
Headline Goes Here

- Level 1 bullet
- Level 1 bullet
  - Level 2 bullet
  - Level 2 bullet
    - Level 3 bullet



CICS MQ DPL Bridge

- MQ DPL Bridge

– this feature enables a client application:

• to invoke a server application running under CICS

• by sending an MQ message

– data passed to server app on a LINK API command

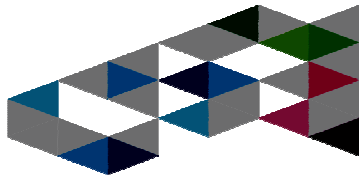
• in a Commarea

– restricted to 32k of data

– to send > 32k requires multi-sends and LINKs per UOW

• in a Container

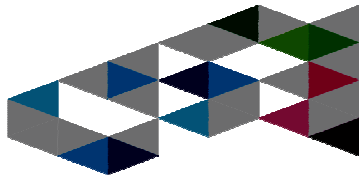
– new feature



CICS MQ DPL Bridge

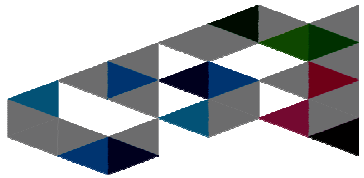
►Transactions and MQ calls

- CKBR
  - –CICS Bridge Monitor transaction – long running task
- CKBP (for Commareas) or CKBC (for Containers)
  - –CICS DPL Bridge task
  - –Transactions started by CKBR bridge monitor
  - –Invokes CICS DPL program(s)
- MQ calls issued
  - –CKBR MQGET BROWSE WAIT
  - –CKBP/CKBC MQOPEN and MQGETs
  - –1 MQGET per inbound message within the UOW
  - –CKBP/CKBC MQOPEN and MQPUTs (when reply-to-queue specified)
  - –1 MQPUT per outbound message sent within the UOW
  - –MQPUT1 used when only 1 outbound message per UOW

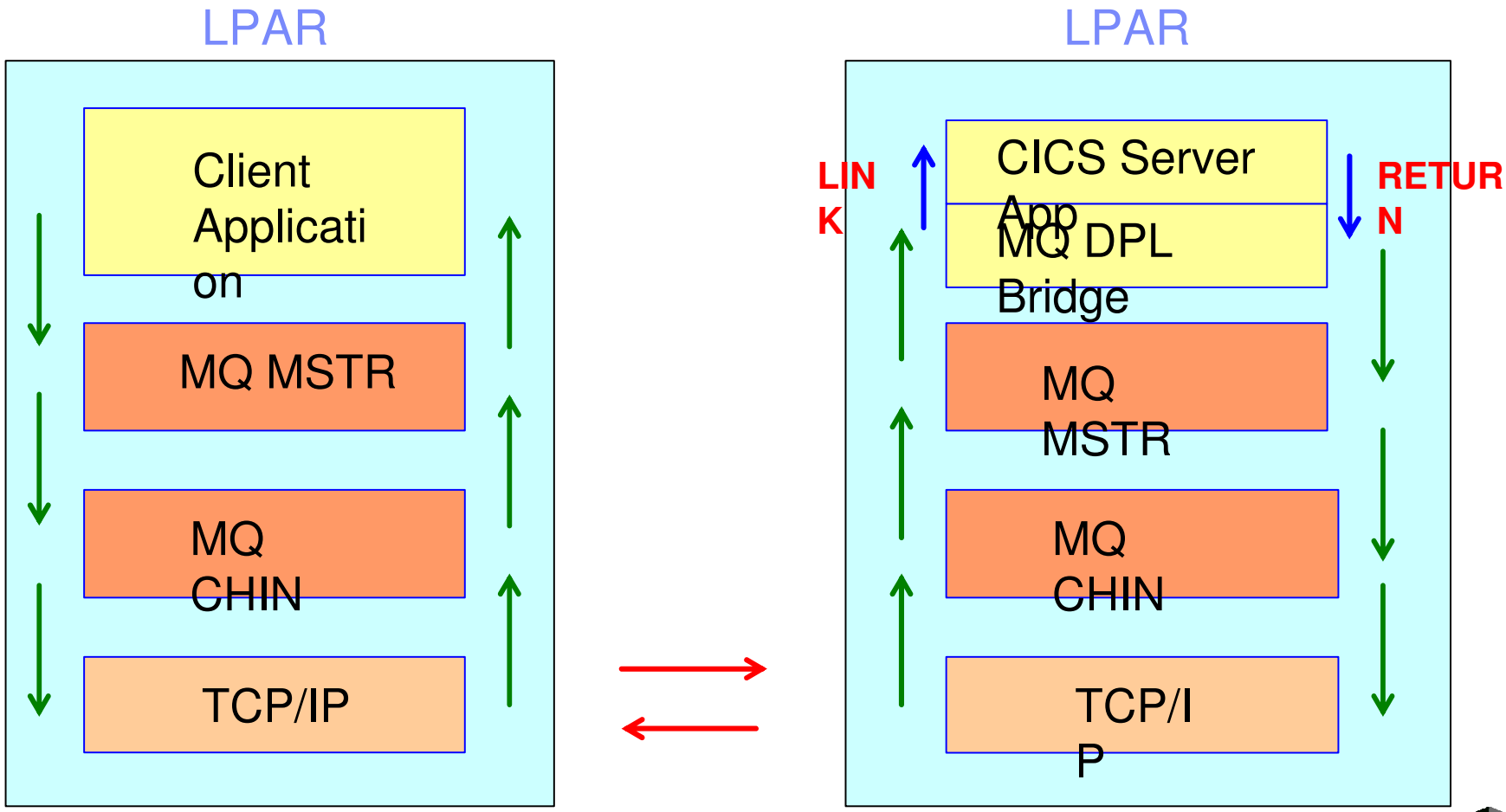


CICS MQ DPL Bridge

- Performance environment
  - TPNS used to drive clients
  - clients run in separate LPAR from CICS server app
  - MQ DPL request and data sent:
    - from an MQ subsystem on the client LPAR
    - to an MQ subsystem on the CICS server app LPAR
    - using TCP/IP
  - data returned to client of same size as data sent
  - CPU usage on CICS Server LPAR is measured



CICS MQ DPL Bridge performance environment



CICS MQ DPL Bridge

►MQ messages

•message sizes used:

–32k

–256k

–1Meg

•using containers a single message is sent and received

•using commareas:

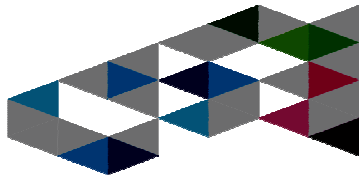
–a single 32k message is sent and received for the 32k scenario

–multiple 32k messages are sent and received for the 256k and 1Meg scenarios

–note that the server app will be linked to multiple times for these 2 scenarios

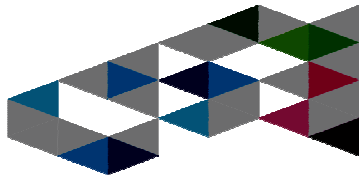
CICS MQ DPL Bridge

- Total CPU costs
  - additional CPU costs are shown on the next slide
  - CICS CPU
  - MQ Master address space CPU
  - MQ Channel Initiator address space CPU
  - TCP/IP CPU



Summary

- MQ DPL Bridge - Commareas vs Containers
  - message sizes < 32k
    - CPU and response times similar
  - message sizes > 32k
    - due to multiple messages required to be sent for Commareas:
      - significant CPU reduction using Containers
        - >46% CICS CPU reduction for 1Meg messages
        - >60% total CPU reduction for 1Meg messages
      - substantial response time improvements using Containers
        - >e.g 233ms vs 25ms for the 1meg scenario



SMC-R
(Backup)

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RDMA (Remote Direct Memory Access) Technology Overview

Key attributes of RDMA

–Enables a host to read or write directly from/to a remote host's memory ***without*** involving the remote host's CPU

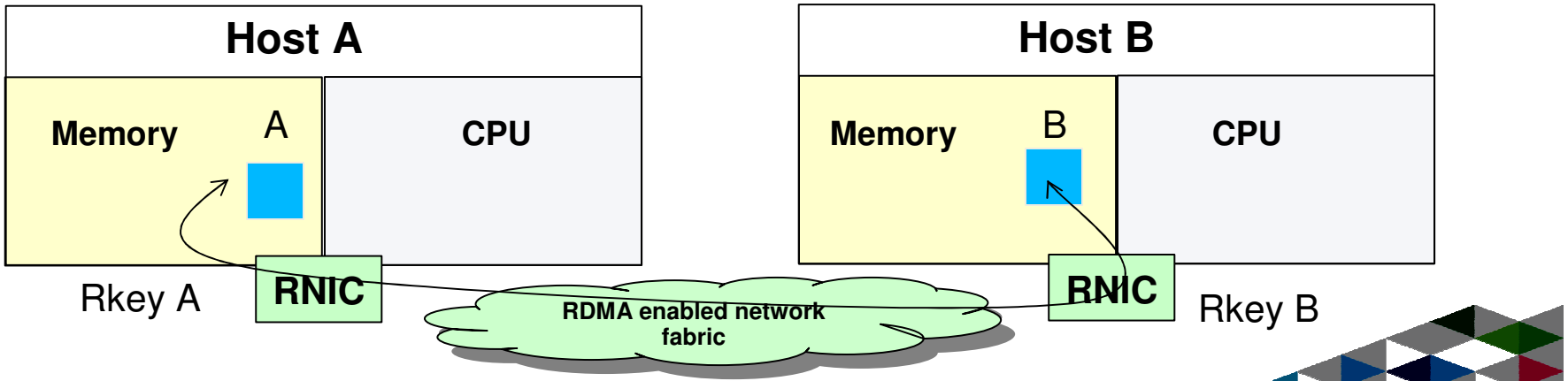
–By registering specific memory for RDMA partner use

–Interrupts ***still required*** for notification (i.e. CPU cycles are not completely eliminated)

–Reduced networking stack overhead by using streamlined, low level, RMDA interfaces

–Key requirements:

- A reliable "lossless" network fabric (LAN for layer 2 data center network distance)
- An RDMA capable NIC (RNIC) and RDMA capable switched fabric (switches)

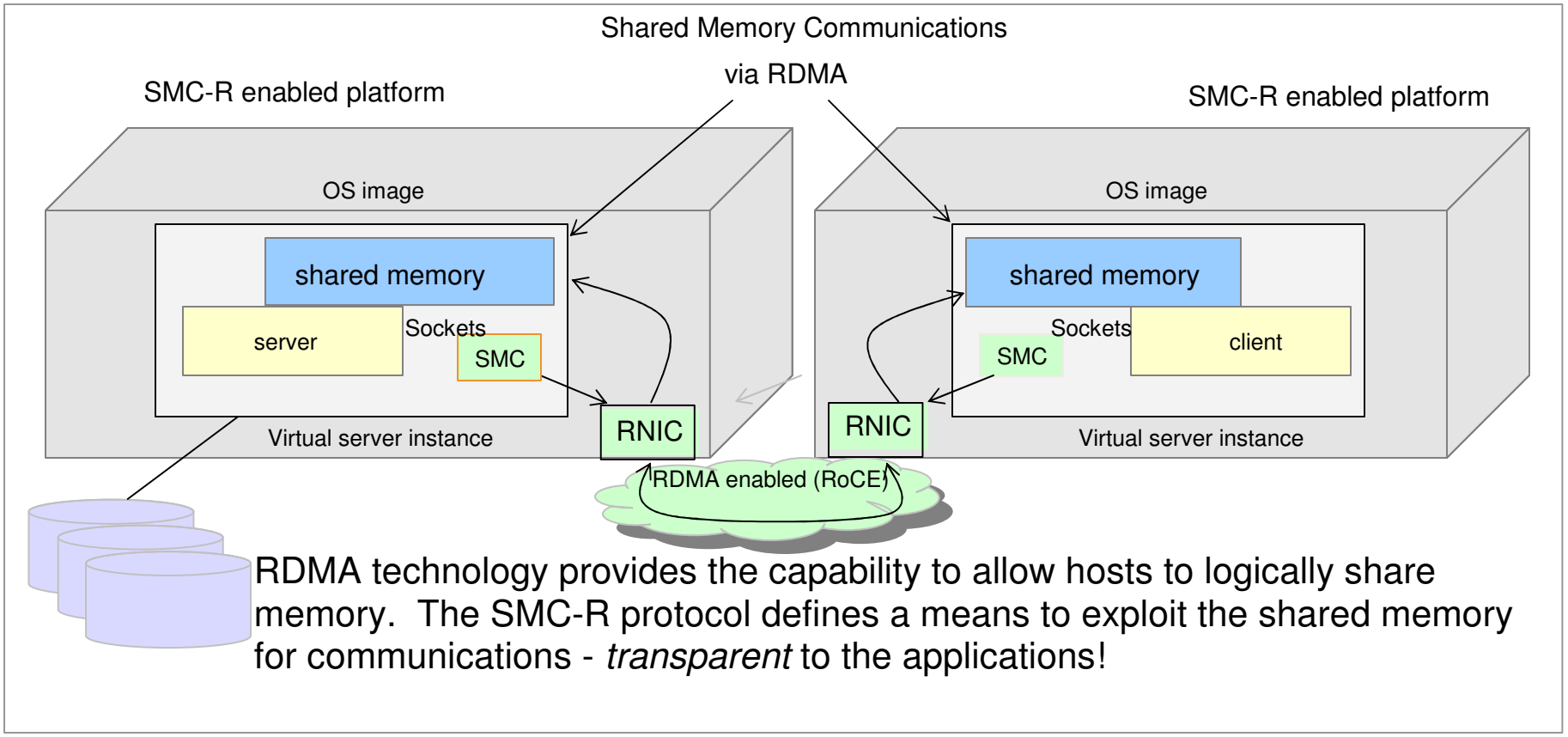


RoCE - RDMA over Converged (Enhanced) Ethernet

- RDMA based technology has been available in the industry for many years – primarily based on Infiniband (IB)
  - IB requires a completely unique network eco system (unique hardware such as host adapters, switches, host application software, system management software/firmware, security controls, etc.)
  - IB is popular in the HPC (High Performance Computing) space
- RDMA technology is now available on Ethernet – RDMA over Converged Ethernet (RoCE)
  - RoCE uses existing Ethernet fabric but requires advanced Ethernet hardware (RDMA capable NICs and RoCE capable Ethernet switches)
  - ***RoCE is a game changer!***
  - ***RDMA technology becomes more affordable and prevalent in data center networks***
- Host software exploitation options fall into two general categories:

“Shared Memory Communications over RDMA” concepts

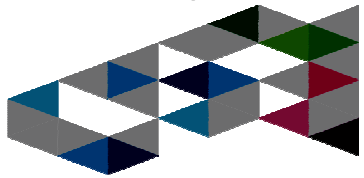
Clustered Systems



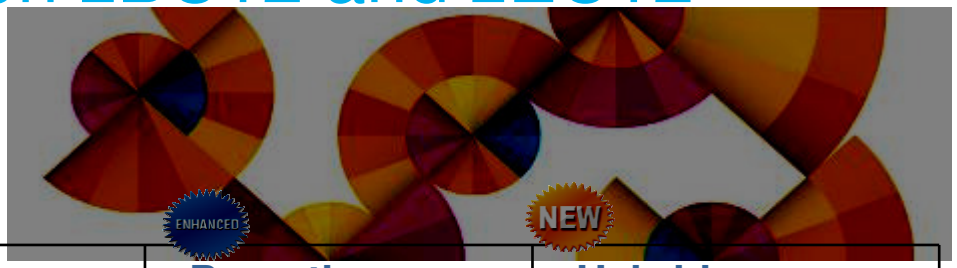
RDMA technology provides the capability to allow hosts to logically share memory. The SMC-R protocol defines a means to exploit the shared memory for communications - *transparent* to the applications!

This solution is referred to as *SMC-R* (Shared Memory Communications over RDMA). SMC-R is an *open* sockets over RDMA protocol that provides transparent exploitation of RDMA (for TCP based applications) while preserving key functions and qualities of service from the TCP/IP ecosystem that enterprise level servers/network depend on!

Draft IETF (Internet Enginnering Task Force) RFC for SMC-R:
http://tools.ietf.org/html/draft-fox-tcpm-shared-memory-rdma-03



New innovations available on zBC12 and zEC12



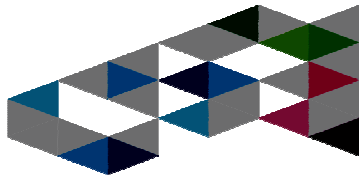
NEW **Data Compression Acceleration**	NEW **High Speed Communication Fabric**	ENHANCED **Flash Technology Exploitation**	**Proactive Systems Health Analytics**	**Hybrid Computing Enhancements**
Reduce CP consumption, free up storage & speed cross platform data exchange	Optimize server to server networking with reduced latency and lower CPU overhead	Improve availability and performance during critical workload transitions, now with dynamic reconfiguration; Coupling Facility exploitation (SOD)	Increase availability by detecting unusual application or system behaviors for faster problem resolution before they disrupt business	x86 blade resource optimization; New alert & notification for blade virtual servers; Latest x86 OS support; Expanding futures roadmap
zEDC Express	*10GbE RoCE Express*	*IBM Flash Express*	*IBM zAware*	

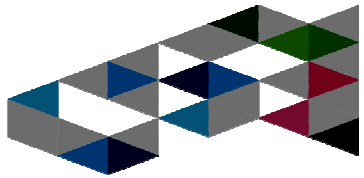
Use cases for SMC-R and 10GbE RoCE Express for z/OS to z/OS communications

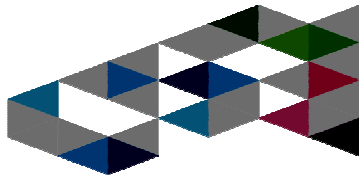
Use Cases

- Application servers such as the z/OS WebSphere Application Server communicating (via TCP based communications) with CICS, IMS or DB2 – particularly when the application is network intensive and transaction oriented
- Transactional workloads that exchange larger messages (e.g. web services such as WAS to DB2 or CICS) will see benefit.
- Streaming (or bulk) application workloads (e.g. FTP) communicating z/OS to z/OS TCP will see improvements in both CPU and throughput
- Applications that use z/OS to z/OS TCP based communications using Sysplex Distributor

Plus … ***Transparent to application software – no changes required!***







SMC-R - RDMA

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- By registering specific memory for RDMA partner use
- **Interrupts still required for notification (i.e. CPU cycles are not completely eliminated)**
- Reduced networking stack overhead by using streamlined, low level, RMDA interfaces
- Key requirements:
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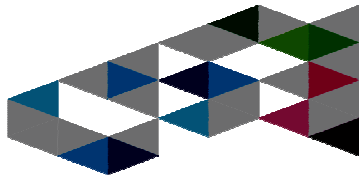
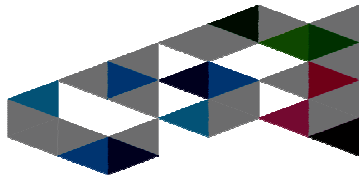


SMC-R - Solution

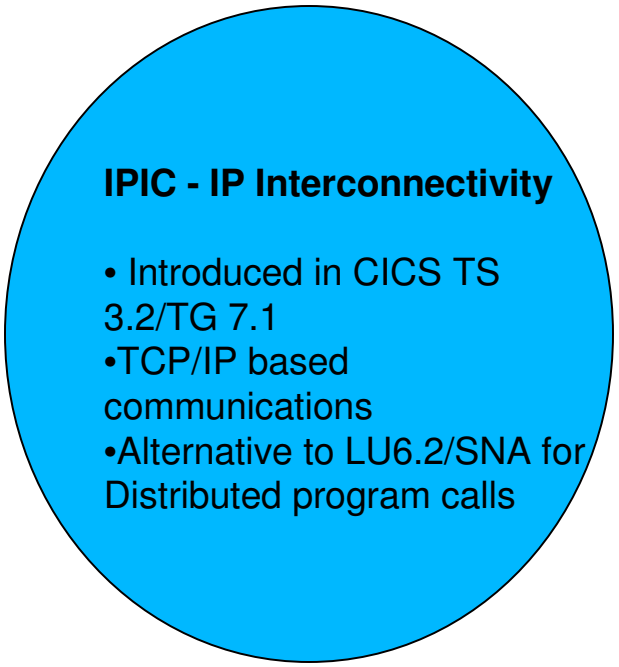
- Shared Memory Communications over RDMA (SMC-R) is a protocol that allows *TCP sockets* applications to transparently exploit RDMA (RoCE)
- SMC-R is a “hybrid” solution that:
- Uses TCP connection (3-way handshake) to establish SMC-R connection
- Each TCP end point exchanges TCP options that indicate whether it supports the SMC-R protocol
- SMC-R “rendezvous” (RDMA attributes) information is then exchanged within the TCP data stream (similar to SSL handshake)
- Socket application data is exchanged via RDMA (write operations)
- TCP connection remains active (controls SMC-R connection)
- This model preserves many critical existing operational and network management features of TCP/IP



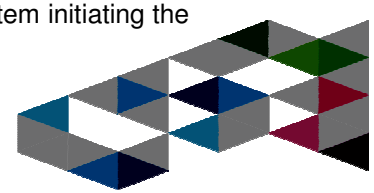
SMC-R – CICS performance improvement

- Response time and CPU utilization improvements
- Workload - Each transaction

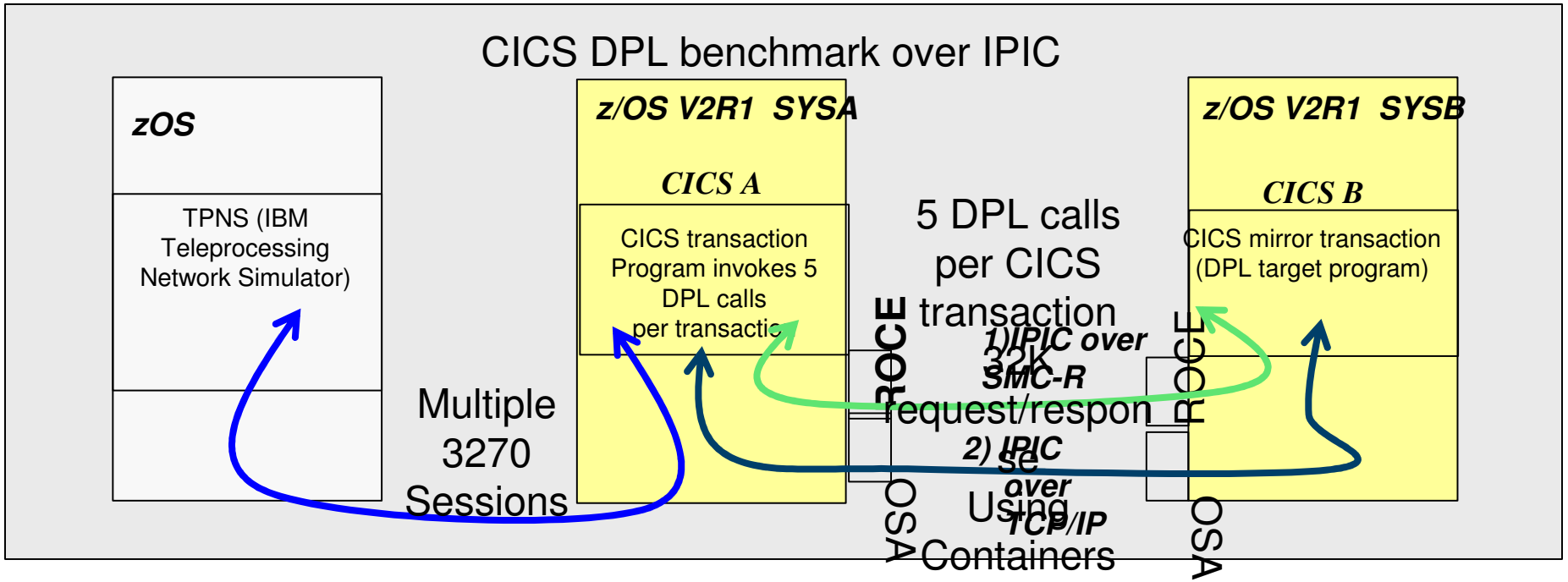
–Makes 5 DPL (Distributed Program Link) requests over an IPIC connection
–Sends 32K container on each request
–Server program Receives the data and Send back 32K
–Receives back a 32K container for each request



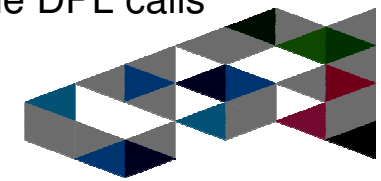
Note: Results based on internal IBM benchmarks using a modeled CICS workload driving a CICS transaction that performs 5 DPL calls to a CICS region on a remote z/OS system, using 32K input/output containers. Response times and CPU savings measured on z/OS system initiating the DPL calls. The actual response times and CPU savings any user will experience will vary.



SMC-R – CICS performance improvement



- Benchmarks run on z/OS V2R1 with latest zEC12 and new 10GbE RoCE Express feature
  - Compared use of SMC-R (10GbE RoCE Express) vs standard TCP/IP (10GbE OSA Express4S) with CICS IPIC communications for DPL (Distributed Program Link) processing
  - ***Up to 48% improvement in CICS transaction response time*** as measured on CICS system issuing the DPL calls (CICS A)
  - ***Up to 10% decrease in overall z/OS CPU consumption*** on CICS system issuing the DPL calls (SYSA)



SMC-R References

- SMC-R Home

•http://www-01.ibm.com/software/network/commserver/SMCR/

- SMC-R Overview

  https://share.confex.com/share/121/webprogram/Session13627.html

- Overview with audio (youtube):

  http://www.youtube.com/watch?v=8_5JviApQXw

- SMC-R Implementation:

  https://share.confex.com/share/121/webprogram/Session13628.html

With audio (youtube):

https://www.youtube.com/watch?v=TN0eS-l1FoE

- Shared Memory Communications over RDMA: Performance Considerations (White Paper)

  http://www-01.ibm.com/support/docview.wss?uid=swg27041273

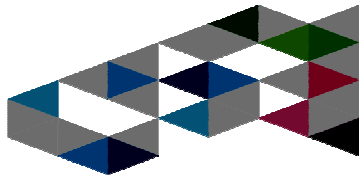
- Performance information:

  https://share.confex.com/share/121/webprogram/Session13633.html

- FAQ:

  https://www-03.ibm.com/support/techdocs/atsmastr.nsf/WebIndex/FQ131485

- RFC:



Workload Consolidation

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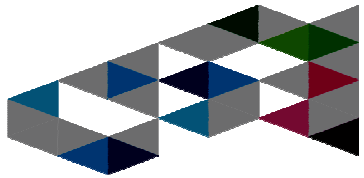
Workload Consolidation

- Run more work through less regions
  - Continual expansion of threadsafe support in V5
  - Further VSCR
  - MXT limit doubled
- Consolidating regions
  - Saves real storage
  - Can save MIPs
  - Saves operational costs



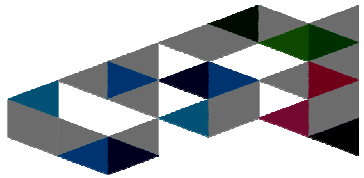
DSW (RLS) consolidation

ETR	CICS %	LPAR %	ms/tran	Real frames
4983.60	253.74%	19.95%	0.640	736,961
6385.12	325.48%	25.35%	0.635	737,319
10135.28	510.46%	39.24%	0.619	738,387
13969.74	704.09%	53.80%	0.616	739,682
15898.14	821.69%	62.53%	0.629	740,917

30 AORs

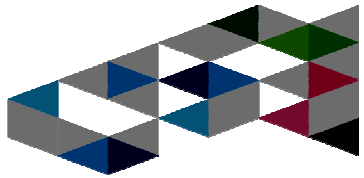
ETR	CICS %	LPAR %	ms/tran	Real frames
4969.95	232.11%	18.09%	0.582	342,299
6390.11	293.22%	22.69%	0.568	342,460
10137.49	456.27%	34.93%	0.551	342,893
13969.68	620.51%	47.22%	0.540	343,470
15867.72	725.80%	55.26%	0.557	343,775

10 AORs



Hardware Instrumentation Data (DSW)

	30 AORs	10 AORs	Delta
Execution Samples	2487298	2201099	-11%
Instruction First Cycle (IFC)	379000	371470	-2%
Micro Seconds per transaction	628.34	556.43	-11%
Cycles per instruction	6.53	5.90	-10%
MIPS per CP	797	882	+10%
Data cache misses (samples)	744894	608550	-18%
Instruction cache miss includes TLB miss	90483	66626	-26%
% Cycles used by TLB misses	6.82	5.94	-13%
Relative Nest Intensity (RNI)	0.48	0.34	



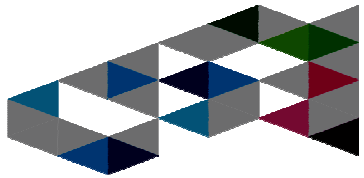
GENAPP (WebServices) consolidation

ETR	CICS %	LPAR %	ms/tran	Real frames
828.31	94.85%	37.47%	1.145	862,739
992.14	114.24%	44.94%	1.151	873,593
1237.67	139.43%	54.45%	1.126	880,690
1633.98	185.24%	71.92%	1.133	897,041
1883.25	233.38%	89.69%	1.239	959,291

30 AORs

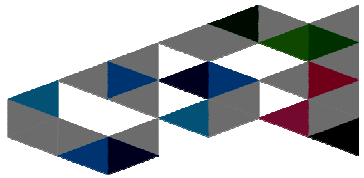
ETR	CICS %	LPAR %	ms/tran	Real frames
827.72	86.42%	34.26%	1.044	381,422
986.51	104.35%	41.20%	1.057	389,384
1231.89	129.67%	50.90%	1.052	394,495
1629.05	166.94%	65.07%	1.024	399,247
1916.36	209.88%	81.54%	1.095	464,827

10 AORs



Hardware Instrumentation Data (GENAPP)

	30 AORs	10 AORS	Delta
Execution Samples	3517830	3188565	-9%
Instruction First Cycle (IFC)	589236	590667	+2%
Micro Seconds per transaction	1240	1095	-11%
Cycles per instruction	5.97	5.39	-10%
MIPS per CP	898	1003	+11%
Data cache misses (samples)	1145876	932896	-18%
Instruction cache miss includes TLB miss	149468	115015	-23%
% Cycles used by TLB misses	9.95	9.23	-7%
Relative Nest Intensity (RNI)	0.75	0.51	



Application Packaging (Backup)

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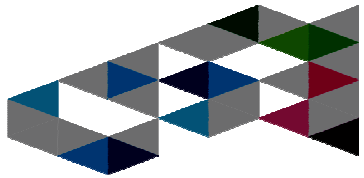
Application Packaging in CICS TS V5.1

- CICS V5.1 introduces a new way of packaging and managing the CICS resources that comprise an application as a single entity
- Using CICS Explorer for definitions:-
  - create a CICS Bundle project declaring resources and optionally dependencies
  - create a Platform bundle that includes existing CICSPlex SM system groups
  - create an Application project that includes bundles of resources
  - create an Application Binding project that associates an Application project with a Platform bundle
  - export Application binding to zFS – which copies referenced CICS bundles to the target zOS system
  - create an Application Definition which defines to CICSPlex SM the zFS location of the bundles copied in the Application binding export
- Similar functionality to CPSM BAS

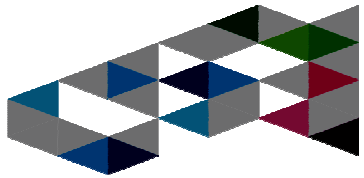
Headline Goes Here

- Level 1 bullet
- Level 1 bullet
  - Level 2 bullet
  - Level 2 bullet
    - Level 3 bullet



Application Lifecycle

- Use CICS Explorer to control a packaged Application
  - deploy by ***export***ing Application
    copies bundles to zFS
  - ***install***
    create all resources in the Application in all target CICS regions contained in platform
  - ***enable***
    enables all resources
  - ***disable***
    disable all resources
  - ***discard***
    remove all the resource definitions created by the Install process



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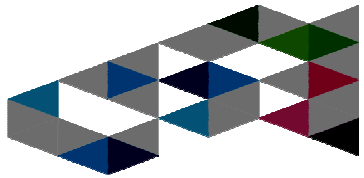
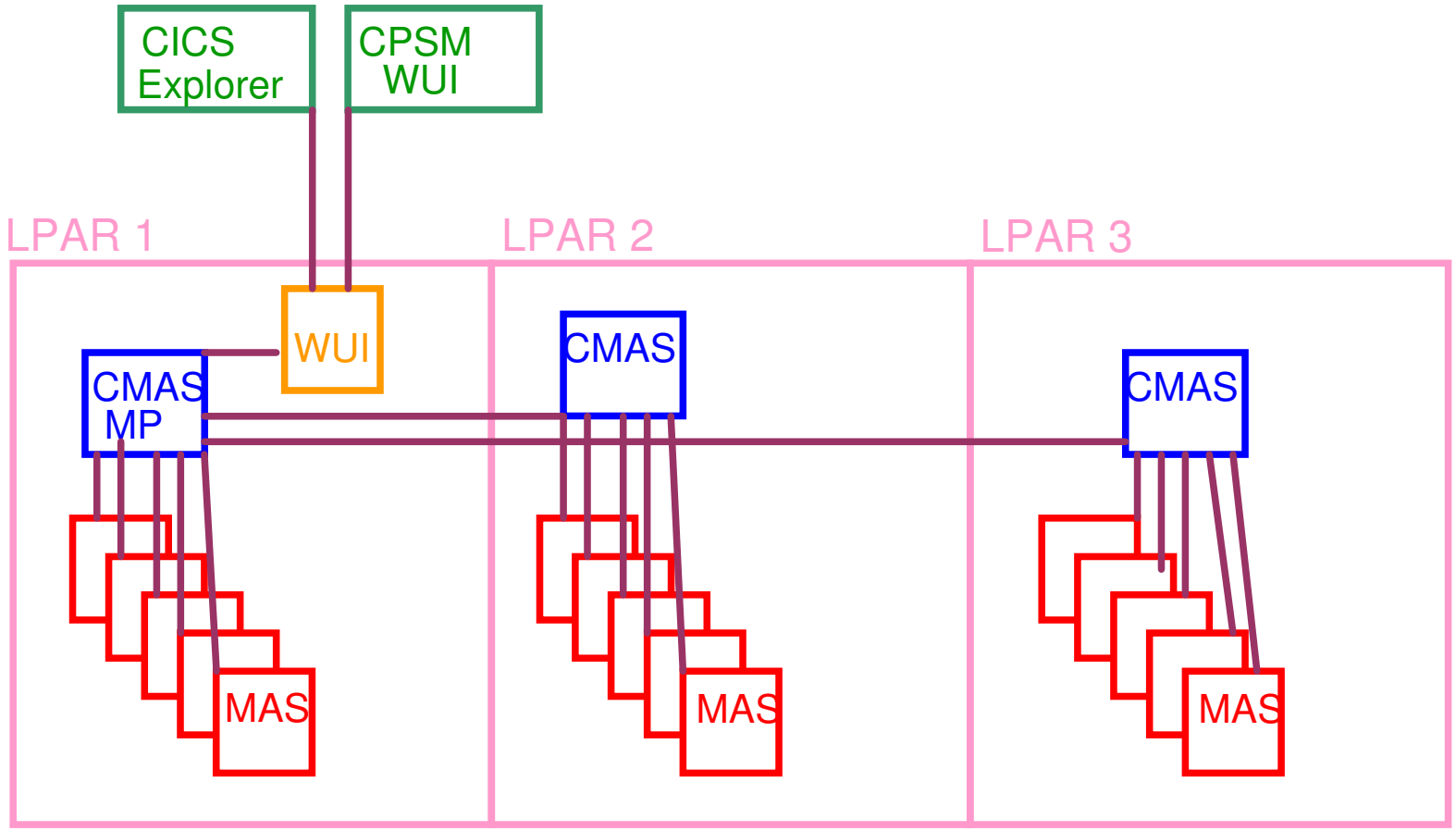
    - Level 3 bullet



Measurement Environment



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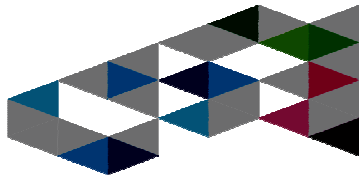
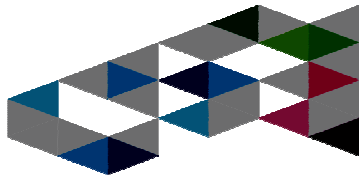


Measurement Environment

- Application
  - Application project comprises 100 CICS bundles
  - Each CICS bundle contains a PROGRAM, LIBRARY, TRANSACTION and URIMAP resource
  - Platform comprises 30 CICS regions, 10 on each LPAR
  - Installing the Application created 400 CICS resources in each of the 30 CICS regions

- Compared to CPSM BAS
  - 100 CPSM Resource groups each contains a PROGRAM, LIBRARY, TRANSACTION and URIMAP definition
  - All 100 Resource groups contained in a single Resource description
  - Resource description has a scope of 30 CICS regions, 10 on each LPAR
  - Installing the Resource description created 400 CICS resources in each of the 30 CICS regions



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- Level 1 bullet
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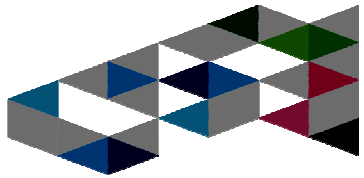
    - Level 3 bullet



Measurement 1: Install and Enable

- Application – Install and Enable Application from CICS Explorer

  Response time = time between install command issued and the time of last DFHRL0132 message - all resources in bundle enabled

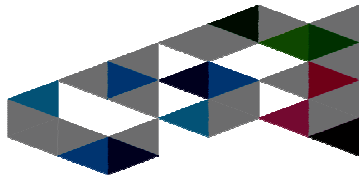
  CPU data extracted from RMF

- CPSM BAS – Install Resource description from CPSM WUI

  Response time = time between install command issued and the time to last EYUBN0099I message - resource creation complete

  CPU data extracted from RMF

	Response time (s)	All CMAS CPU usage (s)	All MAS CPU usage (s)
Application	**5**	**3.504**	**12.570**
CPSM BAS	**41**	**1.518**	**6.732**



Measurement 2: Disable

- Application – Disable Application from CICS Explorer

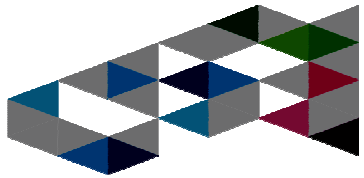
  Response time = time to last DFHRL0132 message - all resources in bundle disabled

  CPU data extracted from RMF

- CPSM BAS – Disable all resources with scope of Resource description from CPSM WUI

  Response time = time to last DFHAP1900 message - resource disabled

CPU data extracted from RMF	Response time (s)	All CMAS CPU usage (s)	All MAS CPU usage (s)
Application	**2**	**1.888**	**6.252**
CPSM BAS	**2**	**0.522**	**3.678**



Measurement 3: Discard

- Application – Discard Application from CICS Explorer

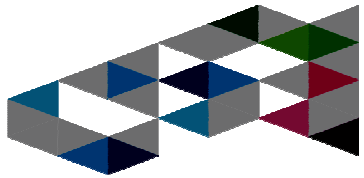
  Response time = time to last DFHRL0130 message - bundle discarded

  CPU data extracted from RMF

- CPSM BAS – Discard all resources with scope of Resource description from CPSM WUI

  Response time = time to last DFHLD0512 message LIBRARY resource discarded

CPU data extracted from RMF	Response time (s)	All CMAS CPU usage (s)	All MAS CPU usage (s)
Application	**<1**	**2.670**	**3.054**
CPSM BAS	**3**	**1.062**	**1.422**



Measurement 4: MAS Warm restart

Time taken in a single CICS region to reinstall all the resources in the Application or Resource description on WARM restart

- Application –

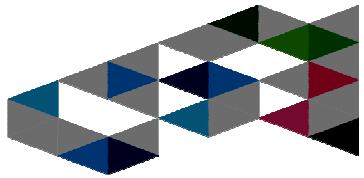
  Response time = time from CICS started to last resource added message produced in MSGUSR log

  CPU data extracted from RMF as difference between with and without Application

- CPSM BAS –
- Response time = time from CICS started to DFHSI1517 message

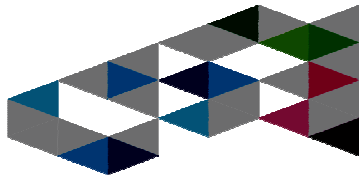
  CPU data extracted from RMF as difference between with and without Resource description

	Response time (s)	All CMAS CPU usage (s)	MAS CPU usage (s)
Application	**2**	**0.834**	**0.060**
CPSM BAS	**3**	**1.290**	**0.050**



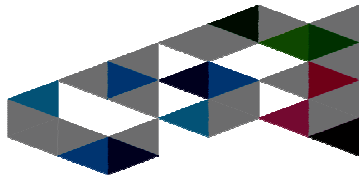
Application Packaging Summary

- Using Application Packaging supports cloud deployment
- Definitions and management performed from CICS Explorer using underlying functionality provided by CICSPlex SM and CICS
- Application packaging provides similar functionality to existing CICSPlex SM Business Application Services but is a framework for continuing cloud enablement.
- Compared to CPSM BAS functions, Application packaging is more costly in overall CPU time but is quicker to make the resources in an Application available for an INITIAL start.
- Compared to CPSM BAS functions, Application packaging both less costly in overall CPU time and quicker to make the resources in an Application available for WARM restart.



Application Context for Resource Usage

- CICS V5.1 allows Application-wide view of resource usage by adding context to Monitor data
  - Application context comprises:-
    - Application name (64 bytes)
    - Platform name (64 bytes)
    - Operation name (64 bytes)
    - Major/minor/micro version number of Application (4 bytes each)
- Application context is added to the monitor data for a CICS task the first time the task runs a program packaged as part of an Application
  - if multiple Application context data is encountered the first occurrence is used
- How to add Application context data to a program?
  - Application, Platform and version data is derived from the Application bundle
  - Operation names are optionally defined as Entry Points in the Application bundle
- Application context reporting provided by CICS PA

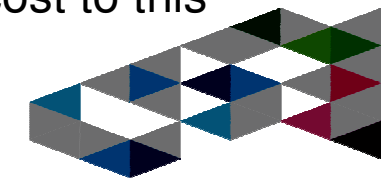


Application Context for Resource Usage

- 2 regions on different LPARs
- Transactions in Region1 DPL to Region2 passing small Container
  - 3 transaction types read/write/delete TS queues on Region2
  - No Application Context resources are installed from CSD definitions
  - Application Context resources are installed as an Application
    - Read/write/delete programs each have an Operation defined

	Region1 CPU per transaction (ms)	Region2 CPU per transaction (ms)	Total CPU per transaction (ms)
No Application Context	**0.078**	**0.510**	**0.588**
With Application Context	**0.083**	**0.498**	**0.581**

- The addition of Application context data shows no significant extra cost to this simple application.



Transaction Isolation (Backup)

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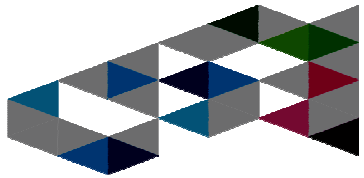
Transaction Isolation

- STGPROT=YES,TRANISO=YES
- Unique Subspaces
  - All TRANs with ISOLATE=YES in User key
- Base Space
  - All TRANs with ISOLATE=YES in CICS key
- Common Space
  - All TRANs with ISOLATE=NO in any key



TRANISO=NO versus TRANISO=YES

ETR	CICS %	Real Storage frames	MS/Tran
2072.30	128.27	163292	0.618
2842.24	173.21	163292	0.609
4130.87	245.55	163335	0.594
5047.97	296.96	163335	0.594
5681.45	333.29	163487	0.586

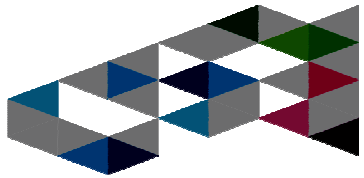
Traniso=NO

Ave CPU/Tran=0.600ms

ETR	CICS %	Real Storage frames	MS/Tran
2073.25	140.49	188103	0.677
2842.38	190.72	188103	0.670
4129.20	272.32	188138	0.659
5044.09	332.28	185032	0.658
5676.44	371.88	185111	0.655

Traniso=YES

Ave CPU/Tran=0.663ms



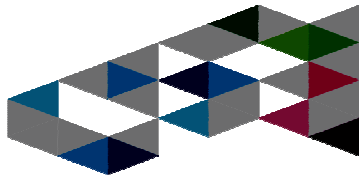
	Traniso (NO)	Traniso(YES)
UDSA	**4K**	**4K**
EUDSA	**64K**	**1M**

Page sizes

	Traniso (NO)	Traniso (YES)
UDSA	**256K**	**1M**
EUDSA	**1M**	**1M**

Extent sizes

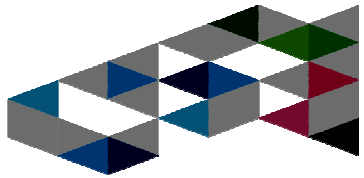
SMI default TASKDATALOCATION has changed in 5.1



CICS Statistics (from the highest ETR)

```
Transaction isolation. . . . . :        INACTIVE
Reentrant programs . . . . . :          PROTECT
Current DSA limit. . . . . :              5120K
Current DSA total. . . . . :              2560K
Peak DSA total . . . . . :                2560K
Current EDSA limit . . . . . :             500M
Current EDSA total . . . . . :              88M
Peak EDSA total. . . . . :                  88M
MEMLIMIT size. . . . . :                20,480M
MEMLIMIT set by. . . . . :                 JCL
```

```
Transaction isolation. . . . . :          ACTIVE
Reentrant programs . . . . . :          PROTECT
Current DSA limit. . . . . :              5120K
Current DSA total. . . . . :              3072K
Peak DSA total . . . . . :                3072K
Current EDSA limit . . . . . :             500M
Current EDSA total . . . . . :             259M
Peak EDSA total. . . . . :                 259M
MEMLIMIT size. . . . . :                20,480M
MEMLIMIT set by. . . . . :                 JCL
```

CPSM Dynamic Routing (Backup)

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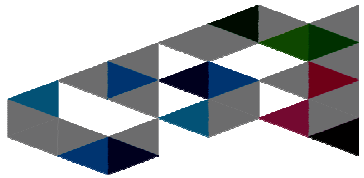
CPSM Dynamic Routing

- 4 standalone regions TOR/AOR COBOL VSAM RLS
  - Run the workload and measure
- Migrate to MRO Transaction routing
  - Front-end the 4 regions with a TOR
  - Use Round robin sample for routing to AORs
  - Run the workload and measure
- Install CPSM
  - Use CPSM Dynamic Routing to distribute the transactions
    - Use CPSM Sysplex Optimised Routing
  - Run the same workload and measure again
- 8 CPs online



TOR ETR	AOR ETR	TOR CPU%	AOR CPU%	TOTAL CPU/TRAN
n/a	2072.61	n/a	178.94	0.863 milliseconds
n/a	2842.46	n/a	230.46	0.810
n/a	4120.62	n/a	324.47	0.787
n/a	5035.52	n/a	387.15	0.768
n/a	5617.90	n/a	427.88	0.761 ave 0.797 ms

TOR ETR	AOR ETR	TOR CPU%	AOR CPU%	TOTAL CPU/TRAN
1982.71	2072.91	21.71	179.85	0.976 milliseconds
2716.34	2841.31	28.32	229.76	0.912
3947.17	4127.12	40.11	320.02	0.876
4782.32	5002.40	49.27	380.17	0.862
5357.32	5602.40	56.98	414.15	0.843 ave 0.893

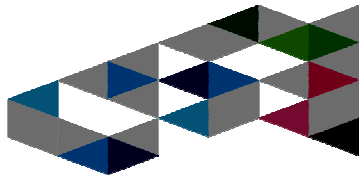
TOR ETR	AOR ETR	TOR CPU%	AOR CPU%	TOTAL CPU/TRAN
1982.55	2071.68	26.31	178.87	0.999 milliseconds
2716.04	2840.08	34.55	229.68	0.935
3946.17	4125.28	48.99	321.11	0.902
4813.04	5033.92	59.46	380.43	0.878
5394.49	5640.63	67.92	418.77	0.867 ave 0.916

Round Robin

DTRPGM=

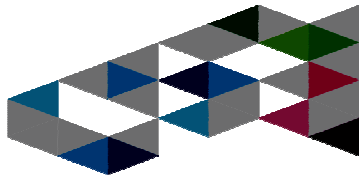
CPSM

Dynamic



Summary

- The terminal processing costs in the standalone regions are replaced with the MRO facility costs.
  - This is similar in this benchmark so AOR CPU% does not change much
- Using the simple Round Robin routing
  - Most of the CPU costs absorbed in the TOR
  - Total CPU/Tran goes from 0.797 ms to 0.893 (+ 86 microsecs)
- CPSM Sysplex Optimised Routing
  - Cost in AOR is similar as workload is stable and not crossing defined thresholds and hence not writing to Coupling Facility often.
  - Slight increase in CPU in the TOR
  - Total CPU per tran goes from 0.893 ms to 0.916 (+ 23 microsecs)
  - See the CICS TS V4.1 report for more on CPSM Dynamic Routing.
- 8 CPs online



EP Adapter Sets (Backup)

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Event Processing Adapter Sets

- EP Adapter Sets

- prior to CICS TS V5.1:

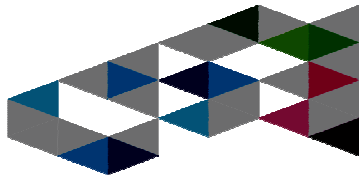
  – events specified in an Event Binding could only be emitted by one EP adapter

  – EP adapter definition could be:

  – embedded in Event Binding or

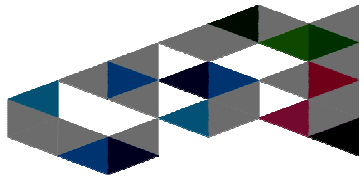
  – defined as a separate EP adapter resource and referenced in the Event Binding

  – emitting events to multiple EP adapters required multiple identical Event Bindings



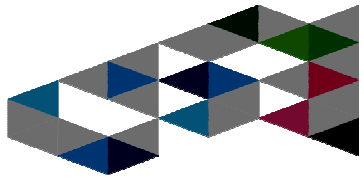
Event Processing Adapter Sets

- EP Adapter Sets
- new to CICS TS V5.1:
  - events specified in an event binding can be emitted by multiple EP adapters
  - events specified in an event binding reference an EP adapter set
  - EP adapter set contains a list of EP adapter resources
  - each EP adapter emits the event



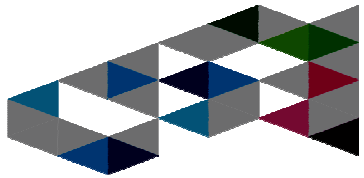
Event Processing Adapter Sets sample XML (1 of 2)

```
<?xml version="1.0" encoding="UTF-8" standalone="yes"?>

<ns2:EPAdapterSet CICSEPSchemaVersion="3"
   CICSEPSchemaRelease="0"
   xsi:schemaLocation="http://www.ibm.com/xmlns/prod/cics/eventprocessing/eventbinding CicsEPAdapterSet.xsd "
   xmlns:ns2="http://www.ibm.com/xmlns/prod/cics/eventprocessing/eventbinding" xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">

<description>wmq_adapterset</description>

<eventAdapterName>wmq_adapter1</eventAdapterName>

<eventAdapterName>wmq_adapter2</eventAdapterName>

<eventAdapterName>wmq_adapter3</eventAdapterName>

</ns2:EPAdapterSet>
```

Event Processing Adapter Sets sample XML (2 of 2)

```
<?xml version="1.0" encoding="UTF-8" standalone="yes"?>
<ns2:eventBinding …….>
<eventSpecification>…….</eventSpecification>
<eventCaptureSpecification>
<name>capture</name>
<eventIdentifier>event</eventIdentifier>
<description></description>
<filter>
<contextFilter>…….</contextFilter>
<locationFilter filterType="CICS_API">…….</locationFilter>
<dataFilter/>
</filter>
<dataCapture/>
</eventCaptureSpecification>
<eventAdapterSetName>wmq_adapterset</eventAdapterSetName>
</ns2:eventBinding>
```

Event Processing user task trace extract (1 of 2)

Multiple event bindings each with a single adapter:

ECEC ENTRY EVENT_CAPTURE

Repeated for each event to be emitted:

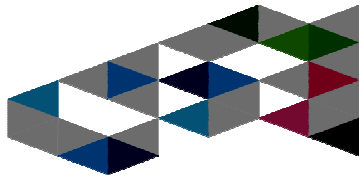
EPEV ENTRY PUT_EVENT

EPEV DATA EPADAPTER

EPEV EVENT MVS_POST_EPSY_ECB

EPEV EXIT PUT_EVENT/OK

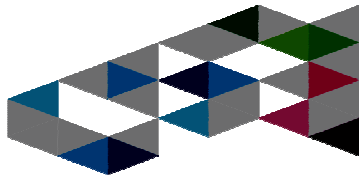
ECEC EXIT EVENT_CAPTURE/OK



Event Processing user task trace extract (2 of 2)

Single event binding using an adapter set:

```
ECEC  ENTRY EVENT_CAPTURE
  EPEV  ENTRY PUT_EVENT
    EPEV  DATA
EPADAPTERSET_NAME(wmq_adapterset)
    Repeated for each adapter in adapterset:
       EPEV  DATA  EPADAPTER
       EPEV  EVENT MVS_POST_EPSY_ECB
  EPEV  EXIT  PUT_EVENT/OK
ECEC  EXIT  EVENT_CAPTURE/OK
```

Event Processing Adapter Set regression testing

- EP processing without adapter sets installed

•there is no regression in CPU/tran or response times

–comparing CICS TS V4.2 with CICS TS V5.1

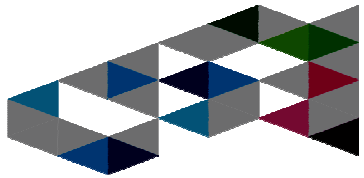
- EP processing with adapter sets installed

•CICS TS V5.1 performance test comparing:

–EP adapter set containing one adapter with

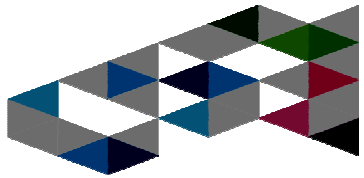
–EP adapter **not** contained within an EP adapter set

–CPU/tran and response times identical

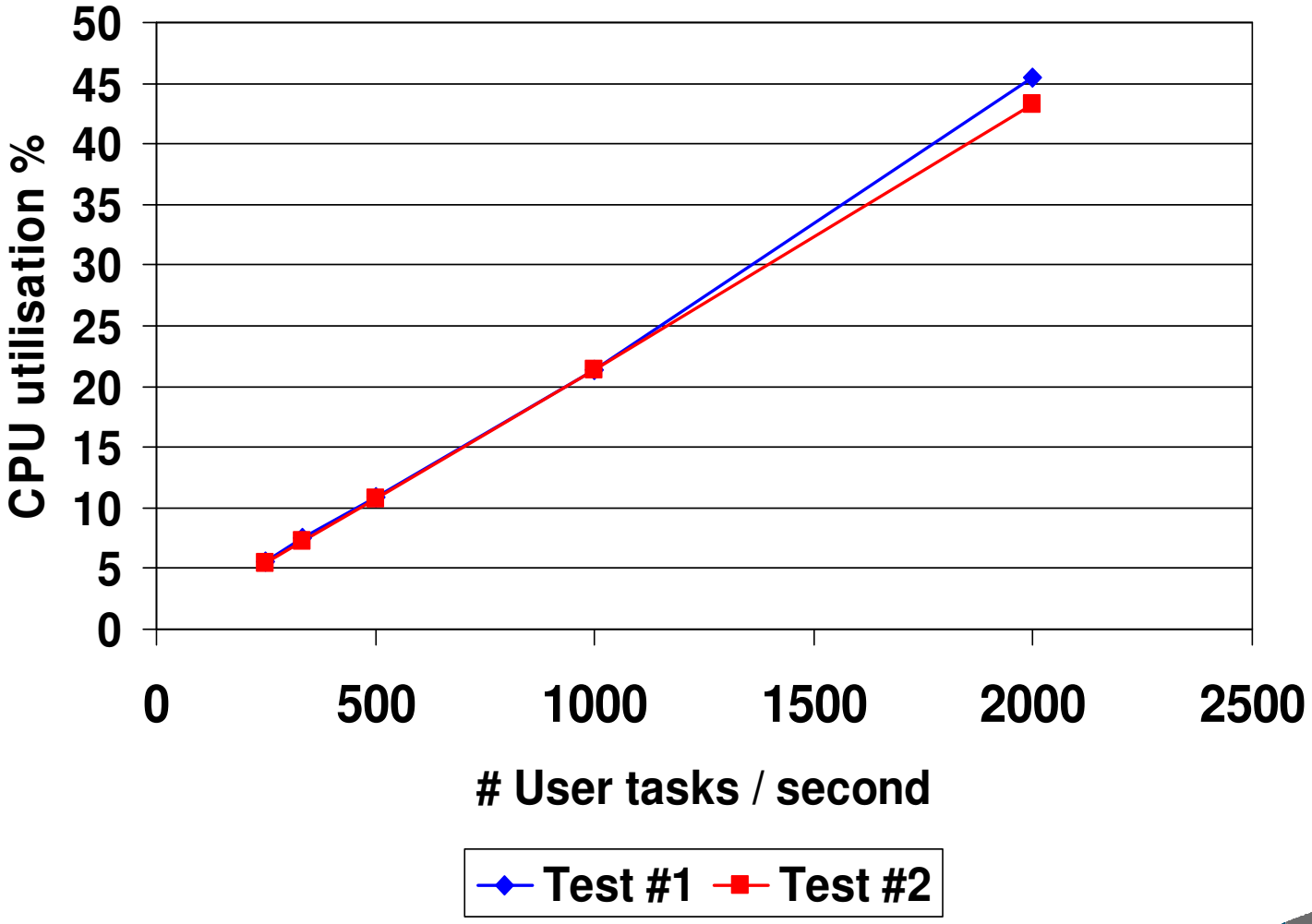


Event Processing Adapter Set performance comparison

- Comparing:
  - Test #1: One Event Binding referencing:
    - Adapter Set containing 3 WMQ adapters
    - Single event captured
  - Test #2: 3 Event Bindings each referencing:
    - a single WMQ adapter
    - 3 events captured

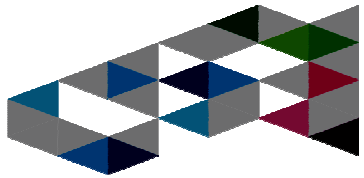


EP Adapter Set performance benefits - CPU usage



Summary

- no performance regression with CICS TS V5.1
- multiple emissions per captured event
  - with adapter sets vs without adapter sets
  - similar performance characteristics



CICS Performance Analyzer (Backup)

Impact2014

Be First.

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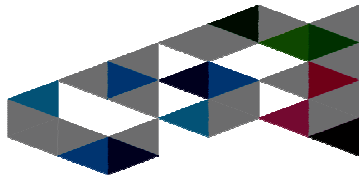
New in CICS PA 5.2

- Performance Alerts in HDB
- Visualization and analysis in the PA plug-in
- Exclude Resource option for Statistics Alerts
- Find command when viewing Statistics data online
- LISTX report TRANFLAG abnormal termination bit
- CICS PA Plug-in v5.2
- Further performance improvements when processing large volumes of SMF data
- Currently at 12%-18%
- Summary reports for Platforms and Applications
- CTG - Activity Summary Report - re-formatting



Performance Alerts in HDB

- **New HDB capability enables**
- **Performance alerts**
- **Related list records**

to be loaded to HDB and exported to DB2

- **New explorer HDB templates**

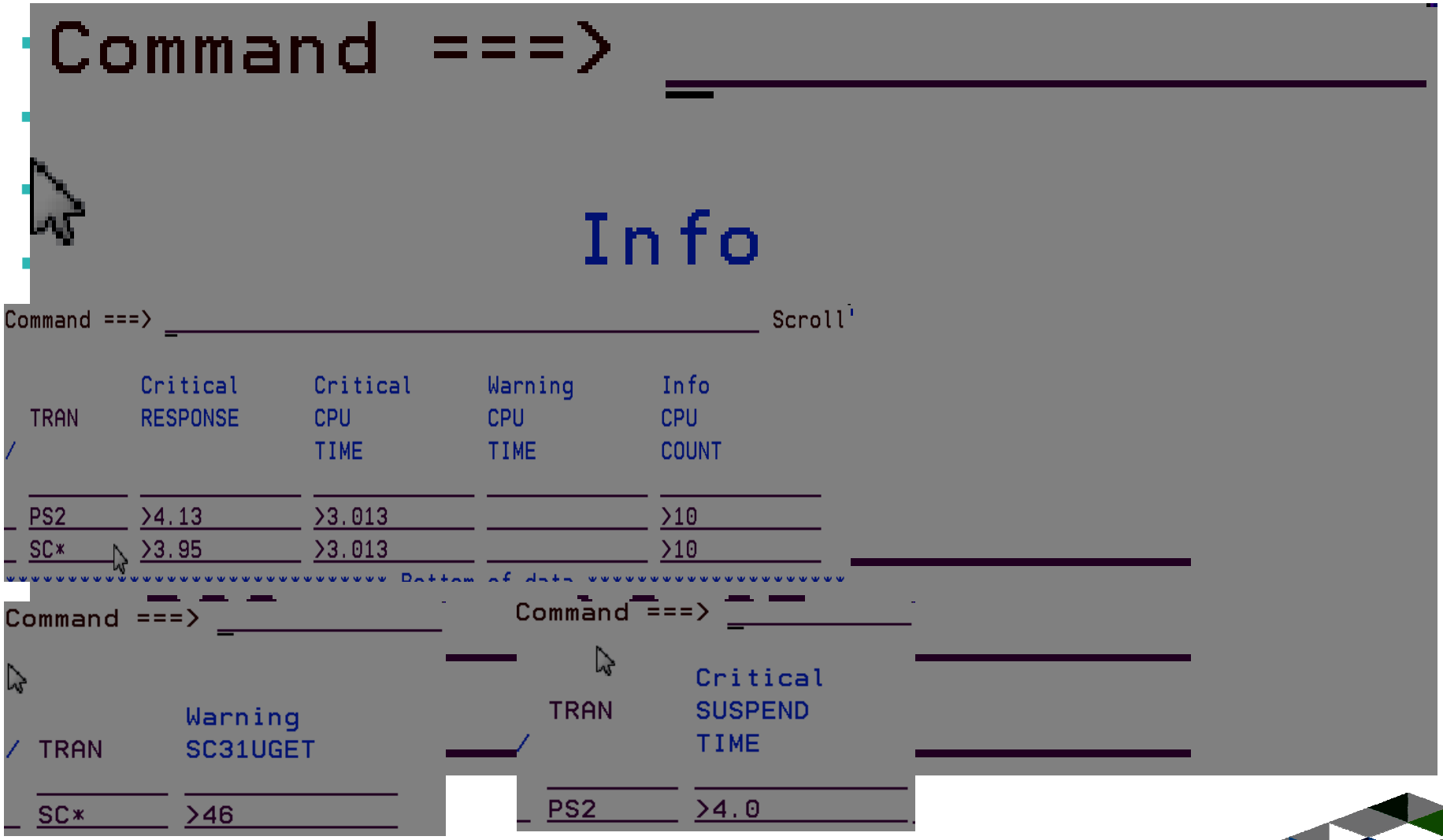
```
  File  Options  Help
                                  _HDB Templates                  Row 1 to 11 of 11
Command ===> _____________________________________________________ Scroll ===> CSR

Select to edit Template. Enter NEW command to define a new Template.

/  Name      Type                Description                    Changed          ID
_ APPLNM51 SUMMARY  Explorer HDB for App Cntx V5.1   2014/07/01 12:00 CICSPA
_ APPLNM52 SUMMARY  Explorer HDB for App Cntx V5.2   2014/07/01 12:00 CICSPA
_ EXPLOR31 SUMMARY  Explorer HDB for CICS TS V3.1    2014/07/01 12:00 CICSPA
_ EXPLOR32 SUMMARY  Explorer HDB for CICS TS V3.2    2014/07/01 12:00 CICSPA
_ EXPLOR41 SUMMARY  Explorer HDB for CICS TS V4.1    2014/07/01 12:00 CICSPA
_ EXPLOR42 SUMMARY  Explorer HDB for CICS TS V4.2    2014/07/01 12:00 CICSPA
_ EXPLOR51 SUMMARY  Explorer HDB for CICS TS V5.1    2014/07/01 12:00 CICSPA
_ EXPLOR52 SUMMARY  Explorer HDB for CICS TS V5.2    2014/07/01 12:00 CICSPA
_ EXPLST42 LIST     Explorer HDB for CICS TS V4.2    2014/07/01 12:00 CICSPA
_ EXPLST51 LIST     Explorer HDB for CICS TS V5.1    2014/07/01 12:00 CICSPA
_ EXPLST52 LIST     Explorer HDB for CICS TS V5.2    2014/07/01 12:00 CICSPA
********************************* Bottom of data ********************************
```


Performance Alerts in HDB

- Performance alert data available in the PA plug-in in addition to Statistics alerts



Performance Alerts in HDB