Session B01

zMainframe Concepts (The Big Picture) - Part 1

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RETURN TO INDEX

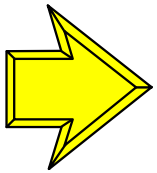
Session Objectives

In this session we will Discuss

The IBM System z9 and zSeries Mainframe Concepts and Server Overview

- What is a Mainframe
- The Mainframe difference
  - engine and channel subsystem usage
- Current zSeries models and comparisons
- High level Server design and operation
  - Operating System to Channel Subsystem relationship

IBM System z9 and zSeries Mainframe Concepts and Overview



System z9 and zSeries Mainframe Concepts and Overview

What is a Mainframe?

How would you describe a mainframe to some one in one or two sentences?

- To someone new to IT (just out of school) ?
- To an 'old timer' ?
  - Would it make a difference?

- A very large and expensive computer capable of supporting hundreds, or even thousands, of users simultaneously
  - http://www.webopedia.com

Costs (Expensive) is relative

Mainframes are often thought of as expensive, however this is only relative to how much work is done (How much - Today's mainframe 'lots')

- Hardware costs have gone down dramatically
- Today its the S/W costs that are most often cited as the most expensive component
- Many S/W costs are associated with the capacity of the server
  - The capacity of the server is almost always rated on the number of 'CP' engines used
- Today's zSeries servers use their resources very efficiently, exploiting other engine types to process workload and manage input / output operations

IBM Mainframe concept (Big Picture)

Considered a General Purpose Business Computer

The Operating System
(Multiple OSs are possible)

Runs various application programs

Exploits various engine types and usage

The Channel Subsystem
(associated with all I/O adapters)
Works closely with the OS manages I/O operations

Has its own dedicated engine (SAP) and operates independently of the OS engines

Mainframe Differences

- Reliability Availability Serviceability (RAS)
- Reliability Availability Scalability (RAS)
  - Vertically
  - Horizontally
  - on demand
- Security
- Engine Versatility
- Engine Usage
- Resource sharing
  - Resource reallocation
  - Autonomic
- Virtualization
- I/O Bandwidth
  - Extremely large number of available channels
  - Massive amounts of data that can be moved

zSeries Engines (Processor Units)

Mainframes typically have more engines physically available then are used in most configurations

Mainframe engines (or PUs) are very versatile and can be assigned (characterized) as the following:

- A Central Processor (CP)
  - CPs are typically associated with S/W license charges
- A System Assist Processor (SAP)
  - Used exclusively by the channel subsystem
- An Internal Coupling Facility (ICF)
  - Used to run Coupling Facility Control Code (Parallel Sysplex)
- An Integrated Facility for Linux (IFL)
  - Used to run the Linux OS (Open source code)
- A zSeries Application Assist Processor (zAAP) **System z9 and zSeries 990/890 only**
  - Runs Java code (z/OS CPs can offload Java workload to a zAAP)

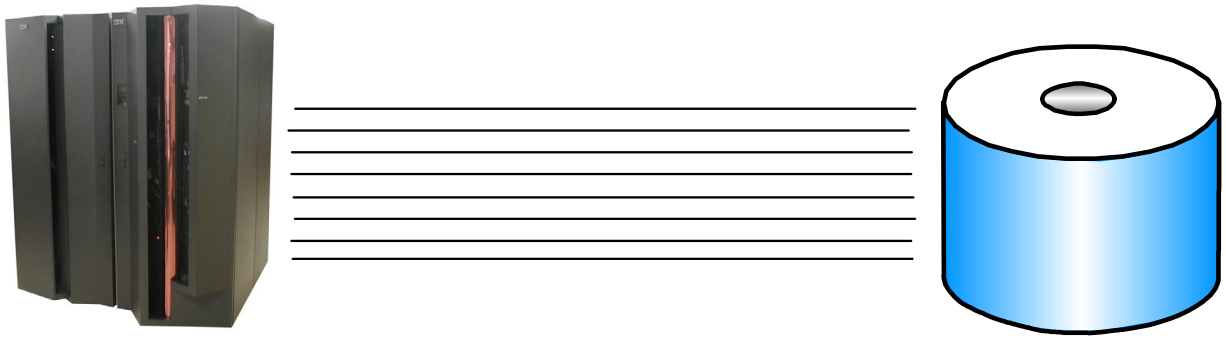
The IBM General Purpose Business Computer (The Mainframe)

A key difference between Mainframes and other servers is the amount of data that can be imported/exported to external shared storage devices while the operating system(s) maintain high performance levels processing other workloads

The OS and the CSS work together to efficiently manage data

I/O Bandwidth is the maximum amount of I/O (data measured in Giga Bytes per second) data that a Server can potentially achieve

9672- 8 GB/sec z900- 24 GB/sec z990- 96 GB/sec z9- 172.8 GB/sec



Mainframe's architecture is designed for efficient data movement
Has multipath capability (up to 8 to an LCU) with up to 256 channels per OS

Common Terms

CMOS - Complimentary Metal Oxide Semiconductor

SE - Support Element

HMC - Hardware Management Console

PU = Processing units

PUs can be assigned as CPs, SAPs, ICFs, IFLs

z900 model 104

Four Engines, 4-Way

Four CPs - Central Processors

IBM @Servers zSeries

zSeries 990 /890 / 900 / 800

or z990 /z890 / z900 / z800

S/390 Parallel Enterprise Server

CPC - Central Processing Complex

CEC - Central Electronic Complex

CPU - Central Processing Unit

Mainframe or Host

Mainframe S/W operating systems

MVS, OS/390, z/OS or → MVS

CHPID - Channel Path ID

PR/SM - Processor Resource Systems Manager

LPAR - Logical Partitioning

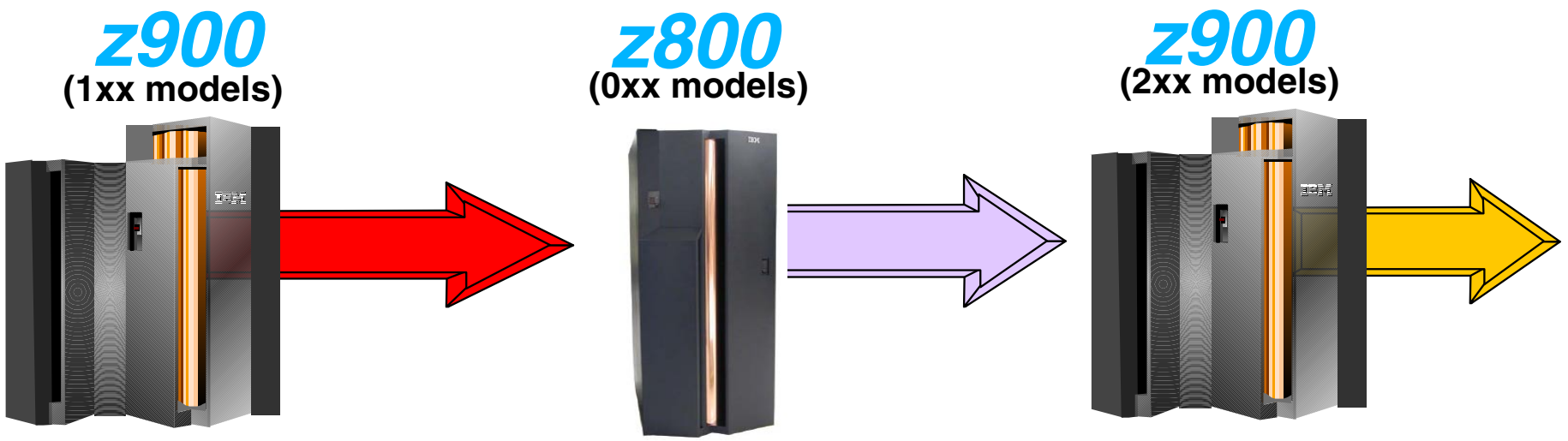
(belongs to PR/SM)

EMIF - ESCON Multiple Image Facility

MIF - Multiple Image Facility

(FICON, OSA and CF Links)

zSeries Hardware Technology (1 of 2)



z900 M/T 2064
(October 2000)

- General Purpose
  (101 - 116)
- Capacity models
  (1C1 - 1C9)
- Coupling Facility
  model 100
  (March 2001)

z800 M/T 2066
(February 2002)

- General Purpose
  (0E1 - 004)
- Coupling Facility
  model 0CF
- Dedicated Linux
  model OLF

z900 M/T 2064
(April 2002)

High-performance models
- General Purpose
  (2C1 - 2C9, 210 - 216)

zSeries Hardware Technology (2 of 2)

z990 M/T 2084
(May 2003)

- General Purpose H/W model
  - A08 (one book - up to 8 CPs)
  - B16 (two books - up to 16 CPs)
  - C24 (three books - up to 24 CPs)
  - D32 (four books - up to 32 CPs)

z890 M/T 2086
(April 2004)

- One General Purpose H/W model
  - A04 (one book - up to 4 CPs)

    Many capacity settings

System z9 109 Hardware Technology

z9 109

The z9 109 introduces a new family of servers
- The System z9 family

z9 109 M/T 2094

(July 2005)

- General Purpose H/W models
  - S08 (one book - up to 8 CPs)
  - S18 (two books - up to 18 CPs)
  - S28 (three book - up to 28 CPs)
  - S38 (four books - up to 38 CPs)
  - S54 (four books - up to 54 CPs) planned availability November 2005

IBM @Server zSeries 800 and 900

IBM @Servers zSeries with new z/Architecture

- z/Architecture
  - Based on 64-bit Real and Virtual Storage Addressing
  - Supports trimodal addressing (64-bit,31-bit and 24-bit)
    - ESA/390 supported bimodal addressing (31-bit and 24-bit)
  - Eliminates need of expanded storage
  - Increased register size to support 64-bit instruction/ data addresses
- Intelligent Resource Director
  - LPAR CPU Management
  - Dynamic Channel Path Management
  - Channel Subsystem Priority Queuing
- HiperSockets

- Faster Processor Unit (PU)
  - Up to 20 PUs (z900)
  - Up to 5 PUs (z800)

- z900 Memory
  - Up to 64 GB
- z800 Memory
  - Up to 32 GB

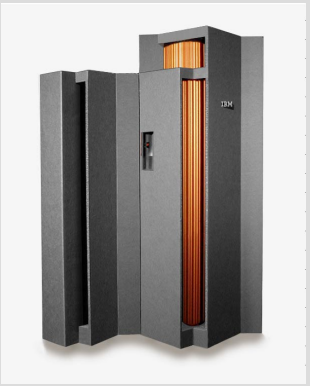
- Channel CHPID Assignment
- Dense Channel Packaging
- New Cabling connectors
- Increased Channel options
  - FICON (z900-96, z800-32)
  - OSA-E (24)
  - PCI-CC (16)
  - PCI-CA (12)
- Increased Total I/O Bandwidth
  - z900 24 GB/sec
  - z800 6 GB/sec
- Increased Parallel Sysplex Connectivity Options
  - Peer mode
  - Compatibility mode
- z900 Upgradable from G5/G6

zSeries Family of Servers

z900

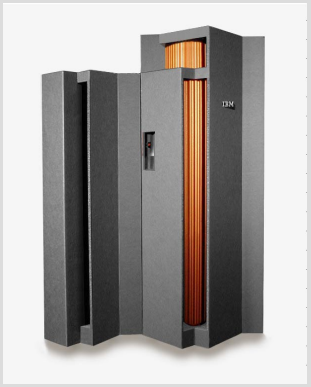
109
108
107
106
105
104
103
102
101

100



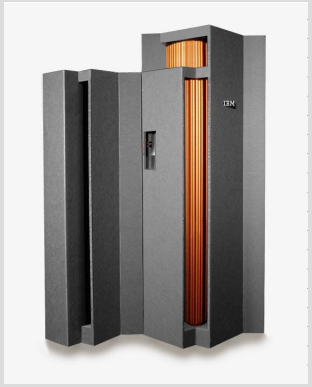
- CMOS 8S with Copper interconnect
- MCUs (Modular Cooling Unit)
- 12 PUs
- Up to nine CPs
- 5 - 32 GB Memory
- 2 Memory cards
- 1.3 ns Cycle time
- CF = Model 100

116
115
114
113
112
111
110
1C9
1C8
1C7
1C6
1C5
1C4
1C3
1C2
1C1



- CMOS 8S with Copper interconnect
- MCUs (Modular Cooling Unit)
- 20 PUs
- Up to 16 CPs
- 10 - 64 GB Memory
- Four Memory cards
- 1.3 ns Cycle time

216
215
214
213
212
211
210
2C9
2C8
2C7
2C6
2C5
2C4
2C3
2C2
2C1



- CMOS 8SE with Copper interconnect
- MCUs (Modular Cooling Unit)
- 20 PUs
- Up to 16 CPs
- 10 - 64 GB Memory
- 4 Memory cards
- 1.09 ns Cycle time

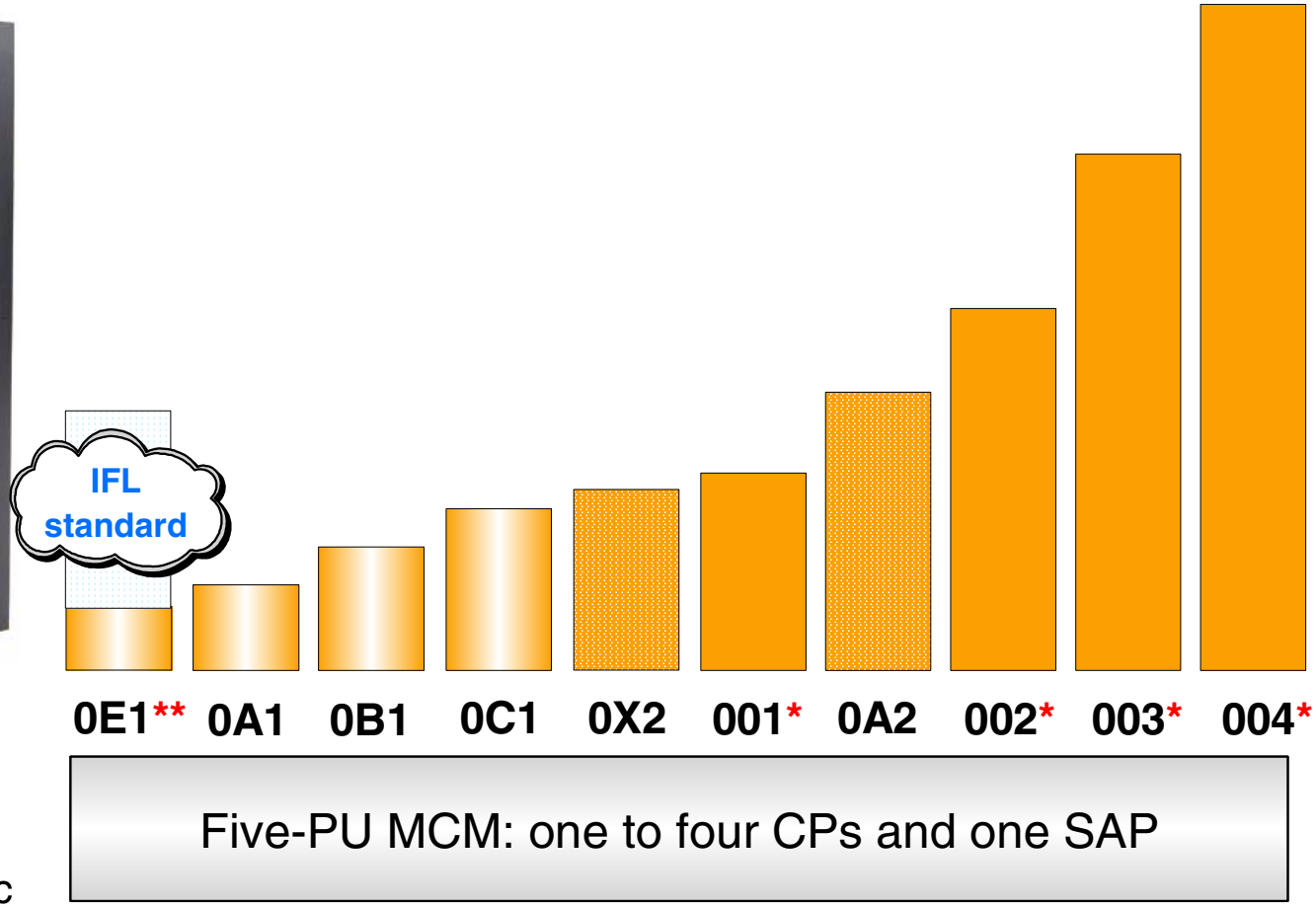
z800

004
003
002
001
0X2
0C1
0B1
0A1
0E1

OCF
OLF

- CMOS 8S with Copper interconnect
- 5PUs
- Up to four CPs
- 8 - 32 GB Memory
- Four Banks of Memory chips
- 1.6 ns Cycle time
- CF = Model OCF
- LINUX model OLF

z800 General Purpose Models Relative Performance

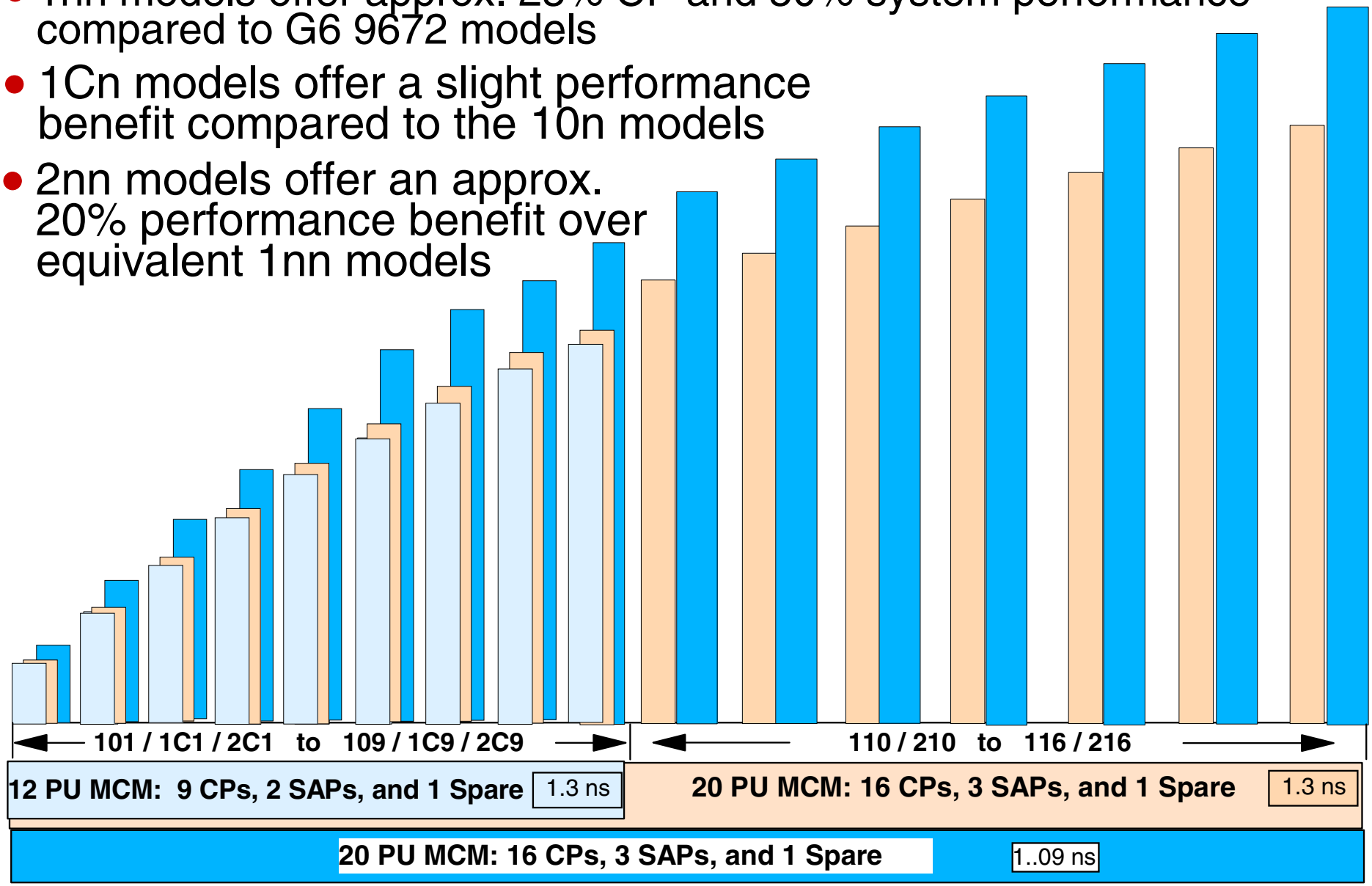


* 001 - 004 is approximately same performance as G6 X17-X47

** 0E1 has one IFL as standard

z900 Models 101 - 216 Relative Performance

- 1nn models offer approx. 25% CP and 50% system performance compared to G6 9672 models
- 1Cn models offer a slight performance benefit compared to the 10n models
- 2nn models offer an approx. 20% performance benefit over equivalent 1nn models



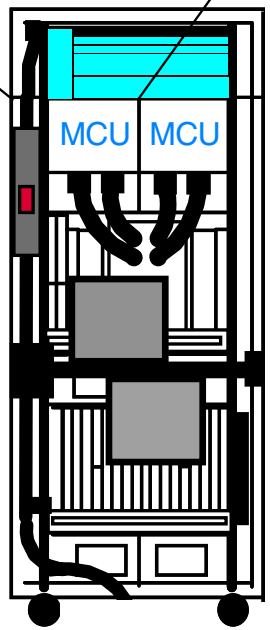
Graph is for illustration purposes only

zSeries 900 CPC Design

Modular Cooling Unit (MCU)

- Modular Refrigeration Unit (MRU)
- Motor Scroll Assembly (MSA)
- Motor Drive Assembly (MDA)

N +1 design



CEC Cage

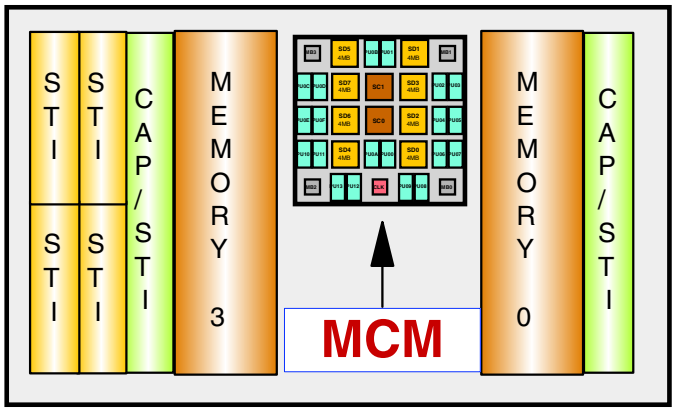
Two S/Es

I/O Cage

z900 A Frame

May have an additional Z and/or B frame

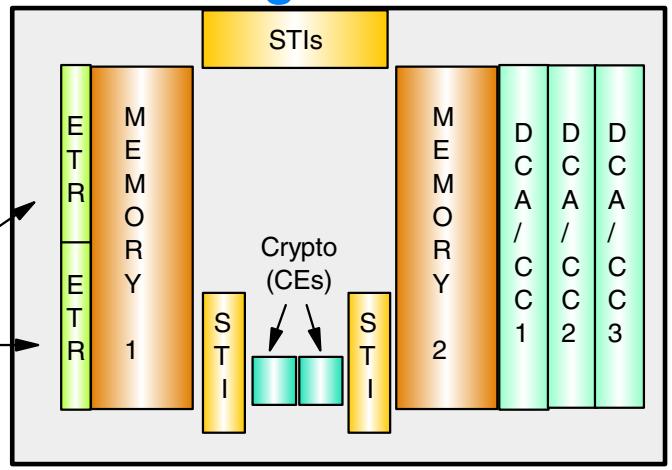
CEC Cage - Front View



zSeries 900 CPC MCM will contain
- 12 PUs
- 20 PUs

depending on z900 model

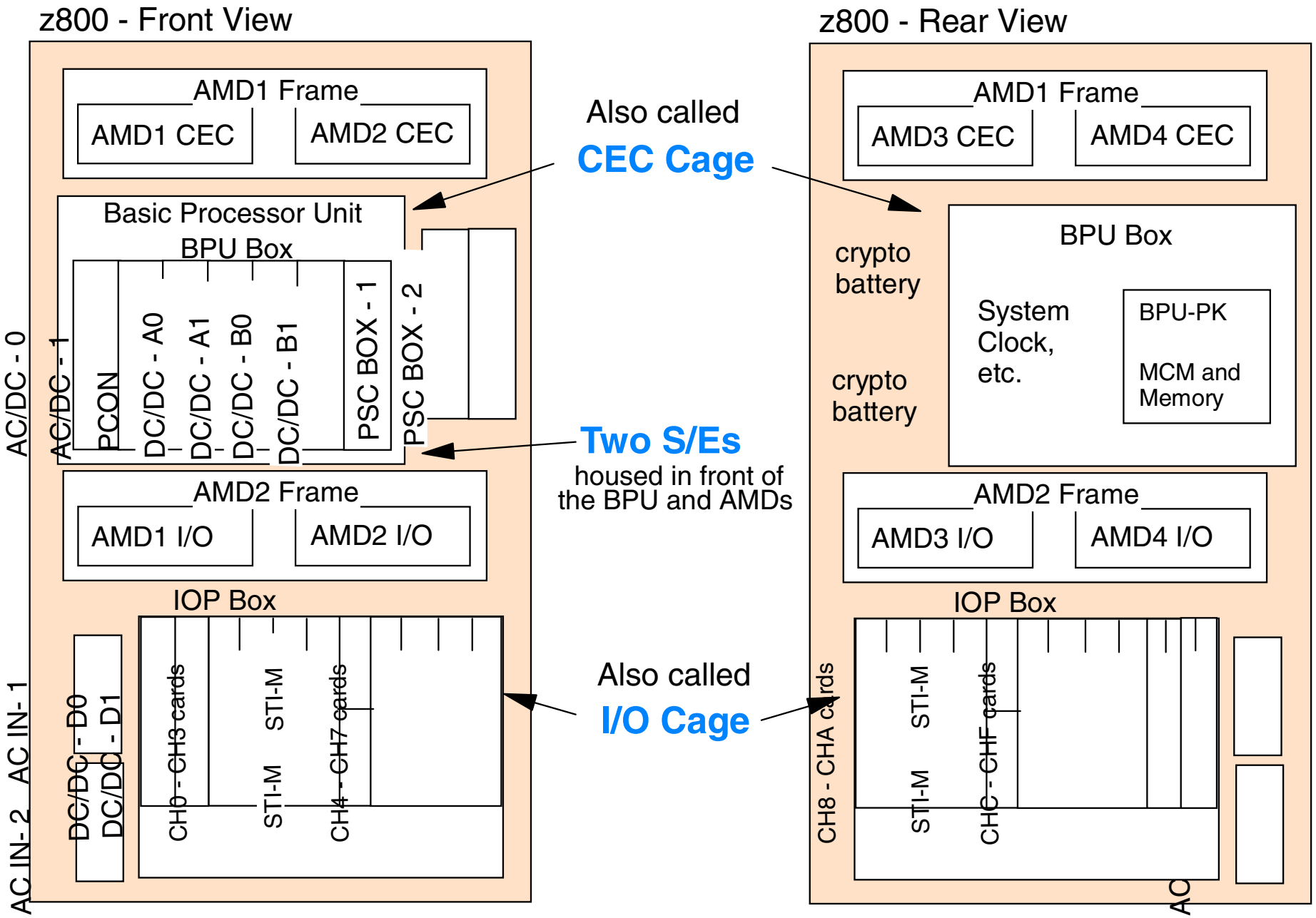
CEC Cage - Rear View



Two ETR cards N+1

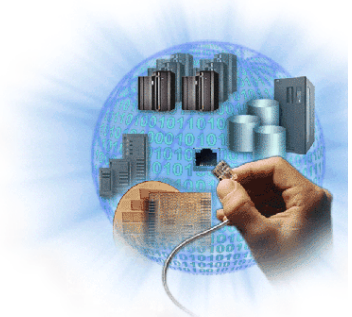
The z800 CEC cage holds the Base Processor Unit (BPU) which contain equivalent functionality as the z900
- MCM contains 5 PUs
- Has memory DIMMS

zSeries 800 CPC Design



IBM System z9 and zSeries 990 / 890 Servers

System z9 109 and zSeries 990/890
Designed for on demand business computing



- Integrated - Open - Virtualized - Autonomic

z890

zSeries Family
sub-uni to 4 CP

z990

zSeries family
1 to 32 CPs

z9 109

System z9 family
1 to 54 CPs
Supporting large business with additional addressing, bandwidth and thru-put requirements

System z9 and zSeries 990 / 890 Terminology

Some new Terminology used with z9 and zSeries z990/z890 Servers

- Book
  - A book contains an MCM (processors), memory and STI connections for the MBAs
  - A z9 and z990 can have multiple books
  - A z890 has one book
- eServer zSeries Application Assist Processor (zAAP)
  - A PU used by the JAVA virtual machine to run JAVA code
- I/O Subsystem
  - These Servers have one I/O Subsystem which utilizes one IOCDS and a single HSA
- Logical Channel Subsystem (LCSS)
  - z9 / z990 / z890 can have multiple LCSSs
- Physical Channel ID (PCHID) System z9 and zSeries 990/890
  - Physical location that can be mapped to a channel path ID (CHPID)
    - PCHID unique to server (CHPID is unique to a LCSS)

IBM @server zSeries 990 Models

- z990 model A08
  - One book with 12 PUs, maximum of 8 PUs can be assigned as CPs
- z990 model B16
  - Two books with 24 PUs, maximum of 16 PUs can be assigned as CPs
- z990 model C24
  - Three books with 36 PUs, maximum of 24 PUs can be assigned as CPs
- z990 model D32
  - Four books with 48 PUs, maximum of 32 PUs can be assigned as CPs

- CMOS 9S-SOI with copper interconnect
- 12 Processor Units (PUs) per MCM, up to 8 as CPs
- 8 - 256 GB Memory
- .8 ns cycle time
- Modular Refrigeration Units (MRU)

z990 models C24 and D32 available at GA2

Note that the system model number no longer reflects the number of CPs

zSeries 990 Software Models

Each z990 model has an additional software model number association. The software model can be used for licensing and MSU purposes. z990 *MSUs range from 70 (301) to 1365 (332)

z990 A08		z990 B16		z990 C24		z990 D32	
S/W model	CPs	S/W model	CPs	S/W model	CPs	S/W model	CPs
301	1	309	9	317	17	325	25
302	2	310	10	318	18	326	26
303	3	311	11	319	19	327	27
304	4	312	12	320	20	328	28
305	5	313	13	321	21	329	29
306	6	314	14	322	22	330	30
307	7	315	15	323	23	331	31
308	8	316	16	324	24	332	32

This chart represents the maximum S/W model that can be assigned to a given H/W model.
Different H/W and S/W model combinations are possible depending on factors such as storage and other PU assignments.

***See www-1.ibm.com/servers/eserver/zseries/library/swpriceinfo/hardware.html for current MSU ratings**

Relative Performance of z990 Models

Relative performance scale of new z990 Processors

Number of z990 CPs	Base	Ratio
1 CP	z900-2C1	1.54 - 1.61
8 CPs	z900-2C8	1.52 - 1.56
16 CPs	z900-216	1.51 - 1.55
32 CPS	z900-216	2.46 - 2.98

IBM @server zSeries 890 model A04

- z890 model A04
  - One book with 5 PUs, maximum of 4 PUs can be assigned as CPs
  - Various capacity settings available across ordered CP(s)
  - One standard SAP
  - Eight STIs for I/O connectivity
  - Up to 32 GB of storage

z890

M/T 2086

- CMOS 9S-SOI with copper interconnect
- Five Processor Units (PUs) per MCM, up to 4 as CPs
- 8 - 32 GB Memory
- 1.0 ns cycle time
- Air cooled

Note that the system model number no longer reflects the number of CPs

zSeries 890 Capacity Settings and MSUs

A z890 model A04 has additional capacity settings available. Capacity settings can be used for licensing and MSU purposes.

z890 Capacity Settings and MSU ratings

1-WAY	MSUs	2-WAY	MSUs	3-WAY	MSUs	4-WAY	MSUs
110	4	210	8	310	11	410	15
120	7	220	13	320	20	420	26
130	13	230	26	330	38	430	49
140	17	240	32	340	47	440	62
150	26	250	50	350	74	450	97
160	32	260	62	360	91	460	119
170 - Full 1-way	56	270 - Full 2-way	107	370 - Full 3-way	158	470 - Full 4-way	208

*Capacity settings are reported by certain software instructions as a machine model number

A capacity setting of 070 indicates a z890 with no CPs assigned, This could be a z890 with only IFLs or ICFs or some combination of IFLs and ICFs

See www-1.ibm.com/servers/eserver/zseries/library/swpriceinfo/hardware.html for current MSU ratings

IBM @server zSeries 990/z890 Features

z990 1 to 48 PU engines (32 CPs)
z890 1 to 5 PU engines (4 CPs)
- SuperScalar design

Greater functionality
Up to 30
Logical Partitions

Spare Engines

zSeries Application Assist Processor (zAAP)

Internal Battery Feature

Security: Increased SSL throughput
- CP Crypto Assist Function (CPACF) Cryptographic-assist instructions
- PCI Crypto Accelerators (PCICA)
- PCIX Crypto Coprocessors (PCIXCC)
- PCI Crypto Express2

Processor Storage
z990 Up to 256 GB
z890 Up to 64 GB

- Up to 48 (z890 40) OSA-E ports (OSA Express2)
- Up to 120/240 (z890 40/80) FICON Express and Express2 channels
- Up to 16 HiperSockets

Multiple Logical Channel Subsystems, 256 Channels per LCSS

Up to 48 (z890 8) 2GB/sec STIs

Coupling Links:
- Internal Coupling Channels (IC)
- InterSystem Channels (ISC)
- Integrated Cluster Bus (ICB)

Spanned Channels
- Channels that may access more than one LCSS

On/Off Capacity on Demand

IBM System z9 109 models

- z9 109 model S08
  - One book with 12 PUs, maximum of 8 PUs can be assigned as CPs
    - A book contains memory and STI connections
- z9 109 model S18
  - Two books with 24 PUs, maximum of 18 PUs can be assigned as CPs
- z9 109 model S28
  - Three books with 36 PUs, maximum of 28 PUs can be assigned as CPs
- z9 109 model S38
  - Four books with 48 PUs, maximum of 38 PUs can be assigned as CPs
- z9 109 model S54
  - Four books with 64 PUs, maximum of 54 PUs can be assigned as CPs

M/T 2094

- CMOS 10S-SOI with copper interconnect
- Up to twelve or sixteen Processor Units (PUs) per MCM.
- 16 - 512 GB Memory
- .6 ns cycle time
- Modular Refrigeration Units (MRU)

Note - system model number does not reflect the number of ordered CPs

zSeries 9 109 Capacity and MSUs

Each z9 109 model has an additional software capacity number association. The capacity number can be used for licensing and MSU purposes. z9 109 *MSUs range from 81 (701) to 2409 (754)

z9 S08		z9 S18		z9 S28		z9 S38		z9 S54	
capacity number	CPs	capacity number	CPs	capacity number	CPs	capacity number	CPs	capacity number	CPs
701	1	709	9	719	19	729	29	739	39
702	2	710	10	720	20	730	30	740	40
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
707	7	717	17	727	27	737	37	753	53
708	8	718	18	728	28	738	38	754	54

This chart represents the maximum capacity number that can be assigned to a given H/W model. Different H/W and capacity combinations are possible depending on factors such as storage and other PU assignments.

***See www-1.ibm.com/servers/eserver/zseries/library/swpriceinfo/hardware.html for current MSU ratings**

Relative Performance of z9 109 Models

Relative performance scale of z9 109 Servers

Number of z9109 CPs	Base	Ratio
1 CP	z990-301	1.35
8 CPs	z990-308	1.34
18 CPs	z990-318	1.34
28 CPs	z990-328	1.32
38 CPs	z990-332	1.51
54 CPs	z990-332	1.95

Note: For MSU values, refer to: www-1.ibm.com/servers/eserver/zseries/library/swpriceinfo/
For ITRs refer to: www-1.ibm.com/servers/eserver/zseries/lspr/zSerieszOS.html

* CI = Capacity Indicator and refers to number of installed CPs. Reported by STSI instruction. Model 700 does not have any CPs.

IBM z9 109 New Functions and Features

z9 109 is the next step in the evolution of the mainframe family

z9 109 offers many of the same zSeries features and functions introduced by the zSeries 990 and much more

- New faster Uni Processors
- Up to 60 LPARs
- CBU for IFL, ICF and zAAP
- Spare Engines
- Enhanced CPACF with AES, PRNG and SHA-256
- Configurable Crypto Express2
- Separate PU pool management
- Redundant I/O interconnect
- Hot Pluggable /maintainable MBA/STI fanout cards
- Enhanced Driver maintenance
- Enhanced Book availability
- MIDAW facility
- FCP N-port virtualization
- OSA-Express2 1000BASE-T
- OSA-Express2 (OSA for NCP)
- Dynamic oscillator switchover
- 54 additional hardware instructions

Five H/W models

- 1 to 54 assignable PUs

Up to 512 GB Processor Memory

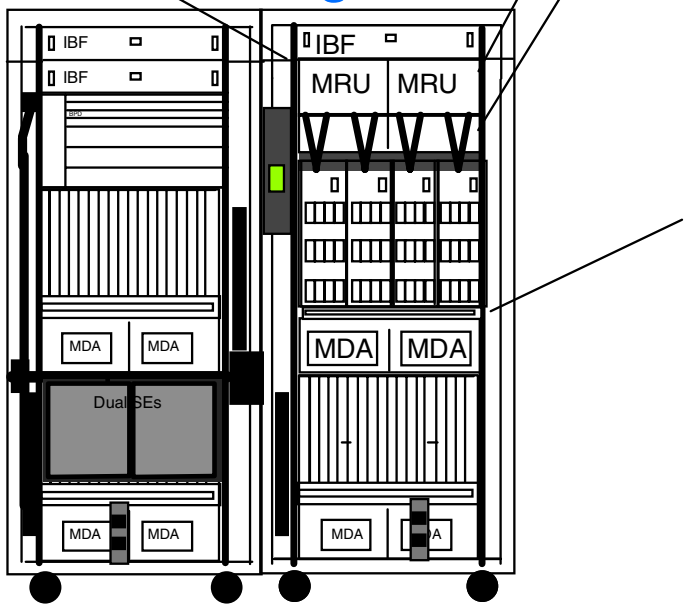
- Up to 4 Multiple Logical Channel Subsystems with Multiple Subchannel Sets (MSS)
  - 63.75K Subchannels for Set-0
  - 64 K subchannels for Set-1
  - more than doubles the amount of subchannels previously available
- 256 Channels per LCSS
- Up to 1024 Channels
- Up to 1024 ESCON ports
- Up to 48 OSA-E ports
- Up to 336 FICON Express2 ports
- Up to 16 HiperSockets
  - with IPV6 support
- Up to 16 2.7GB/sec STIs per book

System z9 / z990/z890 Processor Cage Design

MRU components

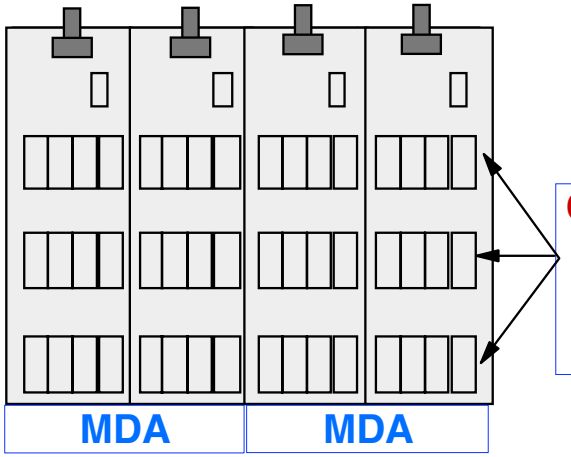
- Modular Refrigeration Unit (MRU)
  - Motor Scroll Assembly (MSA)
  - Motor Drive Assembly (MDA)

Hybrid cooling design



Z frame **A frame**

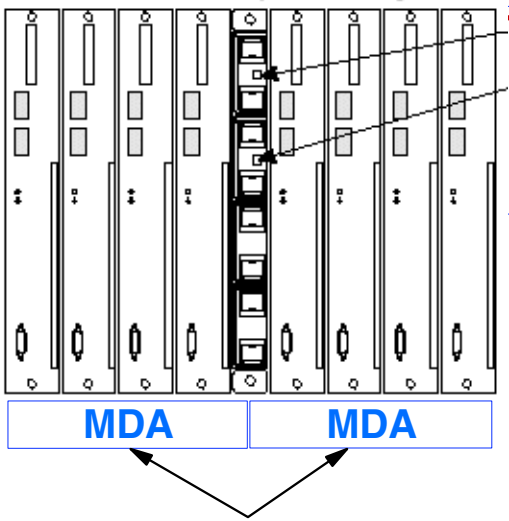
CEC Cage - Front View



One to four books

Each book has STI connections

CEC Cage - Rear View



Two ETR and multiple DCA cards located in rear of CEC cage (N+1)

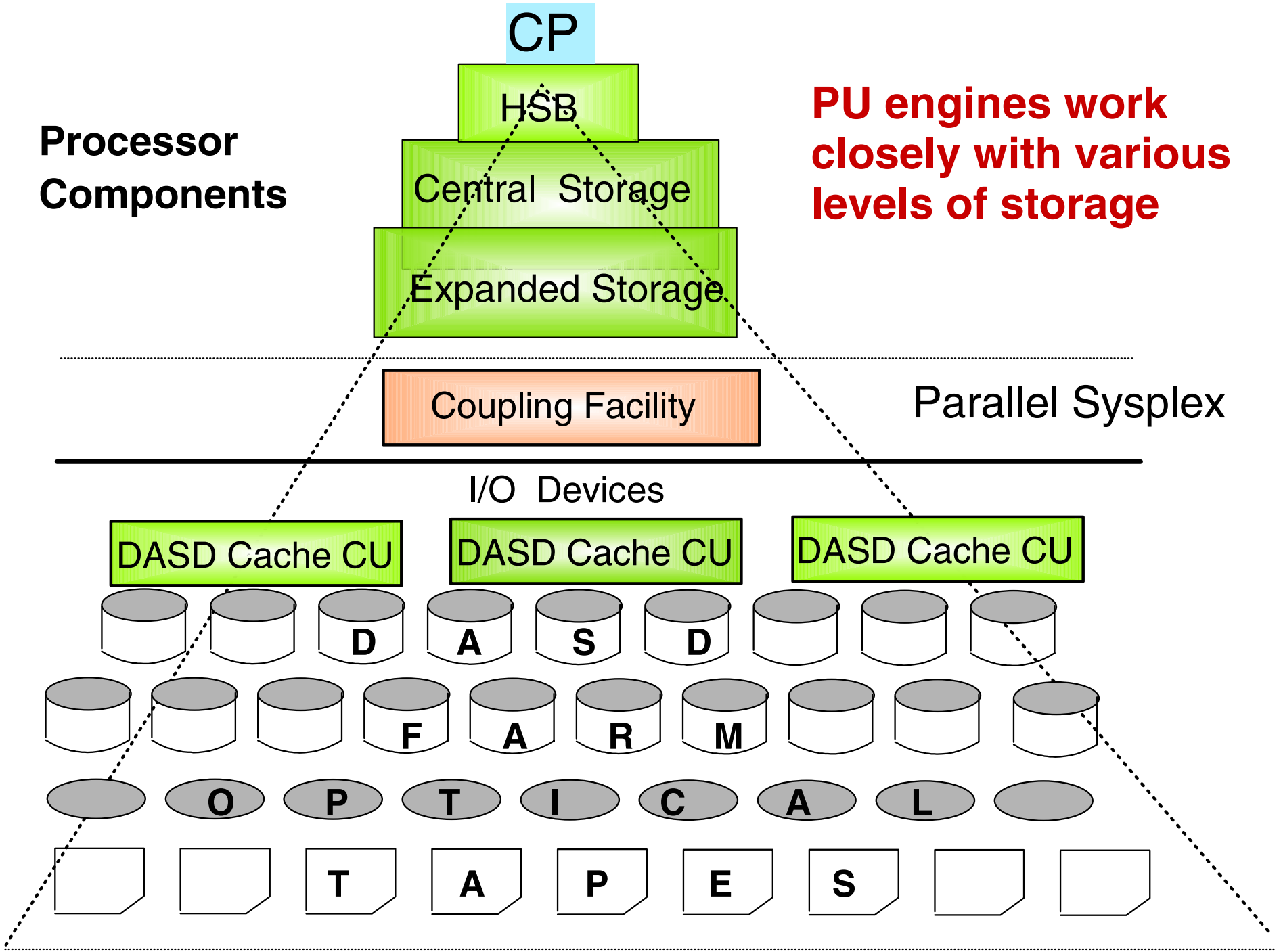
These MDAs are system activated in case of MRU failure

*** z890** - A frame only, one book, MDA used for cooling (N+ 1)

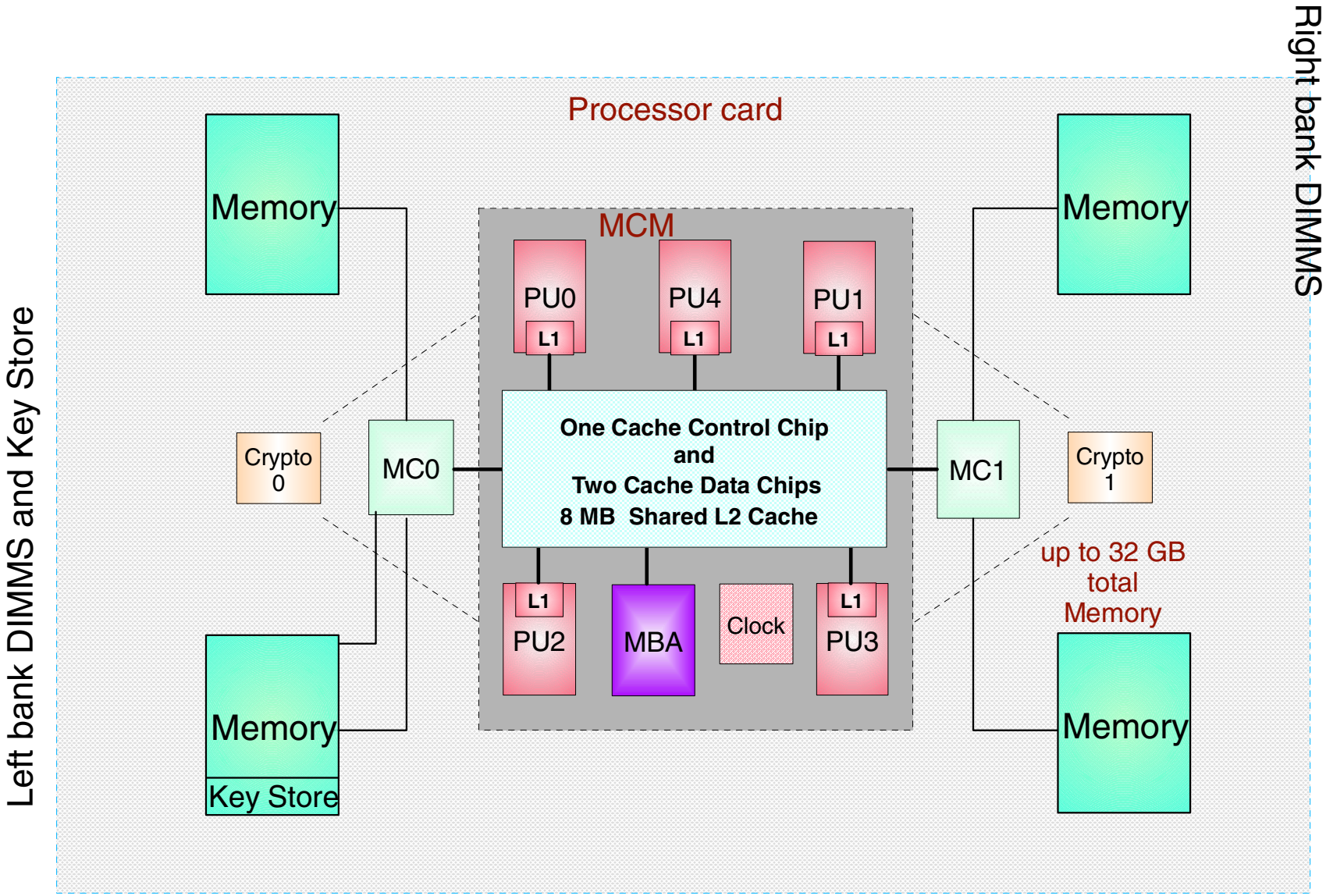
Processor Units Assignments

- A PU can be assigned (characterized) as the following:
  - A Central Processor (CP)
  - A System Assist Processor (SAP)
  - An Internal Coupling Facility (ICF)
  - An Integrated Facility for Linux (IFL)
  - zSeries Application Assist Processor (zAAP) **z9/z990/z890 only**
- Unassigned PUs are considered to be spare PUs
  - Any spare PU can be used for CP, SAP, ICF or IFL sparing
  - Spare PUs can also be used for dynamic upgrades (On/Off CoD, CUoD, CIU, or CBU)
  - Number of spare PUs is dependent on PU configuration and model
  - z900 comes with at least one spare PU
  - z990 comes with at least two spare PUs per book
  - System z9 comes with at least two spare PUs per server

Large Systems Storage Hierarchy

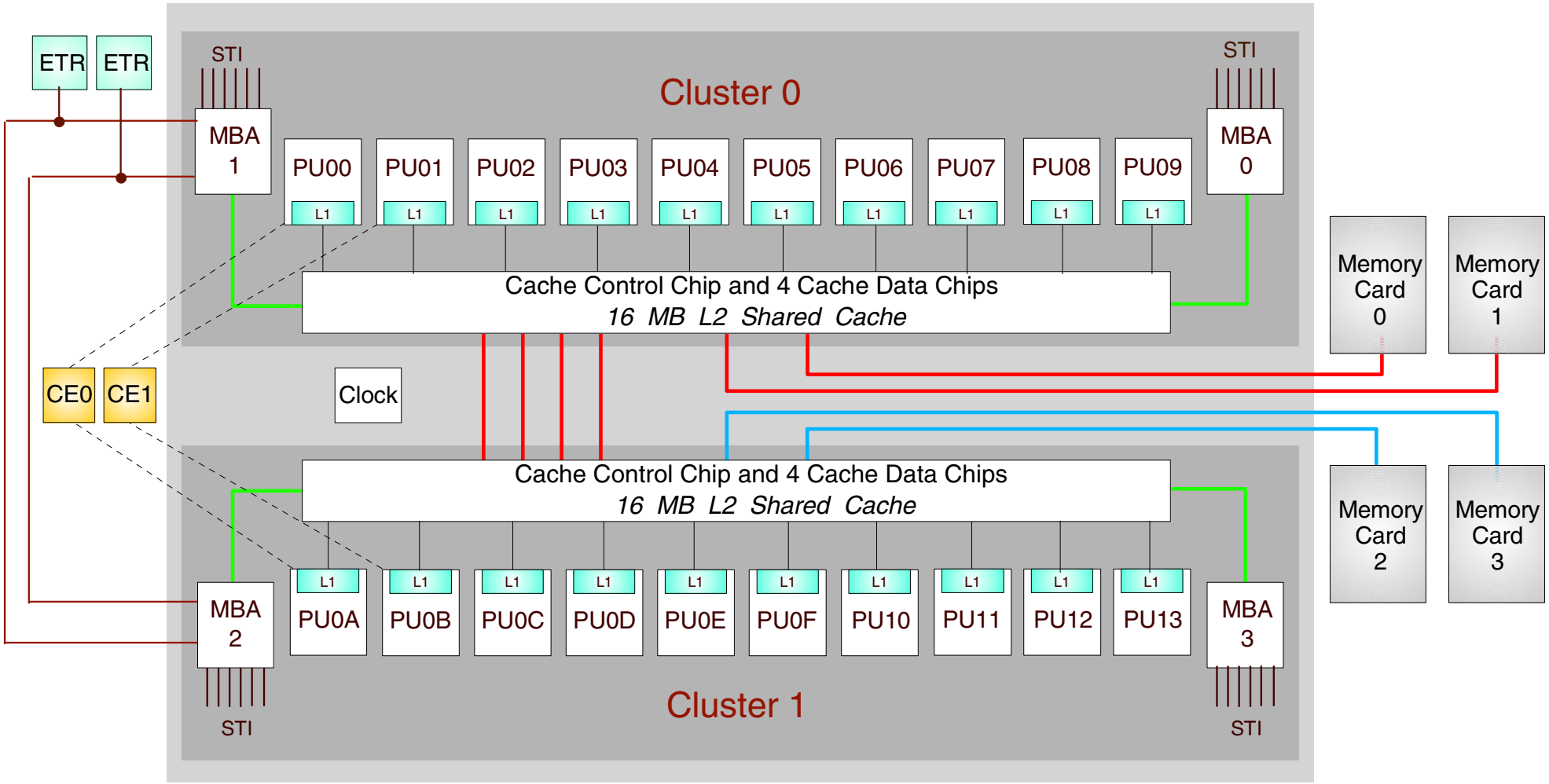


z800 Five-PU MCM System Structure



z900 20 PU MCM System Structure

Number of PUs (12 or 20), Memory cards (2 or 4)

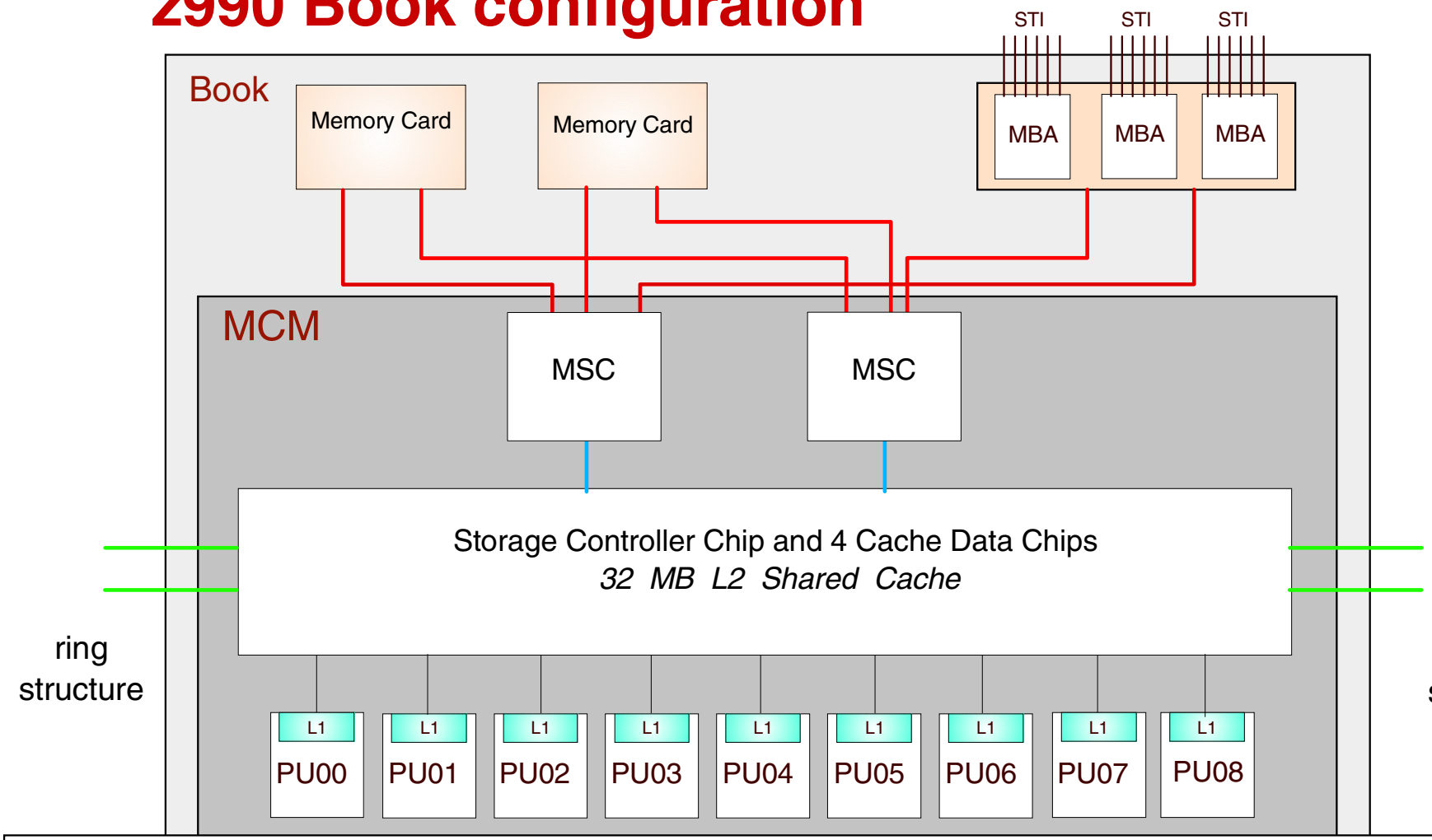


Self Timed Interfaces (STIs) provide all connectivity to I/O via various channel cards and cable connections

- STIs on the z900 and z800 operate at 1GB/sec

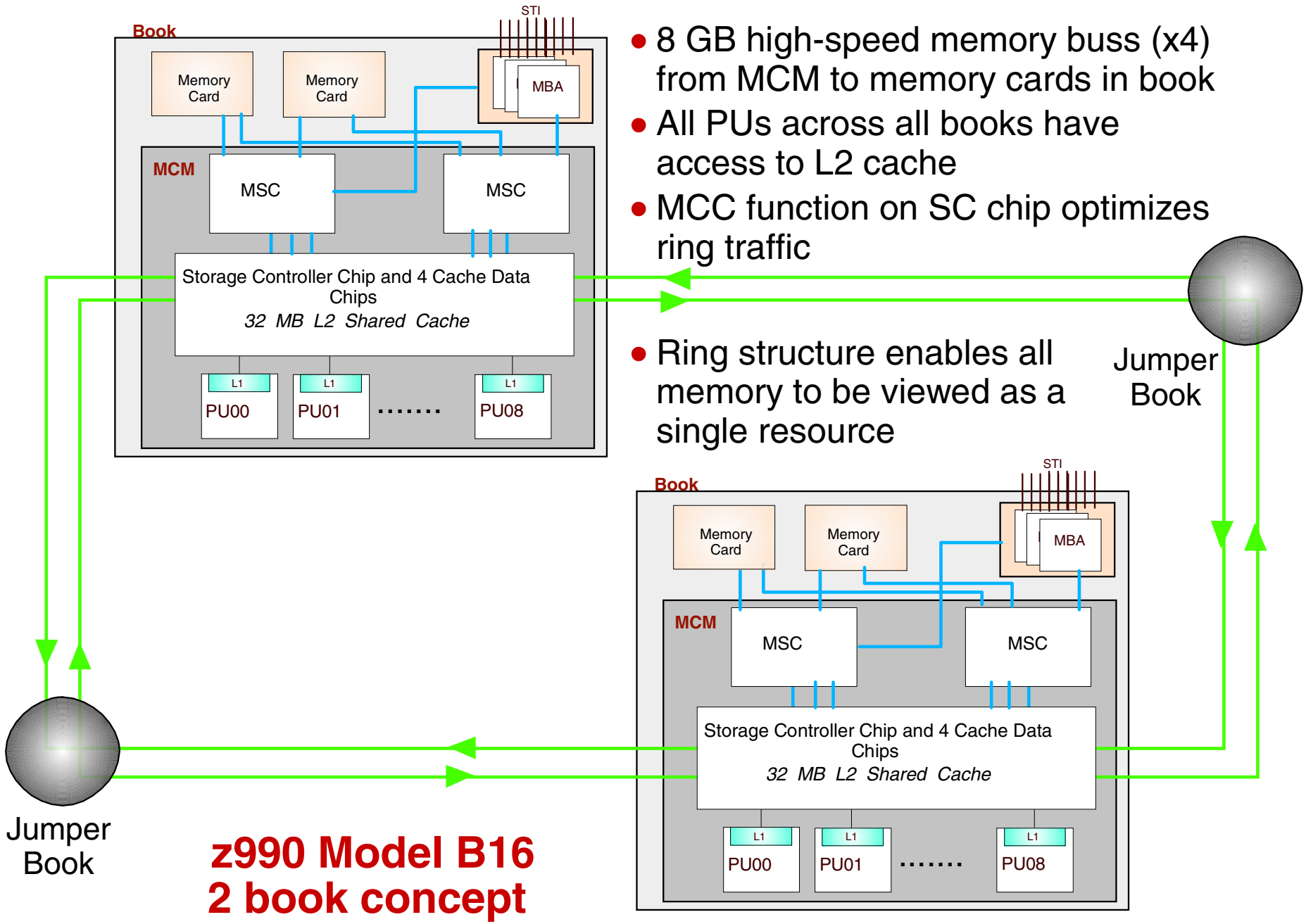
z990/z890 Book and MCM System Structure

z990 Book configuration



- z890 Book configuration similar, with the following exceptions
  One Memory card, Two MBAs, 5 PUs
- System z9 109 book concept is similar, however number of PUs, memory, MBA and STIs configurations are slightly different

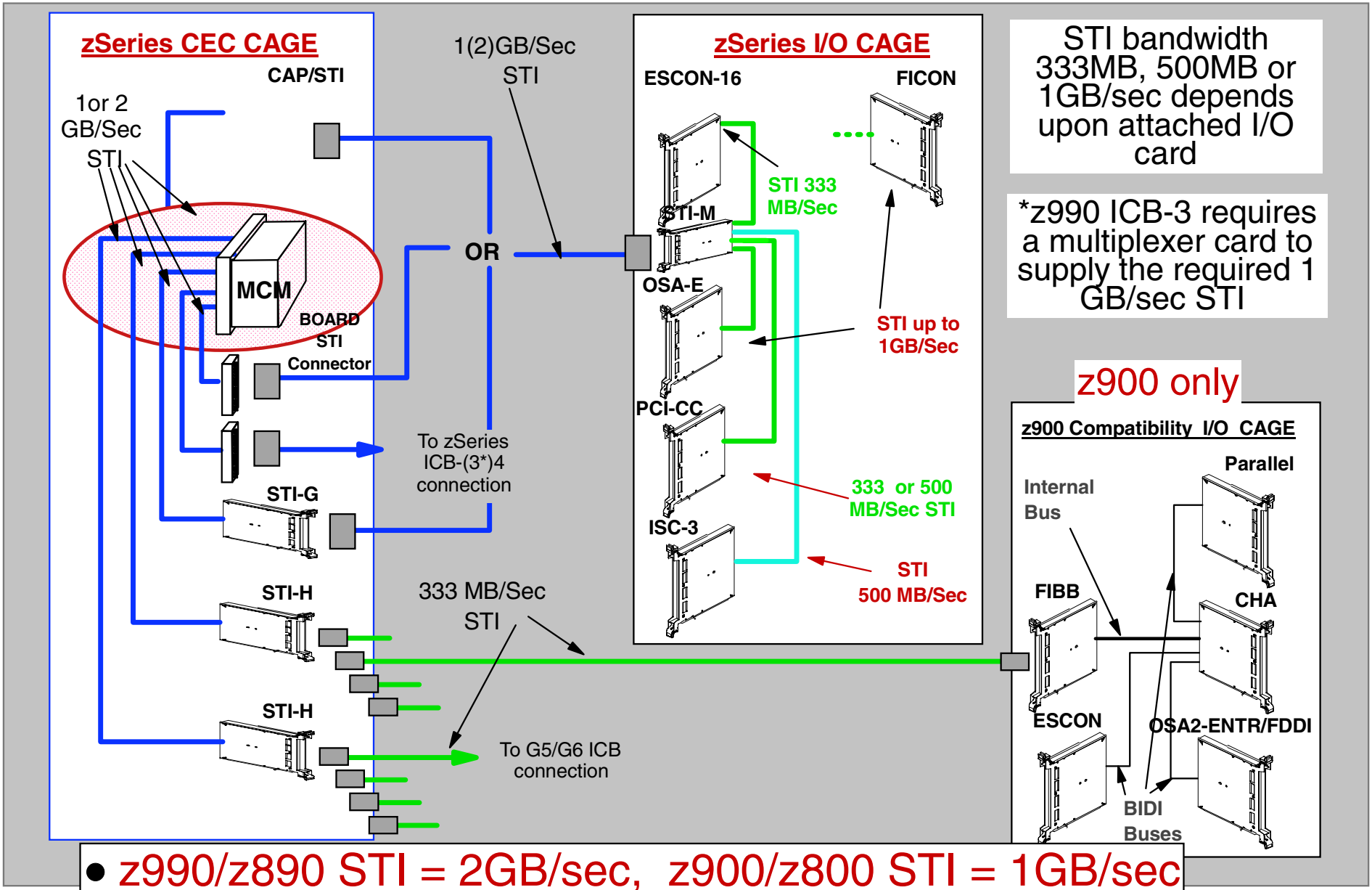
z990 Memory Ring and Book Structure



- 8 GB high-speed memory buss (x4) from MCM to memory cards in book
- All PUs across all books have access to L2 cache
- MCC function on SC chip optimizes ring traffic
- Ring structure enables all memory to be viewed as a single resource

z990 Model B16
2 book concept

zSeries Channel Connections - STIs



- z990/z890 STI = 2GB/sec, z900/z800 STI = 1GB/sec
- Only z900 supports I/O compatibility cage
- System z9 STI = 2.7 GB/sec

CPs, SAPs, STIs - Putting the Pieces Together

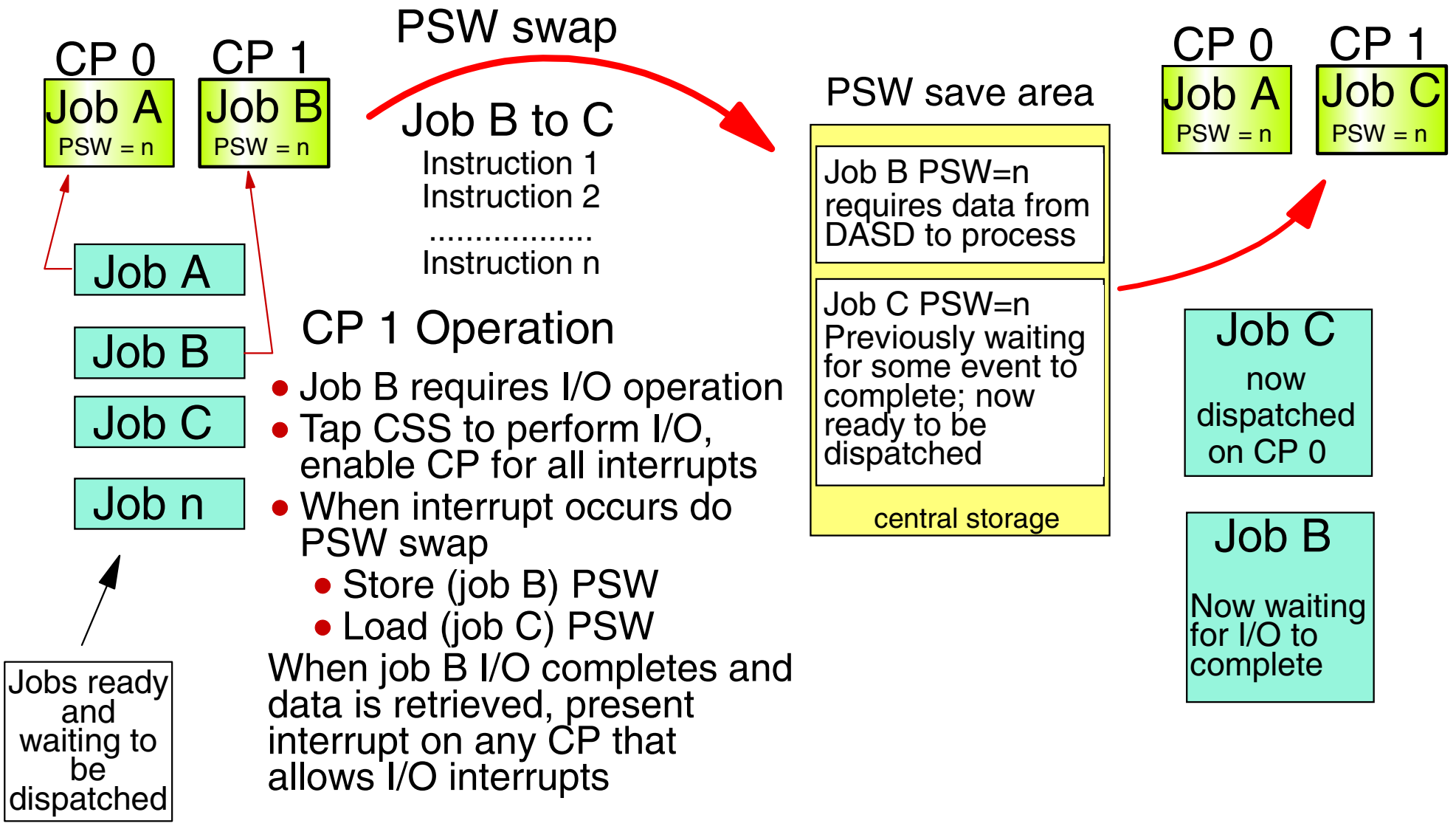
CPs, SAPs, cache, and I/O adapters via the STIs all work together to process instructions and I/O requests.

- CPs process instructions
- SAPS work with the CSS and processes I/O requests via the I/O adapters

Server architecture in conjunction with the operating system provide

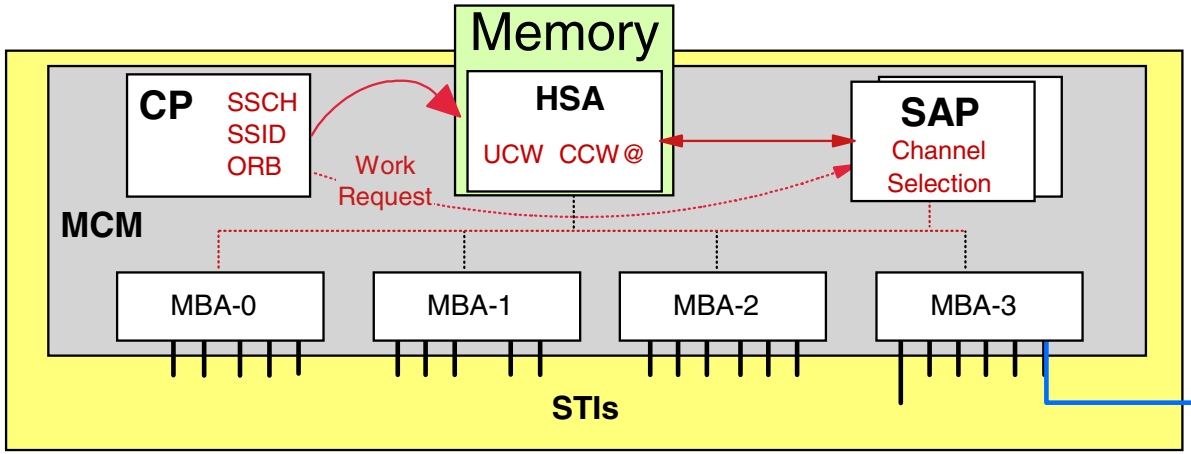
- Hardware registers and formatted areas of storage
  - The Hardware System Area (HSA) stores information that the CSS needs to process requests
  - The Program Status Word (PSW) register (one for each CP) contains information required for the execution of the currently active program.
    - Status, interrupts, instruction sequencing
    - Status of the CP can be changed by loading a new PSW or a PSW swap

PSW Swaps and Interrupts (Concept)

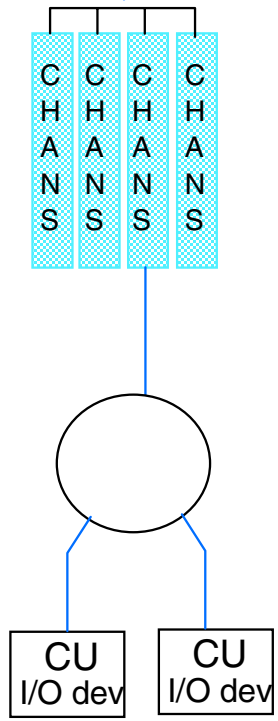


Program Status Word (PSW) - One for each CP, contains status information and next instruction address to be processed.

CSS I/O Operation Overview



- The program working with the access method and IOS provides the channel program and other information in various control blocks. Start subchannel is issued to the CSS to start the I/O operation
- The CSS utilizes a SAP to perform all I/O functions. The CSS works with the subchannel stored in HSA.
- HSA contains reserved storage that is used for specialized functions. Subchannels used for channel operations contains status, channel paths, and other necessary information for I/O operations to a given device. There is one subchannel for every I/O device.
- CCWs and data is passed to the MBA, and exits the MCM through backboard wiring or external cables to the selected channel card. Connected to the channel cards are external fiber or copper cables.



zSeries Educational Offerings

Sysplex / zSeries course offerings

- H4016 (2 days) HMC Class
- H4041 (3) Plex Ops & Recovery (Sysplex only)
- H4057 (5) Plex Ops & Recovery (H4016 & H4041)
- ES902 (5) Advanced Plex Recovery
- ES420 (5) Plex Implementation
- ES830 (5) CSAR (Complex Systems Availability & Recovery)
- ES820 (2) System z9 and zSeries Mainframe Environment (A Technical Overview)
- OZ09 (2) z/Architecture for z900 and z800
- OZ05 (2) System z9 / zSeries 990/890 Technical Update & Configuration
- OZ96 (5) zSeries Channel Architecture, ESCON/FICON Operation and PD
- ES326 (3) FICON(fc,fcv,fcp) Planning, Implementation, Operation and PD
- ES960 (4) HCD and Dynamic I/O
- ES270 (3) z/OS and OS/390 System Operations

RETURN TO INDEX