IBM Systems and Technology Group

Silicon Technology Outlook

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Agenda

- Intro
- CMOS Scaling
- Lithography
- Device innovations
- The third dimension

IBM Technologies……..

IBM DB2

WebSphere software

IBM COGNOS

ILOG An IBM Company

IBM WATSON

IBM SPSS

Linux

IBM PureSystems
THE NEXT GENERATION PLATFORM

IBM Kenexa

Blue Gene

z/VM

NETEZZA

i2 An IBM Company

POWER7 BUILT ON Power

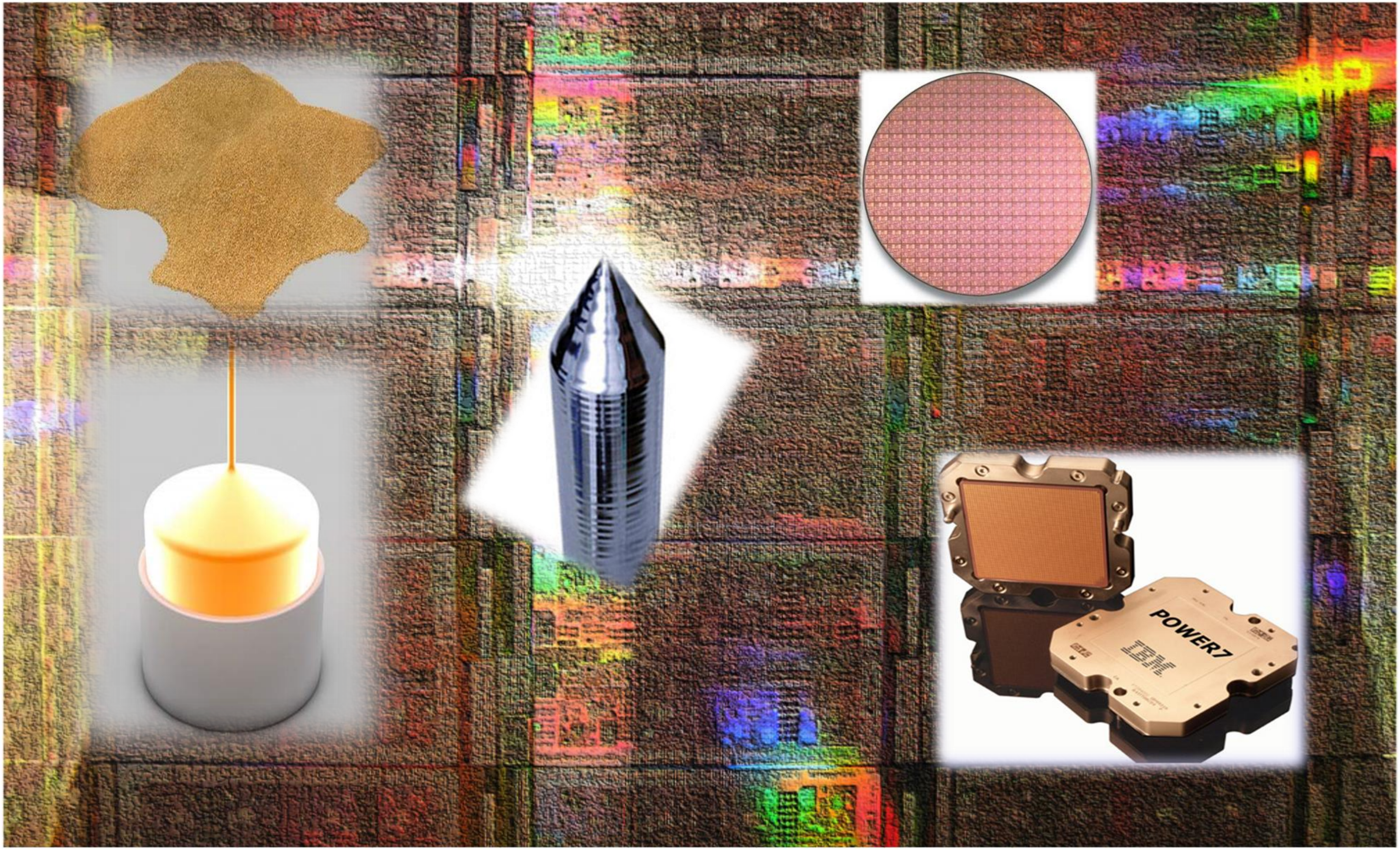
z/VSE

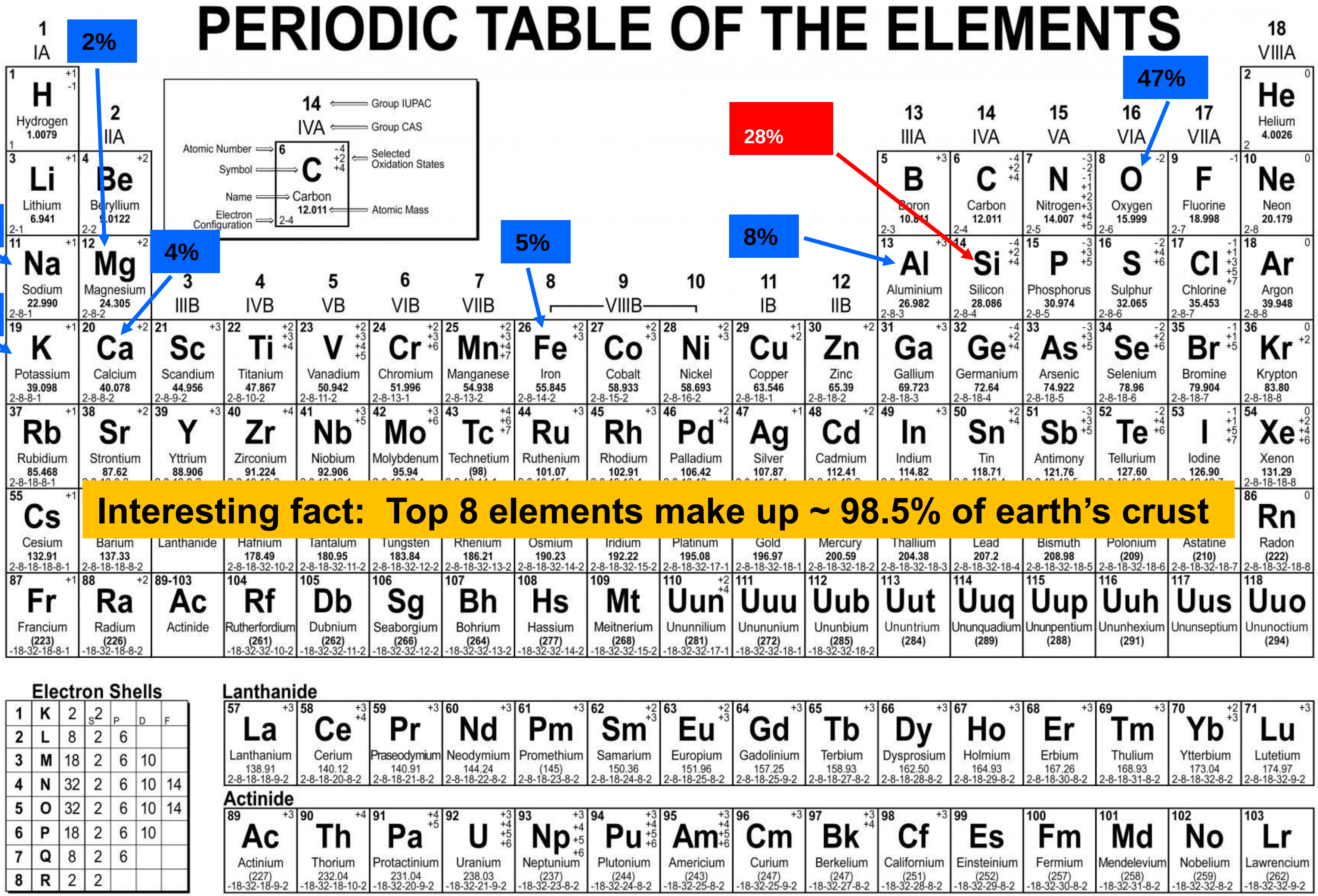
IBM InfoSphere

IBM zEnterprise Systems

All build on sand ....

Fortunately we know how do turn sand into hardware



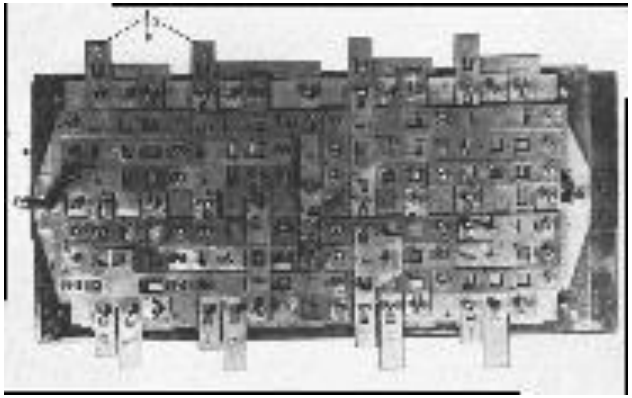


Interesting fact: Top 8 elements make up ~ 98.5% of earth's crust

It started different

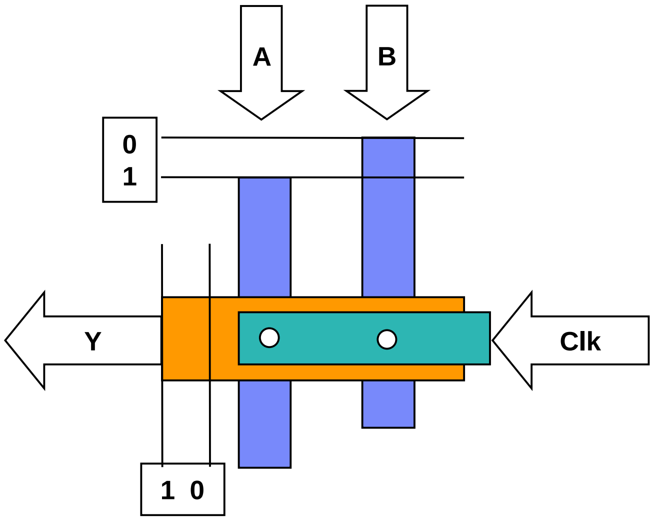
Konrad Zuse Z1

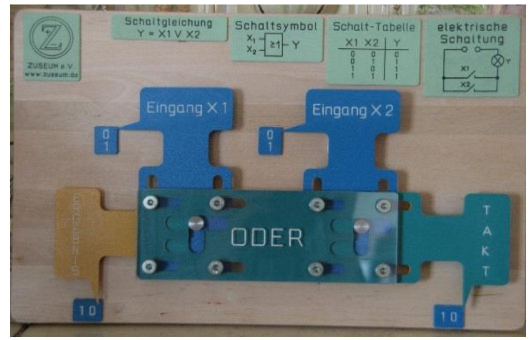
- First freely programmable computer using
  - Boolean logic
  - Binary floating point
- Build between 1936-1938 during WW II in Berlin
- Contained all parts of a modern computer
  - Control unit
  - Memory
  - Micro sequences
  - Floating point unit
  - Two registers
- Technology: mechanical via metal sheets
  - Driven by manually or optinal electrical motor from a vacuum cleaner
  - Never worked flawlessly due to mechanical problems



Source: http://user.cs.tu-berlin.de/%7Ezuse/Konrad_Zuse/en/rechner_z1.html

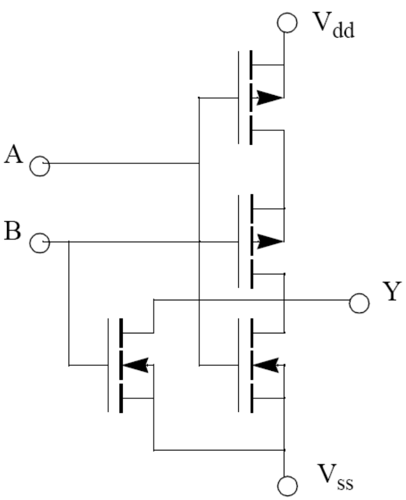
Metal sheets vs CMOS transistors:

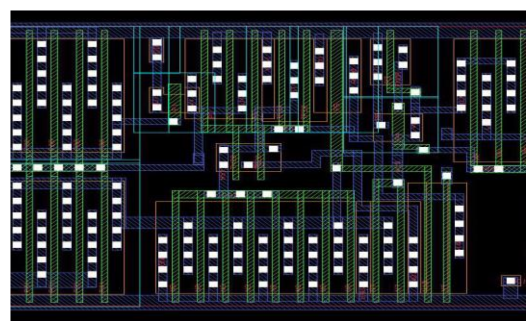




4 metal sheets to build a logic gate

2 inputs, 1 output, 1„clock“
=> 30000 metal sheets represent 7500 logic gates

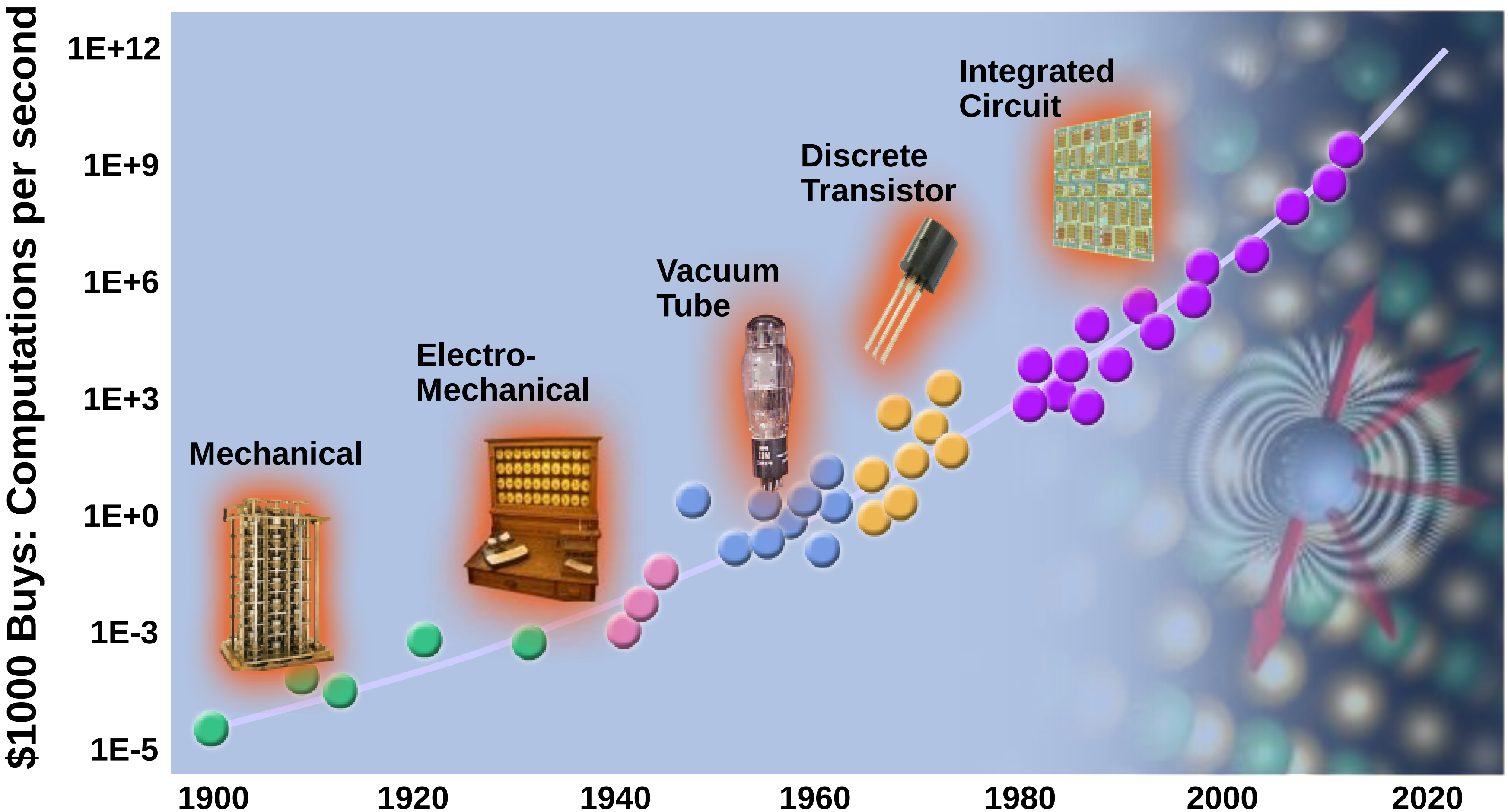




4 CMOS transistors per logic gate

CMOS needs two complementary pairs of CMOS transistors
Six CMOS transistors for a single memory cell

Moore‘s Law or What do a 1000 $ buy?

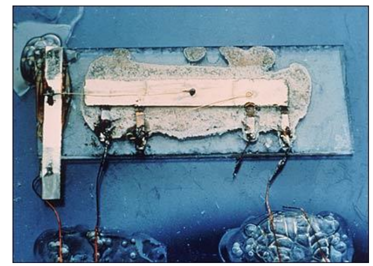


Source: Kurzweil 1999 – Moravec 1998

CMOS Scaling

- ***Transistor (1947), Bardeen, Brattain & Shockley***

- ***First integrated circuit (1959), Kilby***



- ***Moore‘s Law (1965)***

  „Cramming more components onto integrated circuits“
  Complexity of chips doubles every 24 months

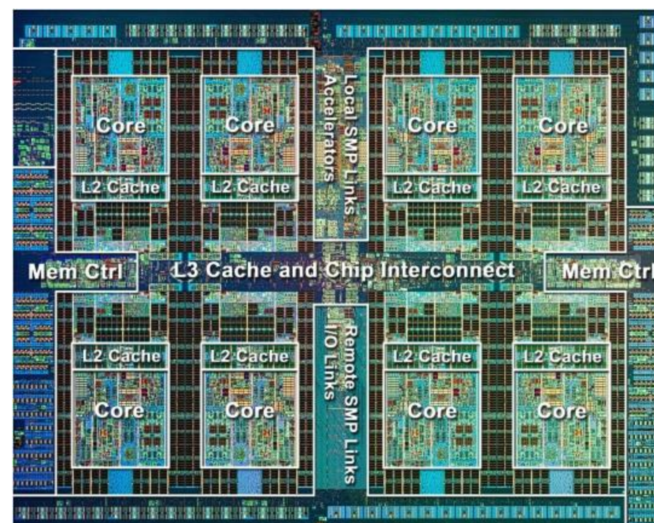
  .
  .
  .

- ***Cell Processor (2005)***
  234 Million Transistors in 90nm Technology

- ***POWER 6 (2006)***
  790 Million Transistors in 65nm Technology

  .
  .
  .

- ***POWER 7+ (2012)***
  2.1 Billion Transistors in 32nm Technology



Trends Observed Across Industry (ISSCC 2013 Supplement)

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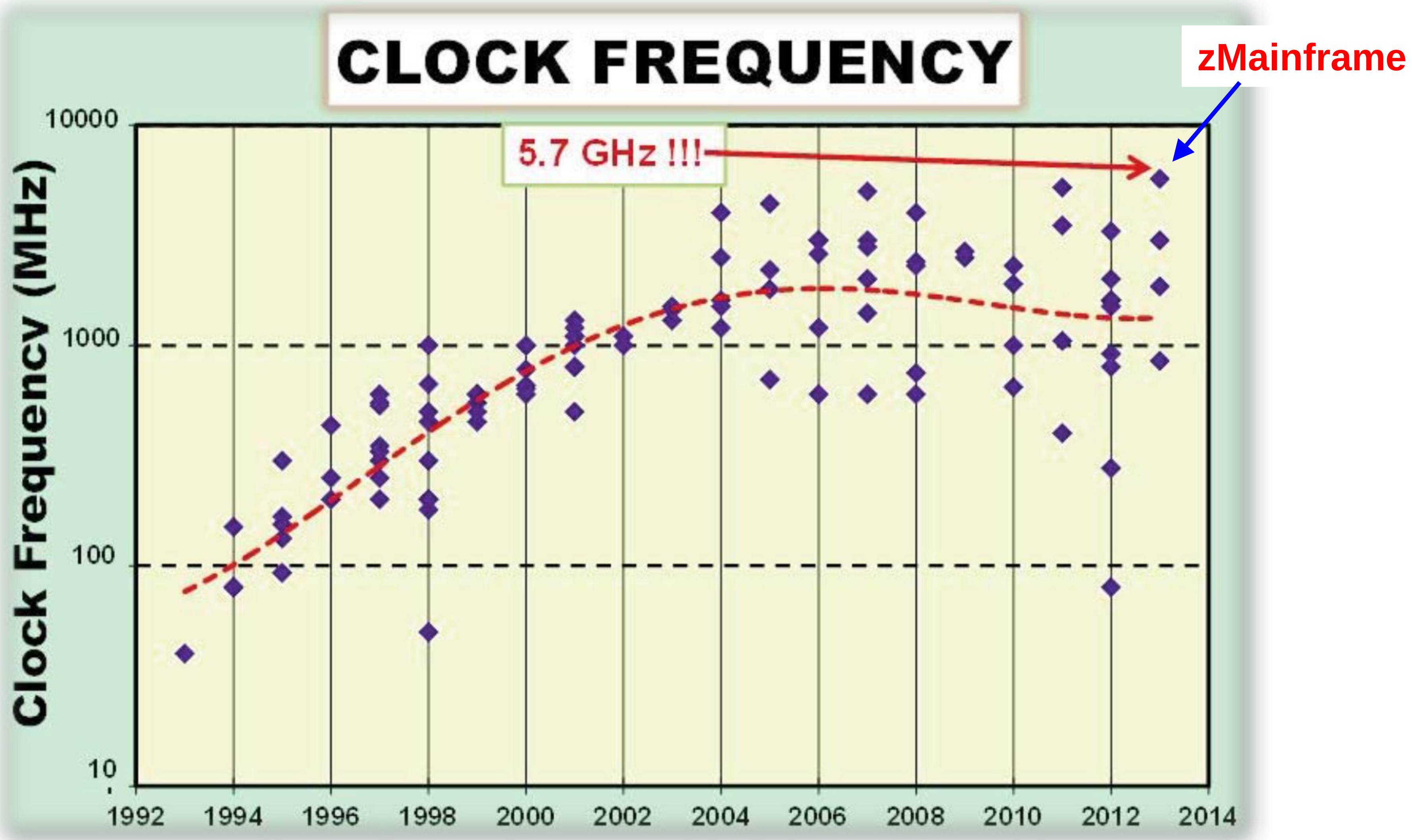
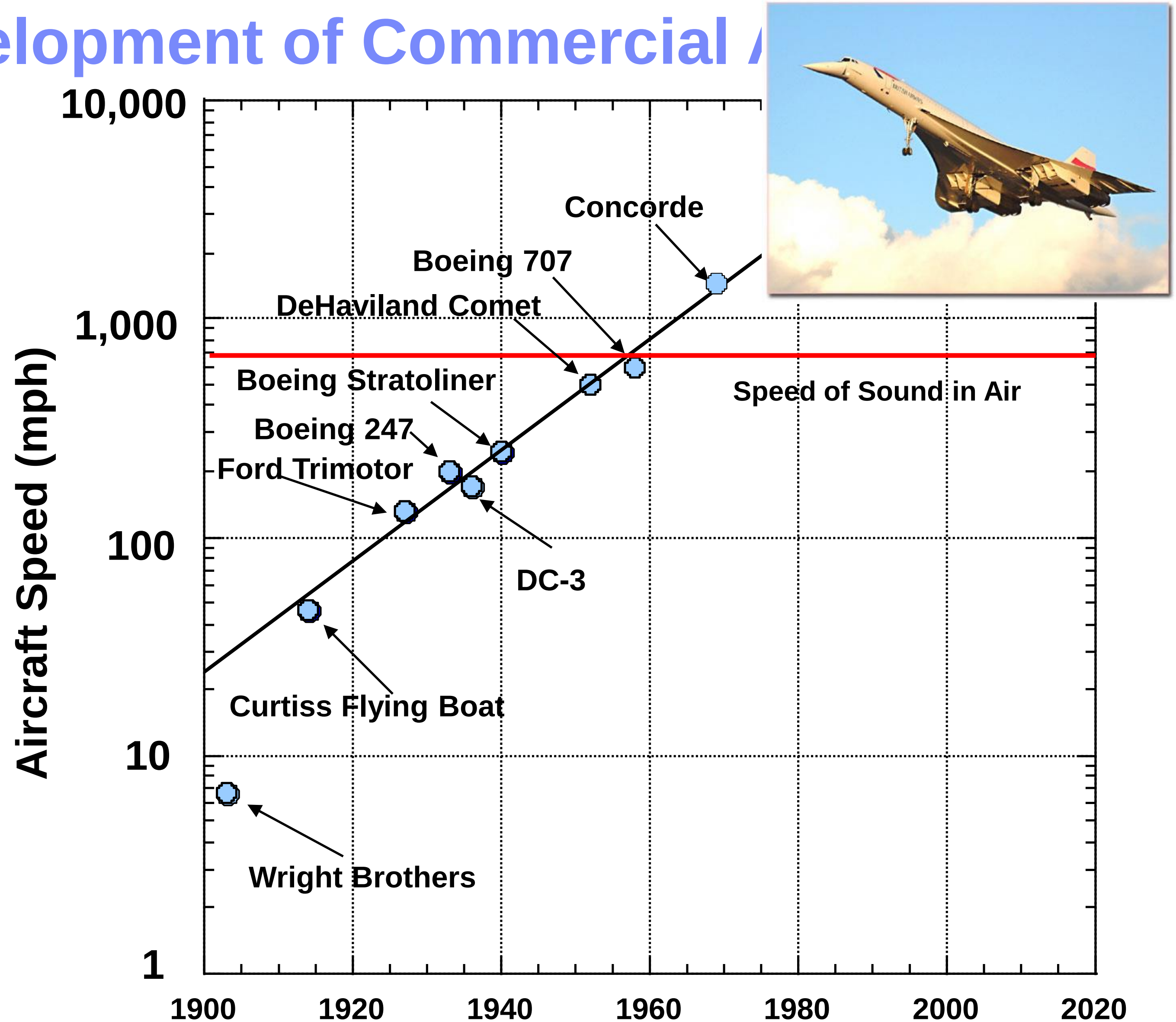
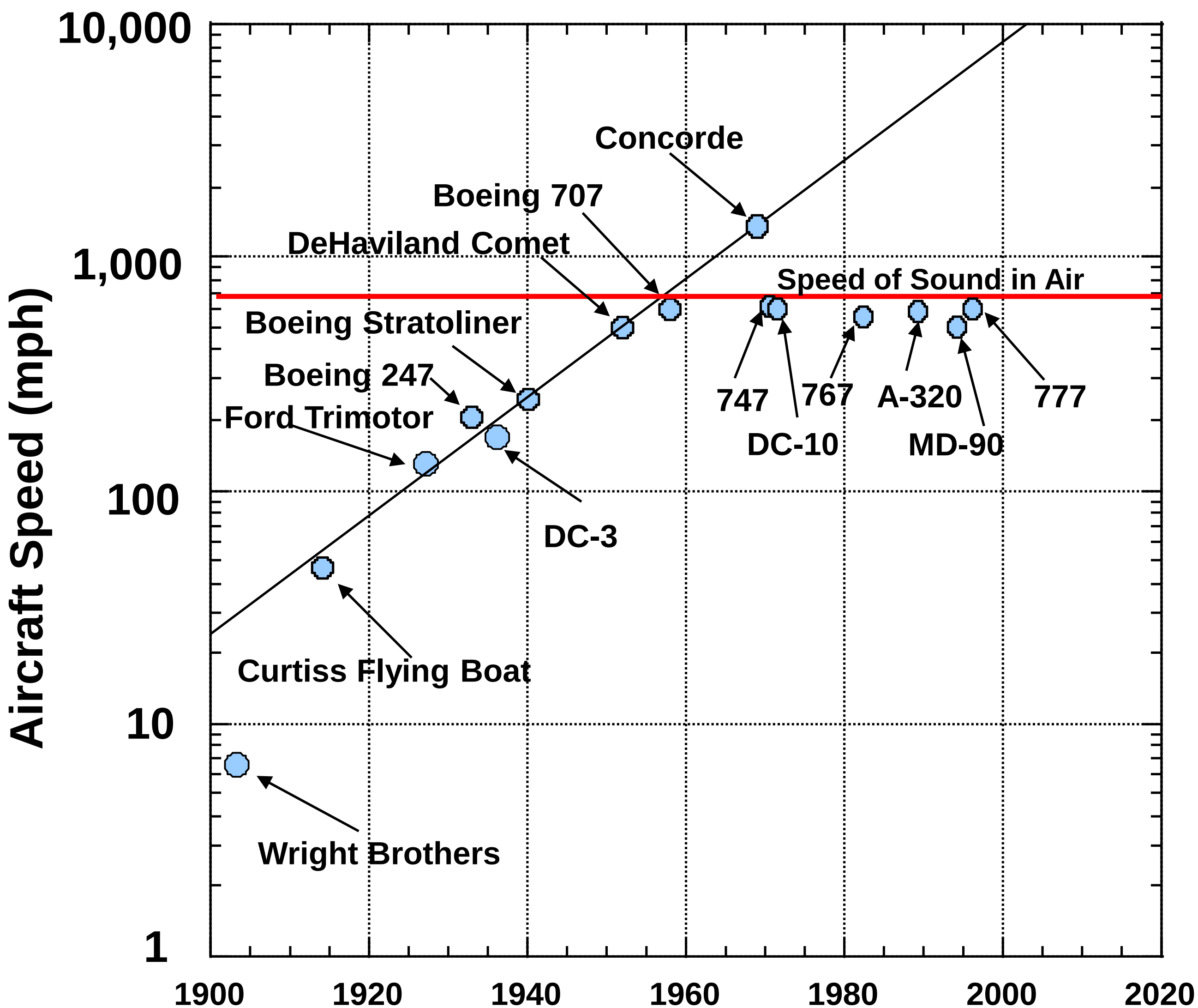


Development of Commercial



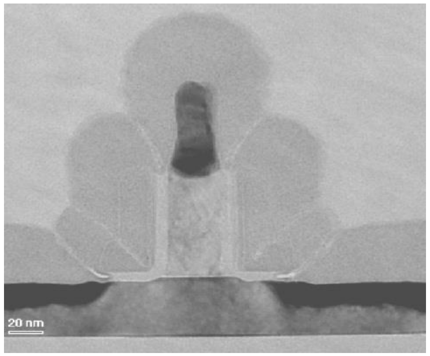
Source: F. M. Schellenberg, UCB Bodega Bay, 5-10-2007

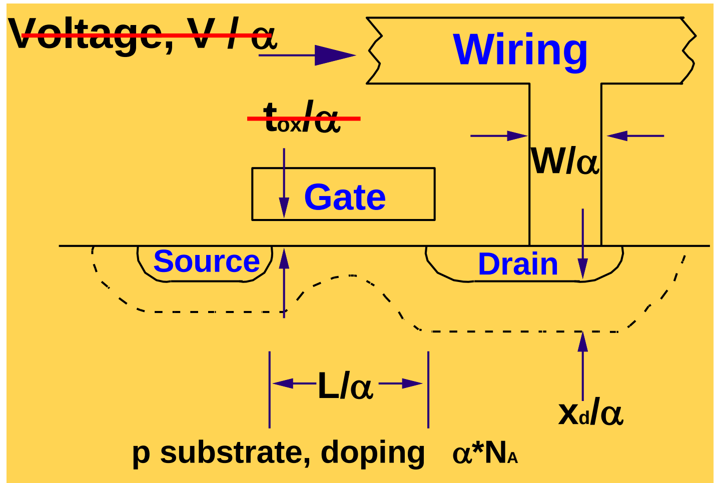
Commercial Aviation



Source: F. M. Schellenberg, UCB Bodega Bay, 5-10-2007

Traditional CMOS Scaling (Dennard, 1974)





<u>Channel Effects</u>

- Drain Induced Barrier Lowering
- Increasing Ioff
- Vt dependence on Vds
- Sub-threshold slope

< 65 nm

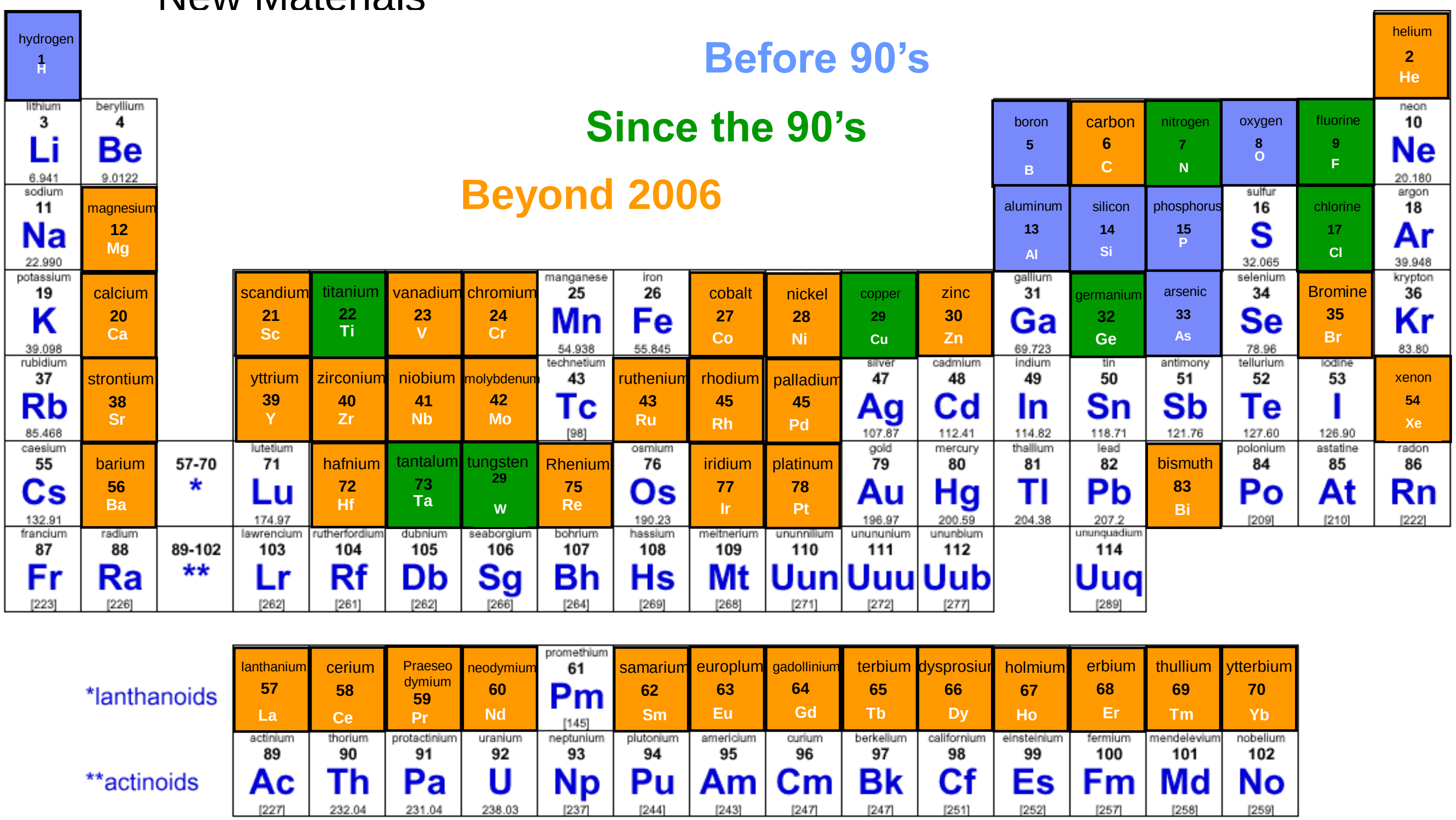
SCALING:	
~~Voltage:~~	~~V/α~~
~~Oxide:~~	~~tox /α~~
Wire width:	W/α
Gate width:	L/α
Diffusion:	xd /α
Substrate:	α * NA

Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
~~Power Density:~~	~~~Constant~~

Improving Performance

No longer possible by scaling alone

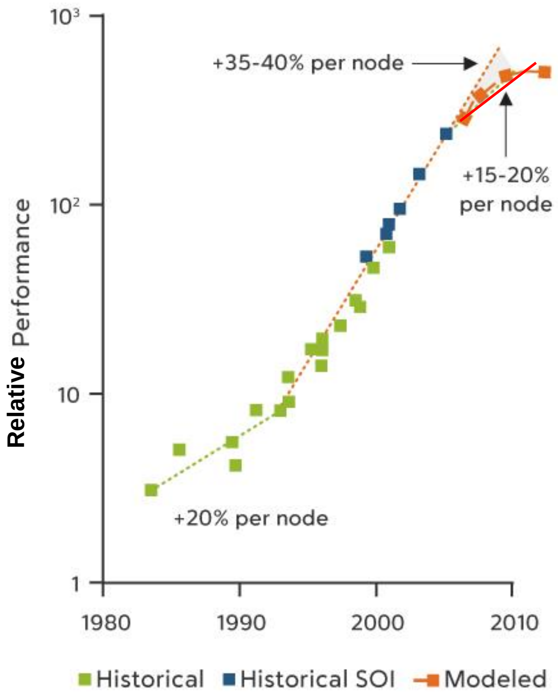
- New Device Structures
- New Device Design point
- New Materials



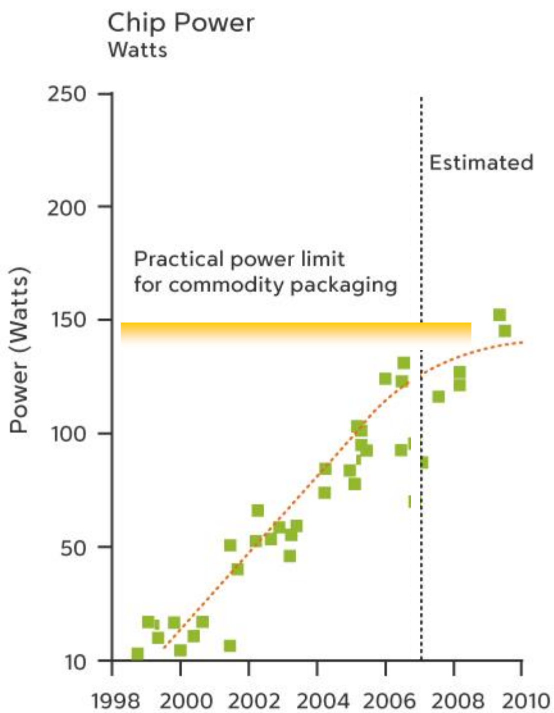
CMOS Technology Trends

Conventional CMOS scaling benefits are diminishing.

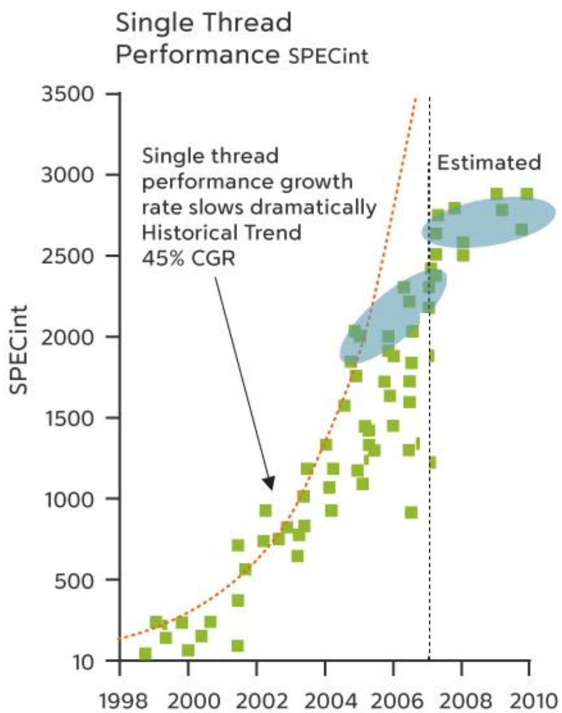
Transistor performance scaling to continue, but at a slower rate



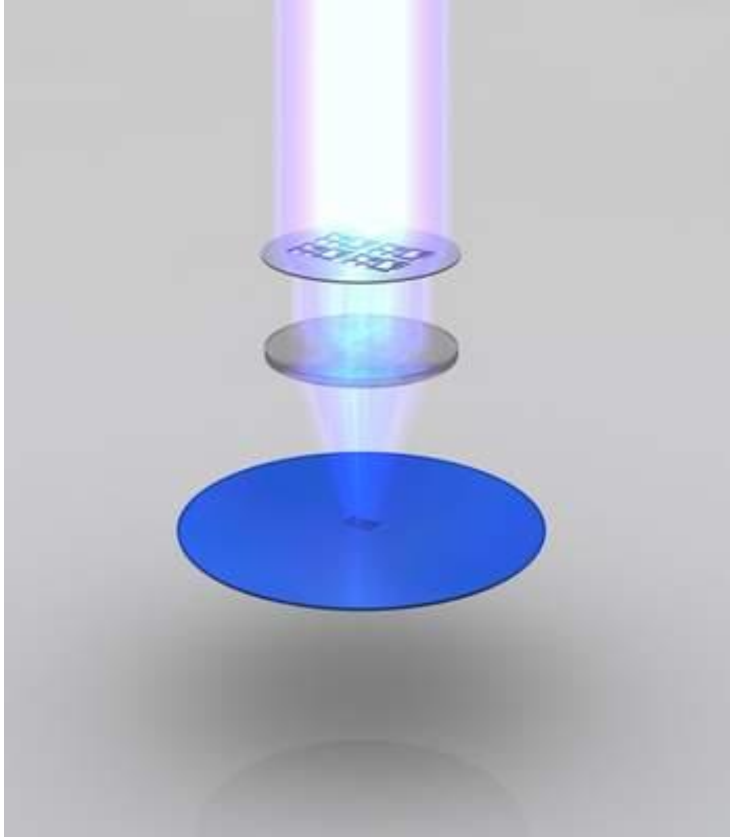
Power is limiting practical performance



Single thread performance growth is slowing dramatically



Lithography



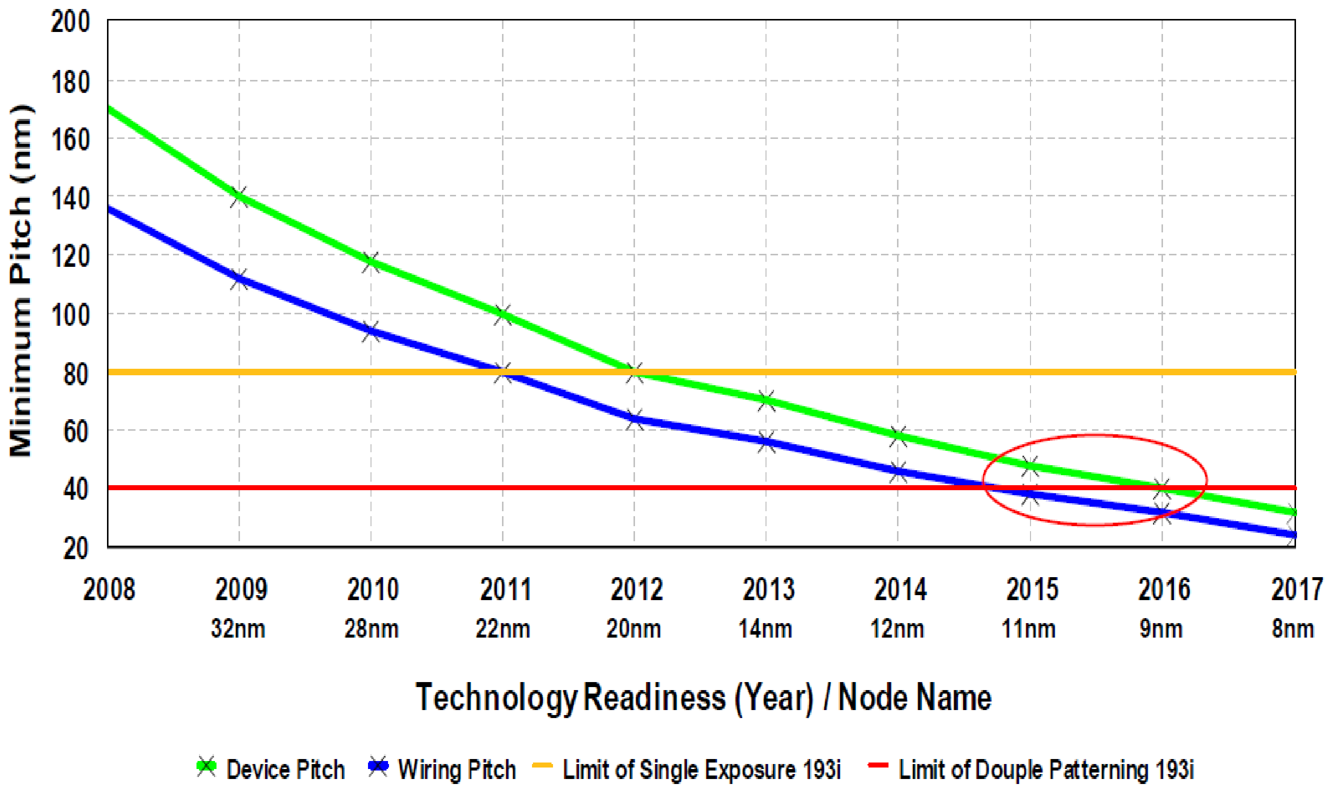
Pushing the Physical Limits of Optical Lithography

- Historically driven by lowering wavelength or increasing lens numerical aperture
- Immersion lithography with 193nm extended for five generation through 10 nm

  double patterning, implementation of restricted design rules, etc…
- EUV offers a return to single patterning with 13.5nm wavelength
  - facing many delays in maturation (radiation source power output)

    => EUV still carries significant risk going forward

- Targeting insertion of EUV at 7nm node
- "Invention required" past 5nm



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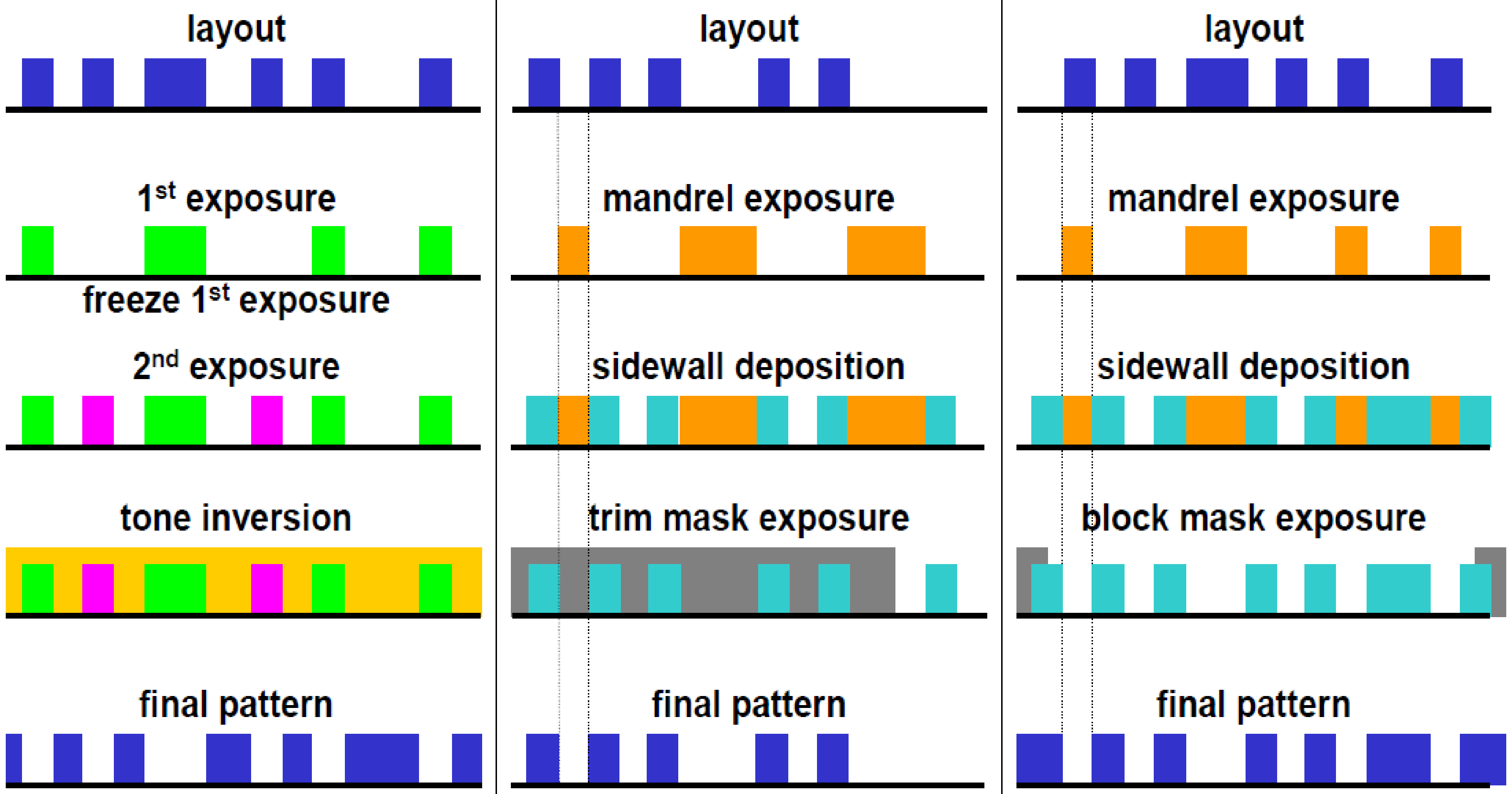
Double pattern Variants

Pitch Split (litho freeze litho etch = LFLE) | **Sidewall Image Transfer** (background mode) | **Sidewall Image Transfer** (foreground mode)



Pitch Split (LFLE): Overlay affects space, bimodal size distribution.

Useful for: local interconnect, via, wires

Sidewall Image Transfer (background mode): Fixed feature width.

Useful for: poly-gate

Sidewall Image Transfer (foreground mode): Discrete feature spaces, no stitching possible.

Useful for: wires

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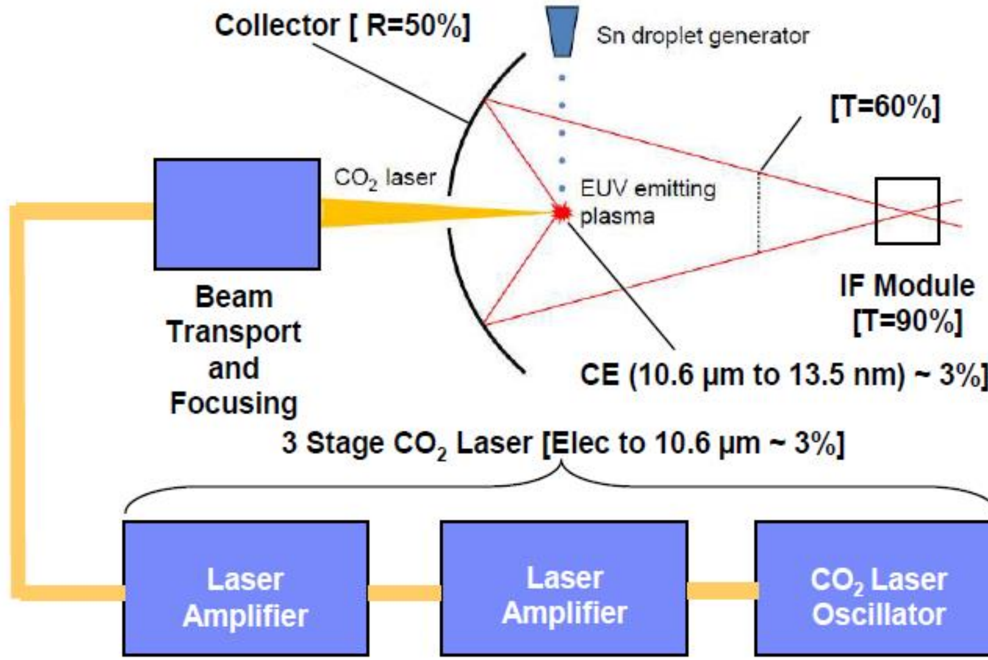
EUV: extreme ultra-violet lithography

ASML's exposure system

Cymer's EUV source



Conversion from wall plug to EUV: ~ 0.02%

Program is making steady progress.

Source power, resist line-edge roughness, mask-blank defects, optics lifetime, overall system cost… remain a challenge

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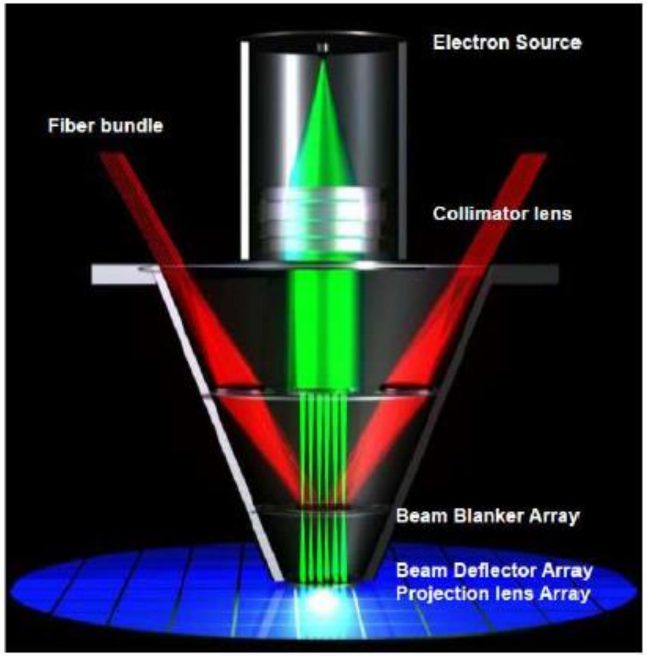
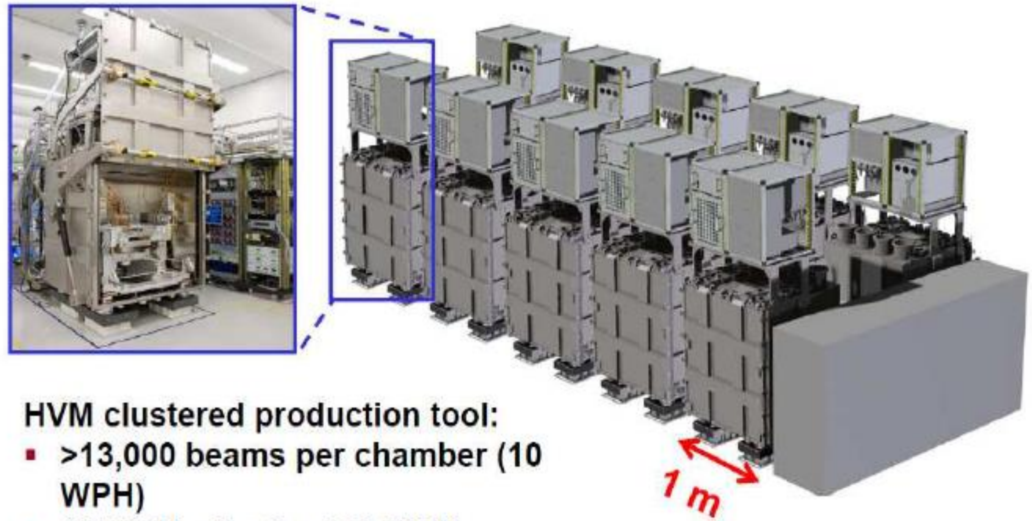
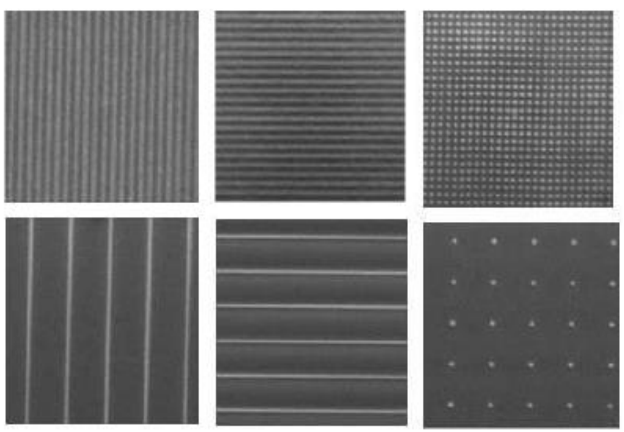
MAPPER: multiple e-beam mask-less lithography





HVM clustered production tool:
- >13,000 beams per chamber (10 WPH)
- 10 WPH x 5 x 2 = 100 WPH
- Footprint ~ArF scanner



- 110 beams working
- Each beam covers a 2x2μm² block
- Met CD mean-to-target & CDU spec

Multiple E-beam Decisions for 22nm and Sub-22nm Lithography, B.J. Lin tsmc, Inc. , Synopsys 2010 TechForum

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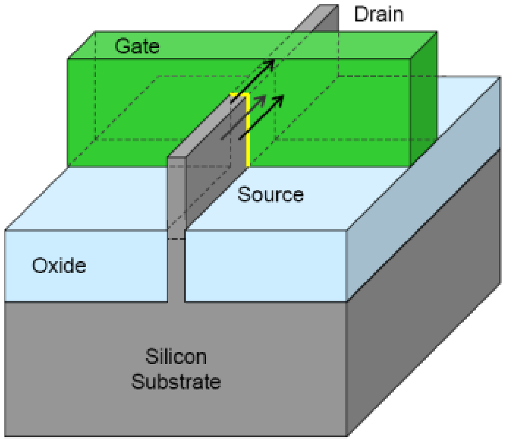
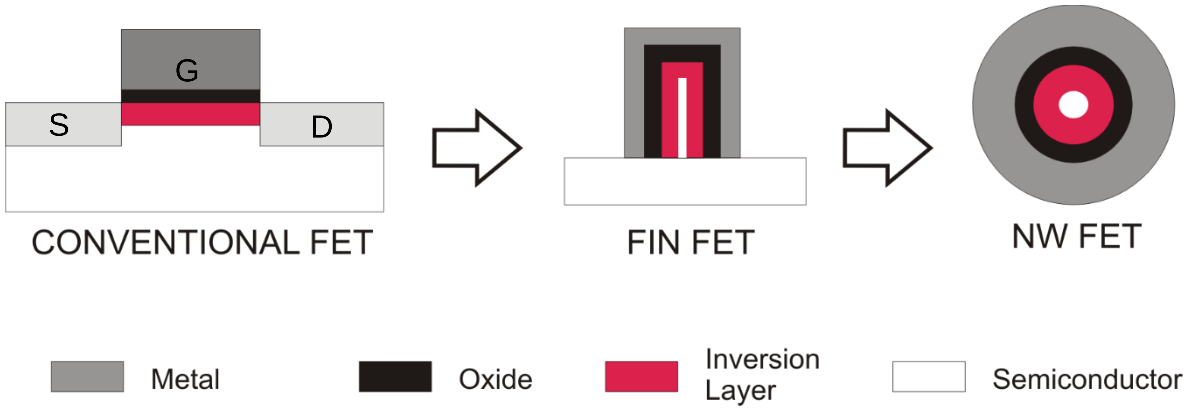
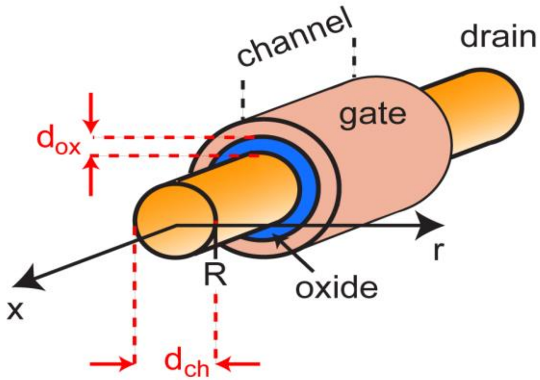
Devices inovation

Electrostatic control of the channel depends on the gate architecture (gate control).

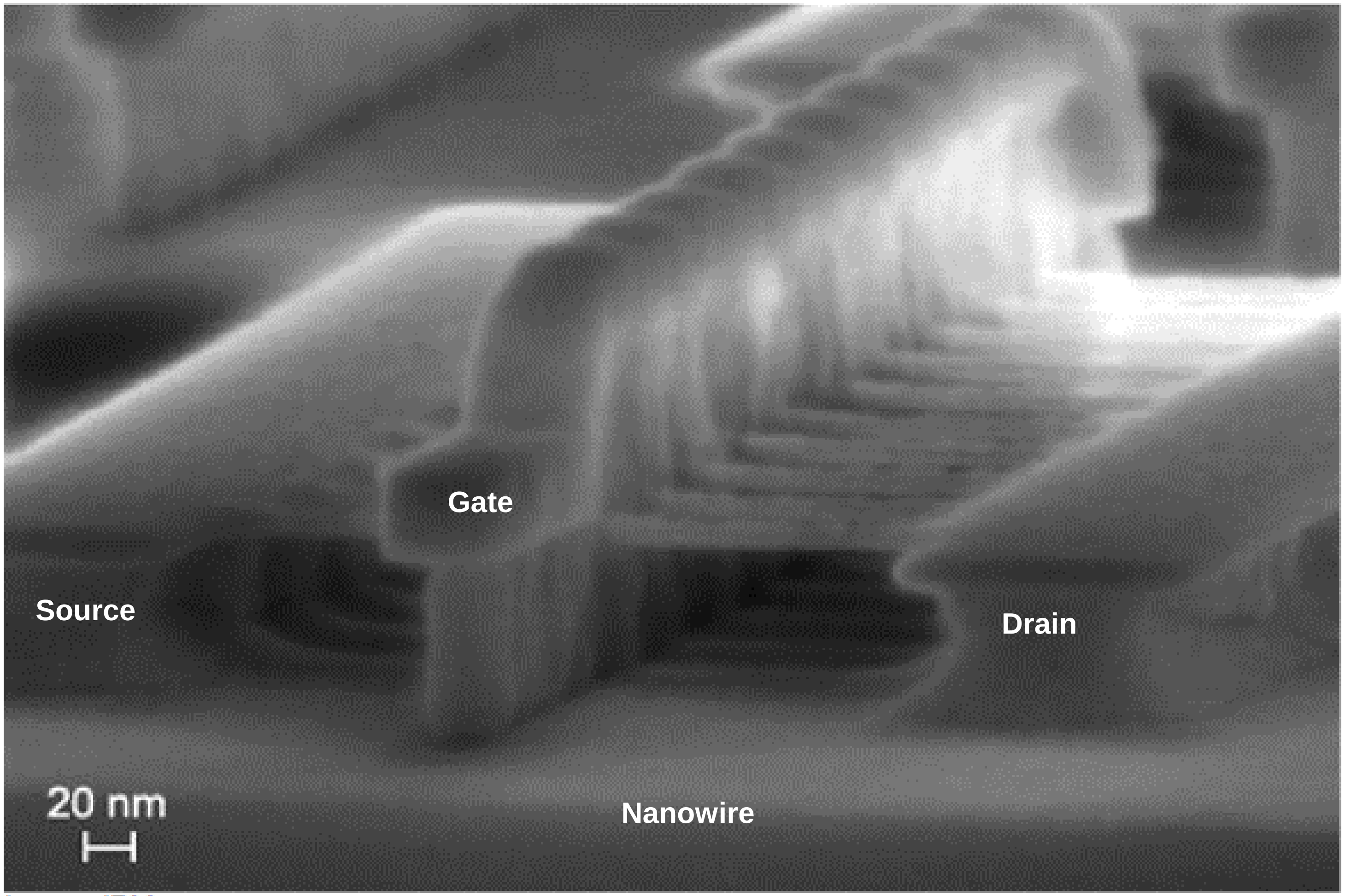




- **Nanowire offers optimum electrostatic gate control of channel**
- Improved scaling: L_g ~1.5 diameter
- Reduced leakage current/power



Silicon Nanowires, 5nm and beyond

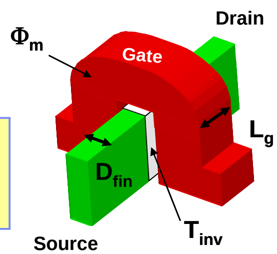


Potential device roadmap

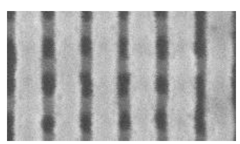
Node: 22nm | 14nm | 10nm | 8nm | 6nm | 5nm

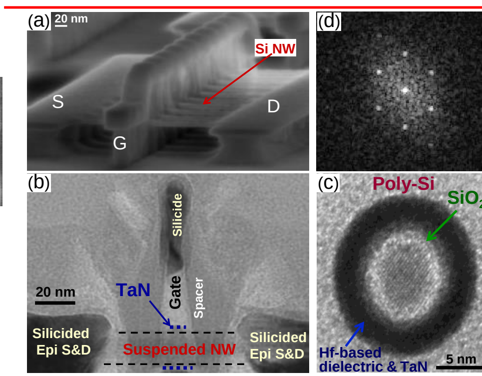
Device:
- **Planar** (22nm): PDSOI
- **FinFET / Nanowire** (14nm – 6nm): Smaller Fins; Nanowires; SiGe pFET; III-V FET
- **Next Generation** (5nm): Tunnel FET; CNT

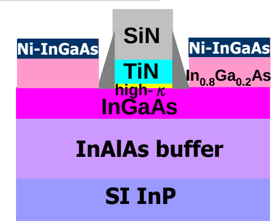
Device Architecture

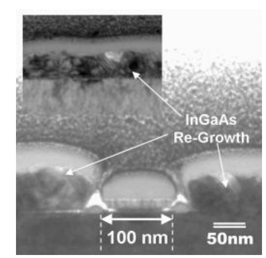


FinFET @ 40 nm CPP

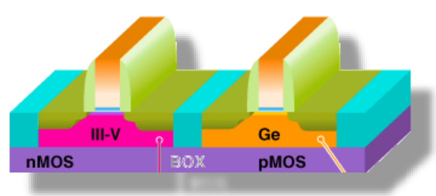




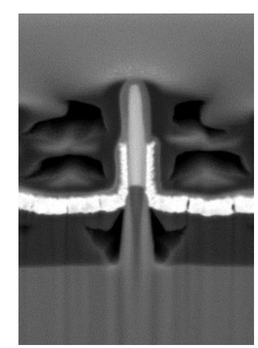




Materials



Novel Device Concepts



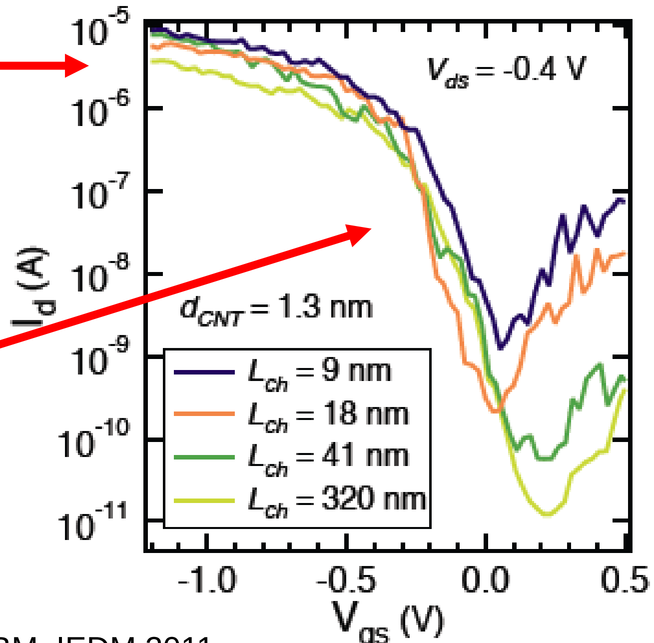
Sub-10nm CNT FET

CNT devices with scaled channel length are fabricated on one CNT

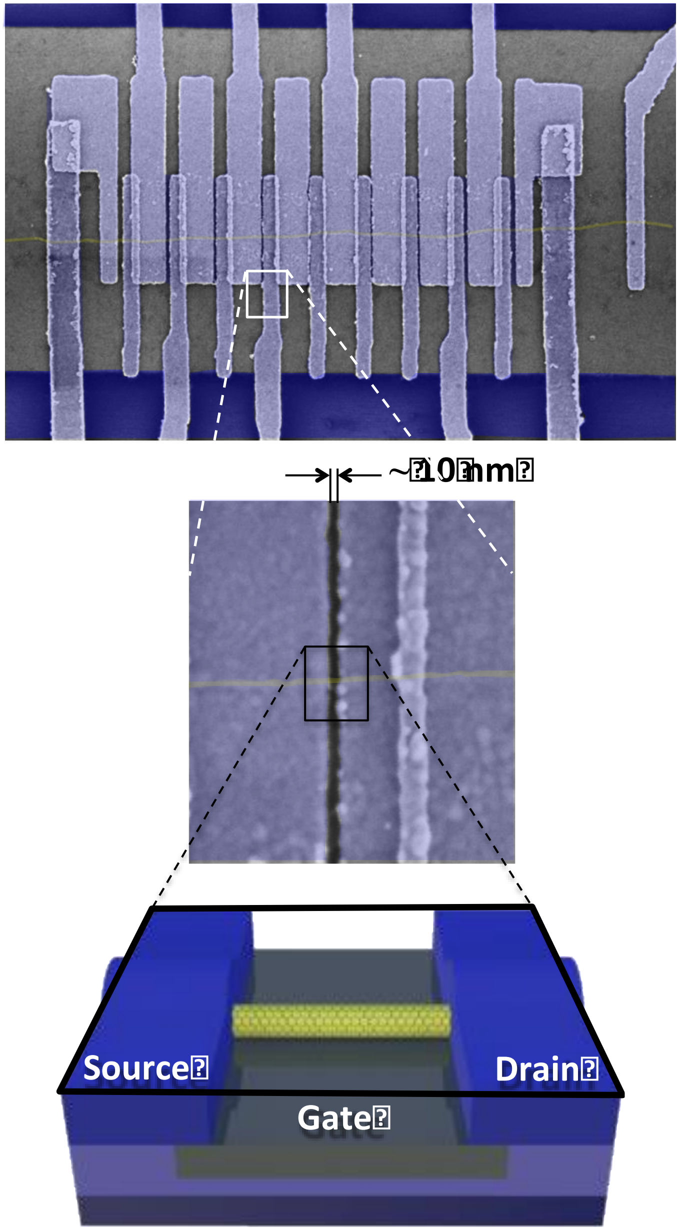
- Channel length was scaled: 320 nm to 9 nm
- First demo of sub-10 nm channel CNT FET
- Minimal short channel effects into the sub-10nm channel length region

Increasing I_{on}

Consistent Subthreshold Slope (94 mV/dec)



A. Franklin, IBM, IEDM 2011.



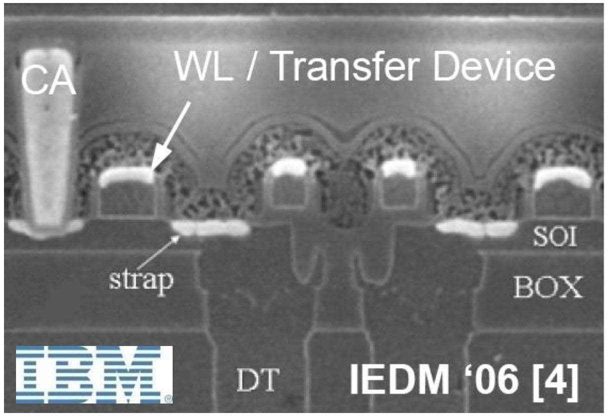
The Third Dimension

Despite all innovative materials/structures CMOS scaling looses benefits

- ***Large chips => long wires***
- ***Cache memory size limited => access time critical for performance***
- ***Power-Management, -Delivery, -Distribution, -Dissipation***
- ***I/O => Bandwidth, latency, on-chip integration***

  - **Let‘s enter the 3rd dimension**

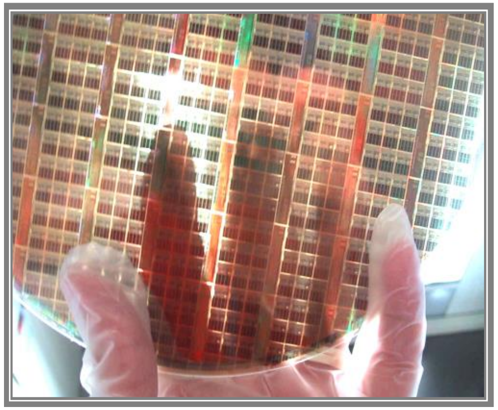
Embedded DRAM on SOI, 2006



3D Chip Integration

Benefits

- ***Density***
- ***Memory access time***
- ***Performance (Bandwidth, Latency)***
- ***Heterogeneous components***

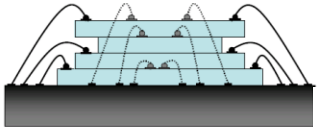


Challenges

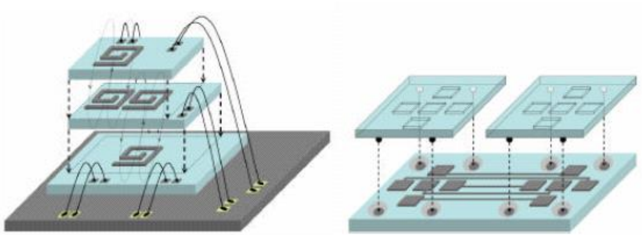
- ***Process***
- ***3D Design / EDA Tools***
- ***Heat Dissipation, Hotspots***
- ***Test***
- ***Yield / Reliablity***

3D Interconnect schemes

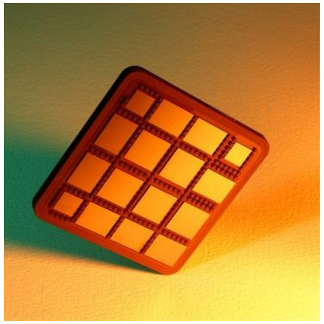
- *Wire Bonding*



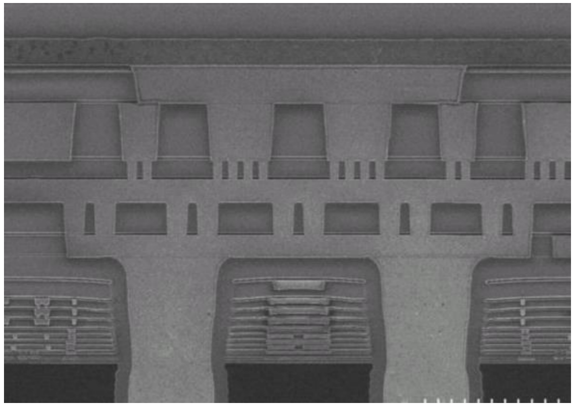
- *Coupled virtual connections (capacitive, inductive)*



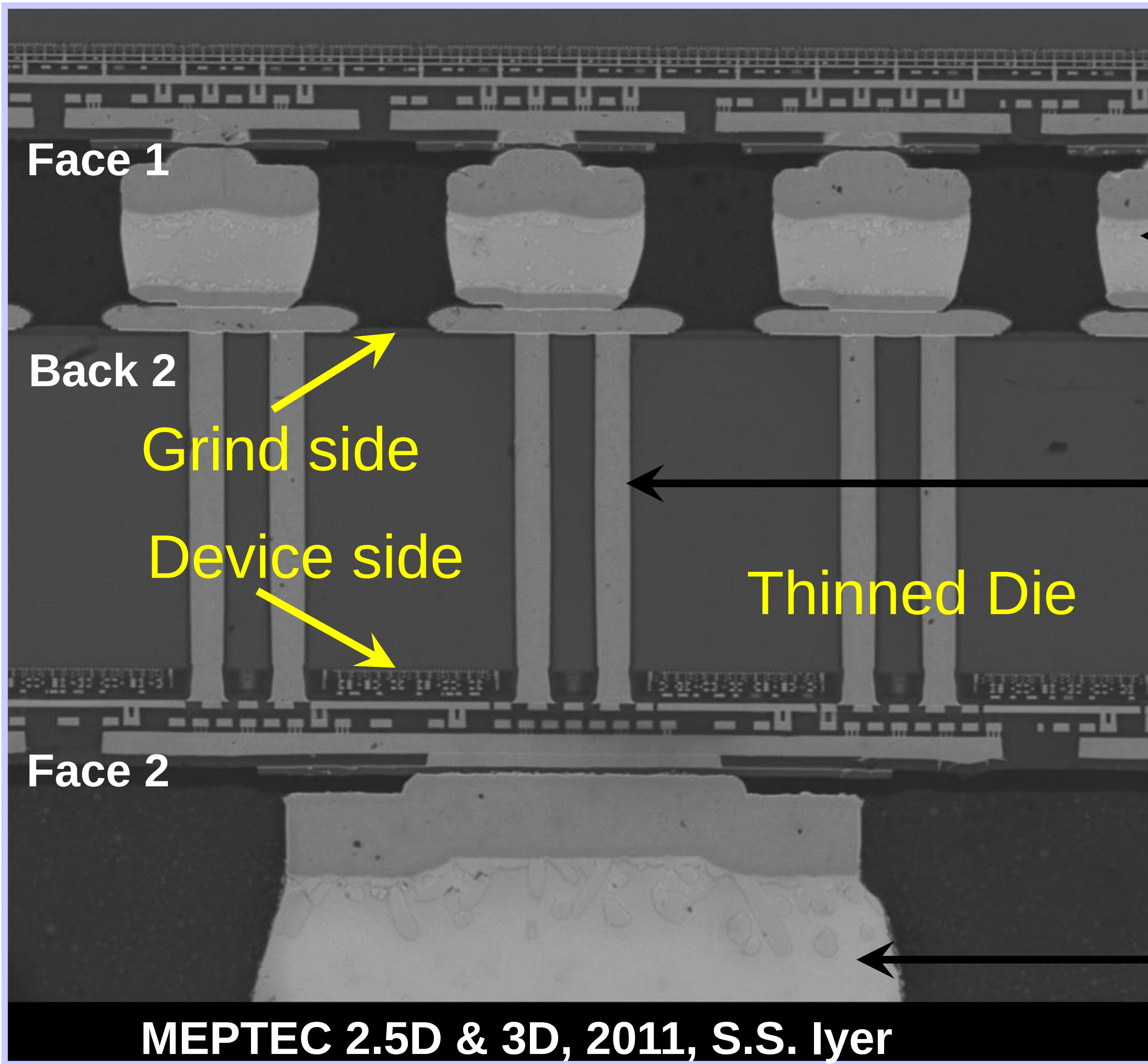
- *Microbump (C4)*



- *Through Silicon Vias (TSV)*

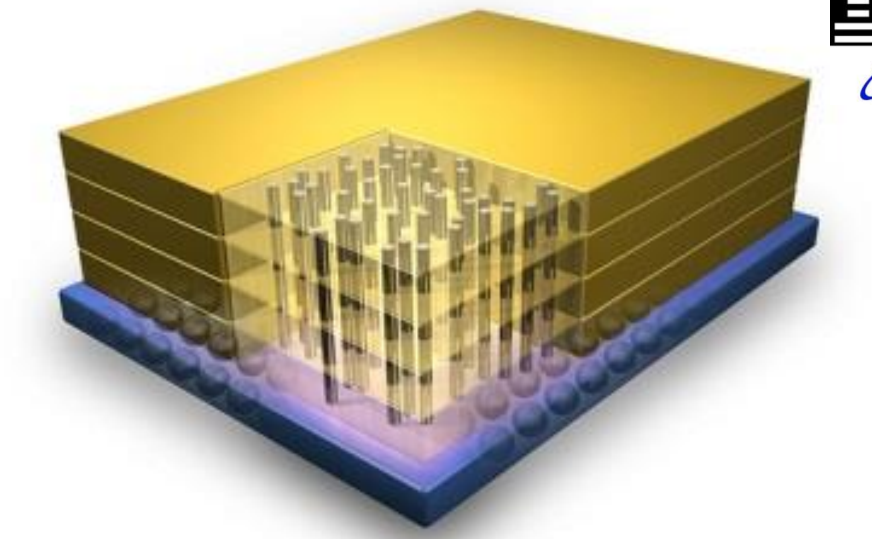


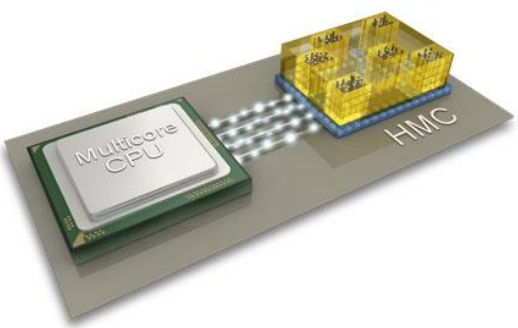
Close up of 45 nm 3D module (Face to Back)

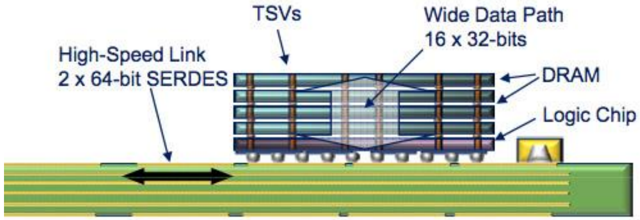


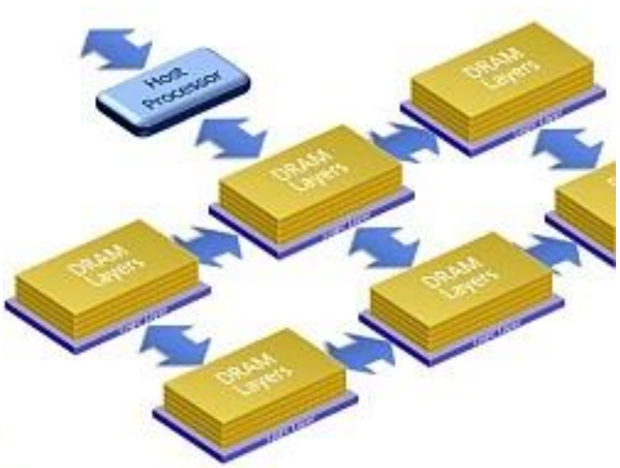
Hybrid Memory Cube

Hybrid Memory Cube
CONSORTIUM

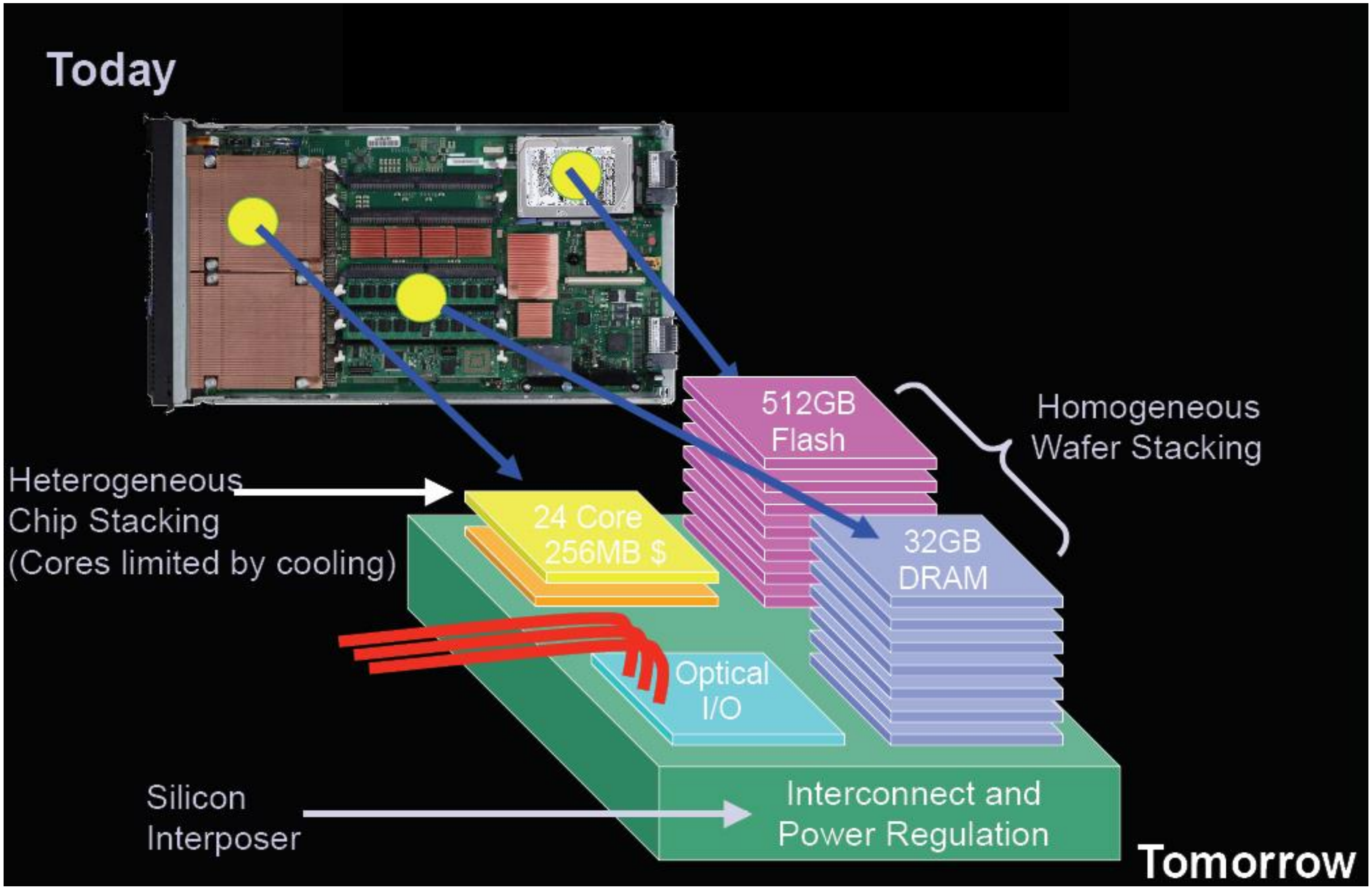








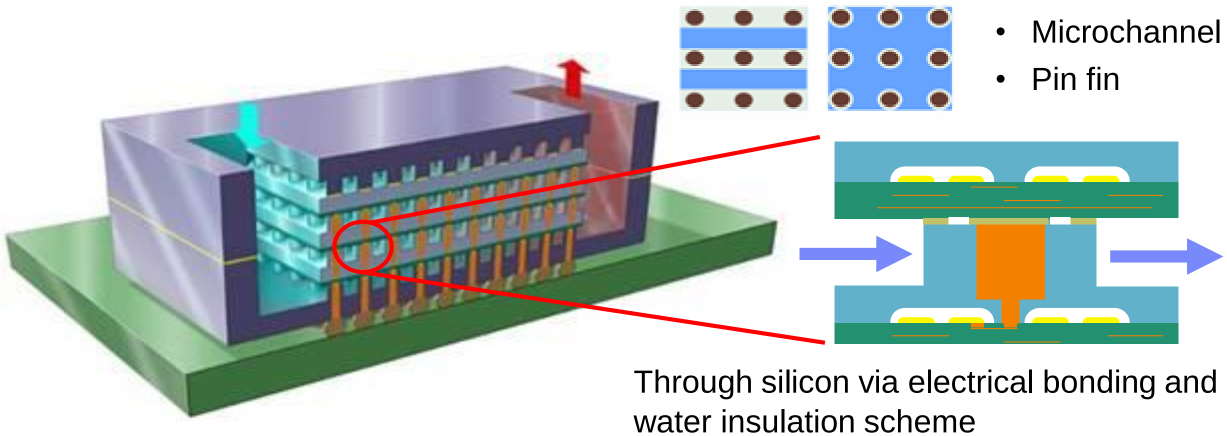
System on Silicon Interposer



Barth et al, SRC 2011

3D-chips cooled with interlayer liquid cooling

A look inside a 3D-chip stack

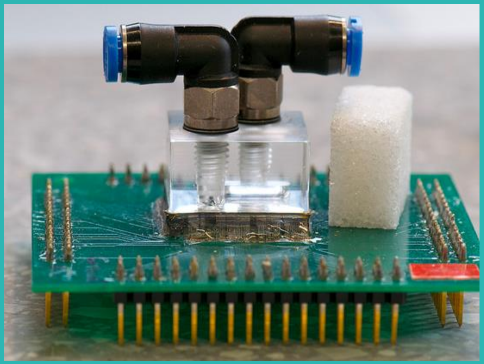


Through silicon via electrical bonding and water insulation scheme

B. Michel et al, CeBIT 2011

Exploit 3D to full extent => System in a Cube...

cross-section through fluid port and cavities



Test vehicle with fluid manifold and connection

Vielen Dank

Thank You

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