



IBM Systems and Technology Group

Silicon Technology Outlook



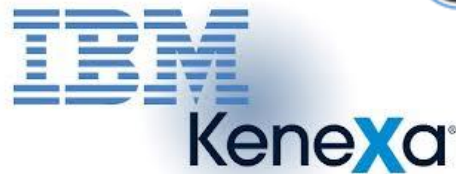
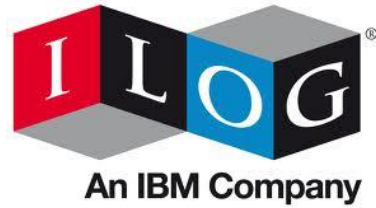
Dieter Wendel
Distinguished Engineer
IBM Deutschland Research & Development
wendel@de.ibm.com

IBM Deutschland Research & Development GmbH

Agenda

- Intro
- CMOS Scaling
- Lithography
- Device innovations
- The third dimension

IBM Technologies.....

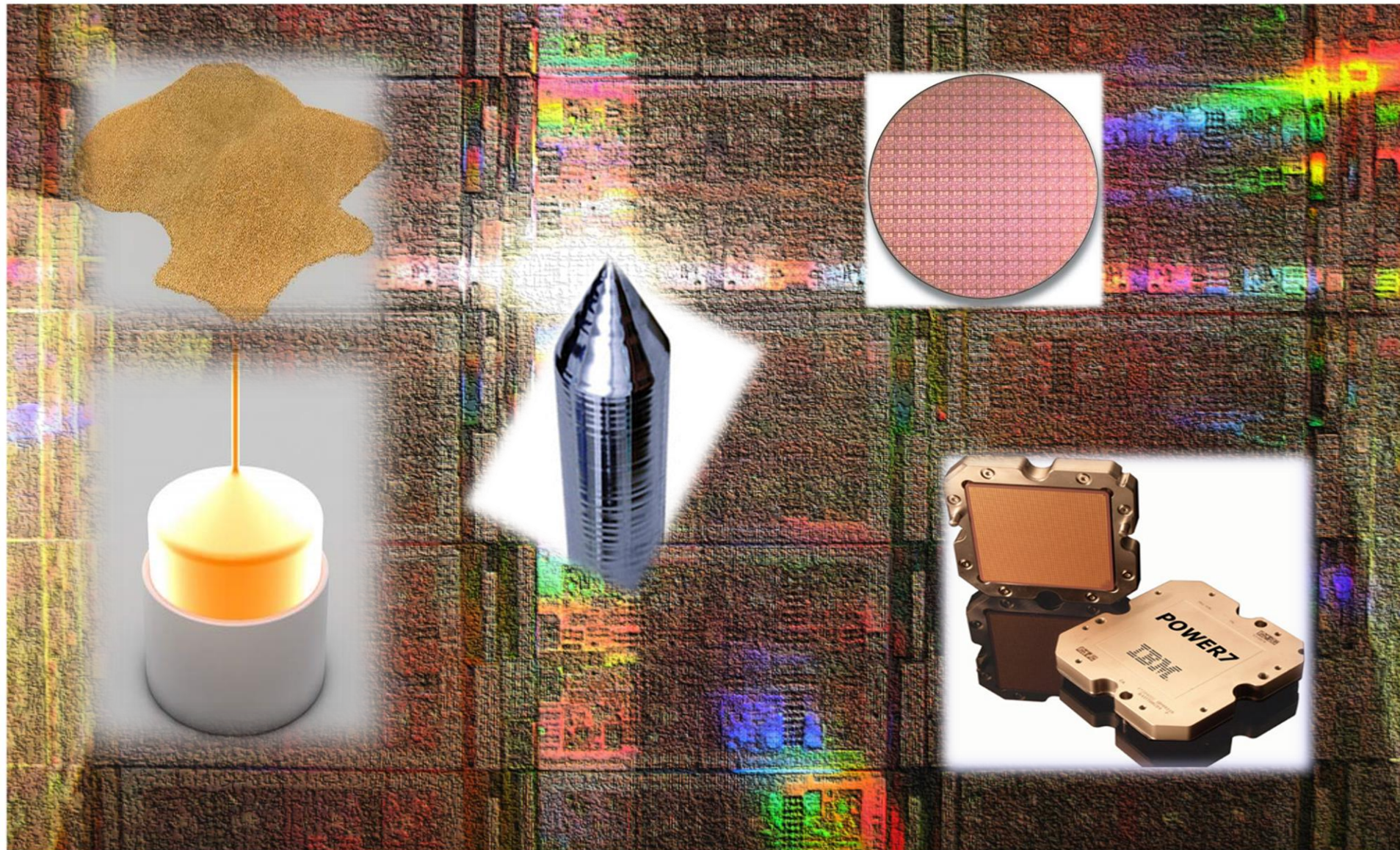


IBM zEnterprise Systems

All build on sand



Fortunately we know how do turn sand into hardware



PERIODIC TABLE OF THE ELEMENTS

1	1 IA	2%	2	IIA	3	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	VIIIA														
1	1	H	2	He																			2	He												
2	3	Li	4	Be																			5	B	6	C	7	N	8	O	9	F	10	Ne		
3	11	Na	12	Mg																			13	Al	14	Si	15	P	16	S	17	Cl	18	Ar		
4	19	K	20	Ca	21	Sc	22	Ti	23	V	24	Cr	25	Mn	26	Fe	27	Co	28	Ni	29	Cu	30	Zn	31	Ga	32	Ge	33	As	34	Se	35	Br	36	Kr
5	37	Rb	38	Sr	39	Y	40	Zr	41	Nb	42	Mo	43	Tc	44	Ru	45	Rh	46	Pd	47	Ag	48	Cd	49	In	50	Sn	51	Sb	52	Te	53	I	54	Xe
6	55	Cs	56	Ba	57-80	Lanthanide	81	Hf	82	Ta	83	W	84	Re	85	Os	86	Ir	87	Pt	88	Au	89	Hg	90	Tl	91	Pb	92	Bi	93	Po	94	At	95	Rn
7	87	Fr	88	Ra	89-103	Actinide	104	Rf	105	Db	106	Sg	107	Bh	108	Hs	109	Mt	110	Uun	111	Uuu	112	Uub	113	Uut	114	Uuq	115	Uup	116	Uuh	117	Uus	118	Uuo

Interesting fact: Top 8 elements make up ~ 98.5% of earth's crust

14 ← Group IUPAC
IVA ← Group CAS

Atomic Number → 6
Symbol → C
Name → Carbon
Electron Configuration → 2-4

Selected Oxidation States → -4, -2, +2, +4
Atomic Mass → 12.011

Electron Shells

1	K	2	S	P	D	F
2	L	8	2	6		
3	M	18	2	6	10	
4	N	32	2	6	10	14
5	O	32	2	6	10	14
6	P	18	2	6	10	
7	Q	8	2	6		
8	R	2	2			

Lanthanide

57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
Lanthanum	Cerium	Praseodymium	Neodymium	Promethium	Samarium	Europium	Gadolinium	Terbium	Dysprosium	Holmium	Erbium	Thulium	Ytterbium	Lutetium
138.91	140.12	140.91	144.24	(145)	150.36	151.96	157.25	158.93	162.50	164.93	167.26	168.93	173.04	174.97
2-8-18-18-9-2	2-8-18-20-8-2	2-8-18-21-8-2	2-8-18-22-8-2	2-8-18-23-8-2	2-8-18-24-8-2	2-8-18-25-8-2	2-8-18-25-9-2	2-8-18-27-8-2	2-8-18-28-8-2	2-8-18-29-8-2	2-8-18-30-8-2	2-8-18-31-8-2	2-8-18-32-8-2	2-8-18-32-9-2

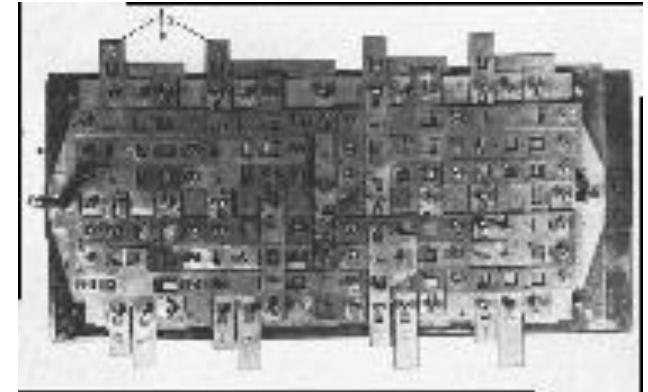
Actinide

89	90	91	92	93	94	95	96	97	98	99	100	101	102	103
Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr
Actinium	Thorium	Protactinium	Uranium	Neptunium	Plutonium	Americium	Curium	Berkelium	Californium	Einsteinium	Fermium	Mendelevium	Nobelium	Lawrencium
(227)	232.04	231.04	238.03	(237)	(244)	(243)	(247)	(247)	(251)	(252)	(257)	(258)	(259)	(262)
-18-32-18-9-2	-18-32-18-10-2	-18-32-20-9-2	-18-32-21-9-2	-18-32-23-8-2	-18-32-24-8-2	-18-32-25-8-2	-18-32-25-9-2	-18-32-27-8-2	-18-32-28-8-2	-18-32-29-8-2	-18-32-30-8-2	-18-32-31-8-2	-18-32-32-8-2	-18-32-32-9-2

It started different

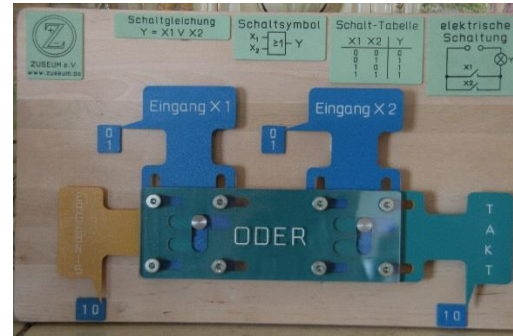
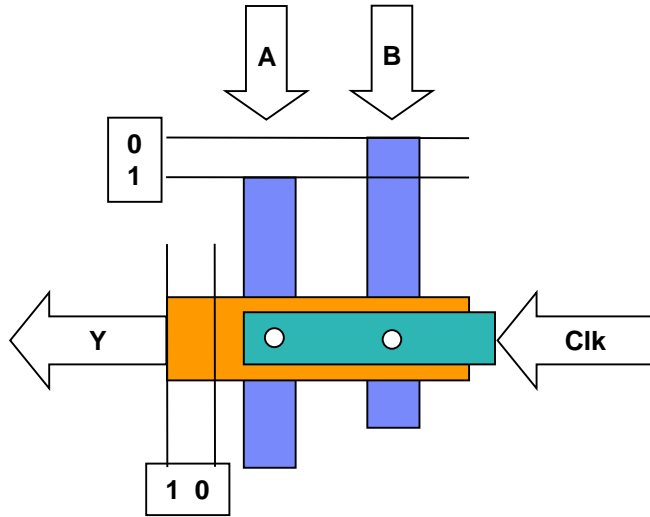
Konrad Zuse Z1

- First freely programmable computer using
 - Boolean logic
 - Binary floating point
- Build between 1936-1938 during WW II in Berlin
- Contained all parts of a modern computer
 - Control unit
 - Memory
 - Micro sequences
 - Floating point unit
 - Two registers
- Technology: mechanical via metal sheets
 - Driven by manually or optinal electrical motor from a vacuum cleaner
 - Never worked flawlessly due to mechanical problems



Source: http://user.cs.tu-berlin.de/%7Ezuse/Konrad_Zuse/en/rechner_z1.html

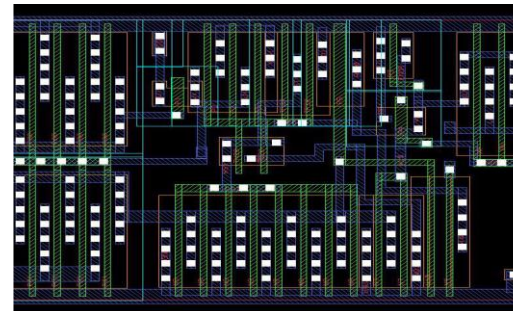
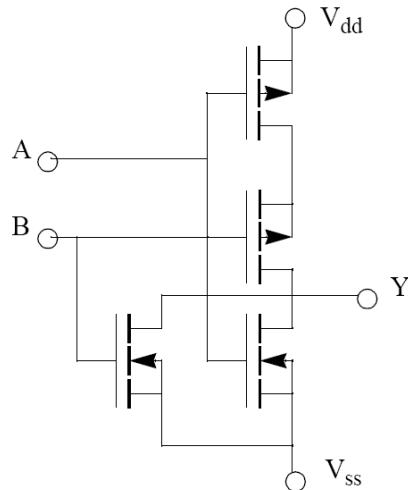
Metal sheets vs CMOS transistors:



4 metal sheets to build a logic gate

2 inputs, 1 output, 1 „clock“

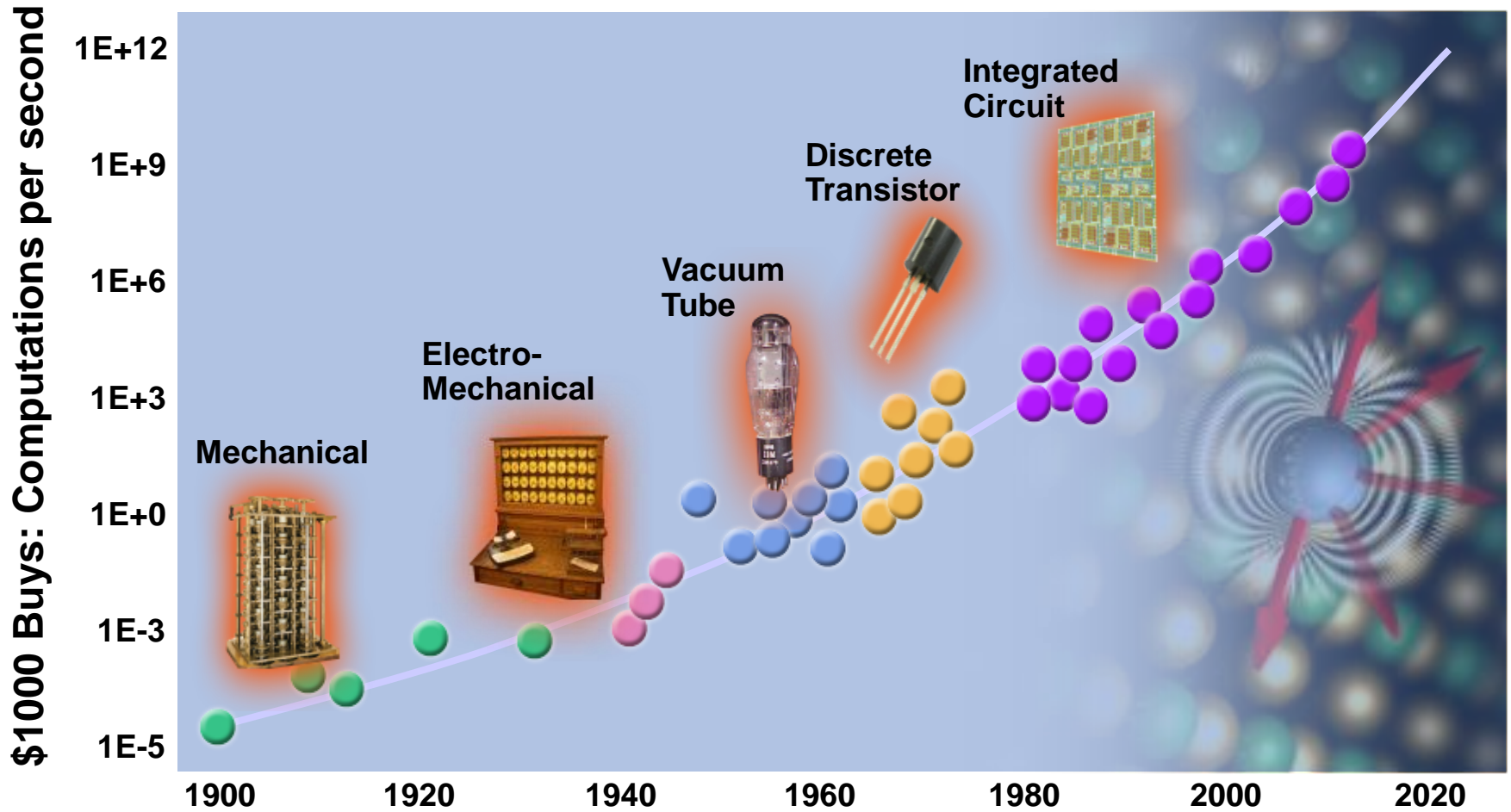
=> 30000 metal sheets represent 7500 logic gates



4 CMOS transistors per logic gate

CMOS needs two complementary pairs of CMOS transistors
Six CMOS transistors for a single memory cell

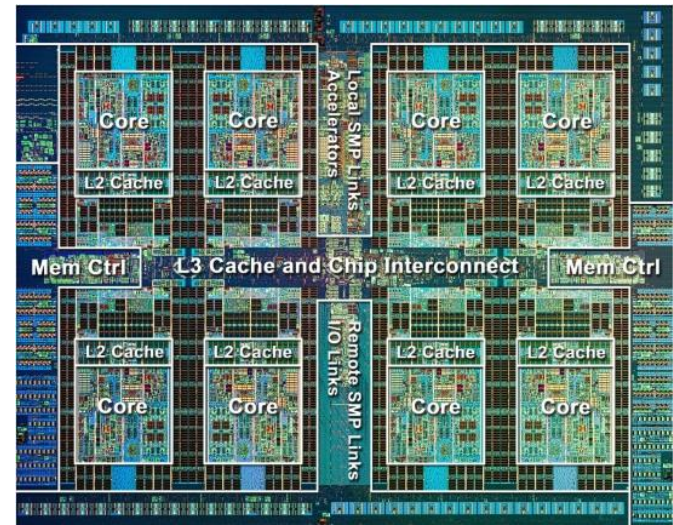
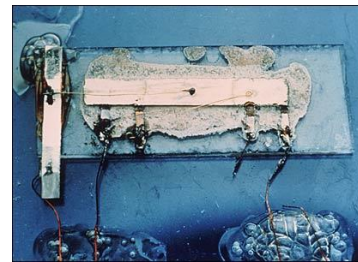
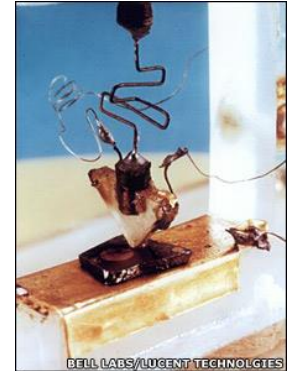
Moore's Law or What do a 1000 \$ buy?



Source: Kurzweil 1999 – Moravec 1998

CMOS Scaling

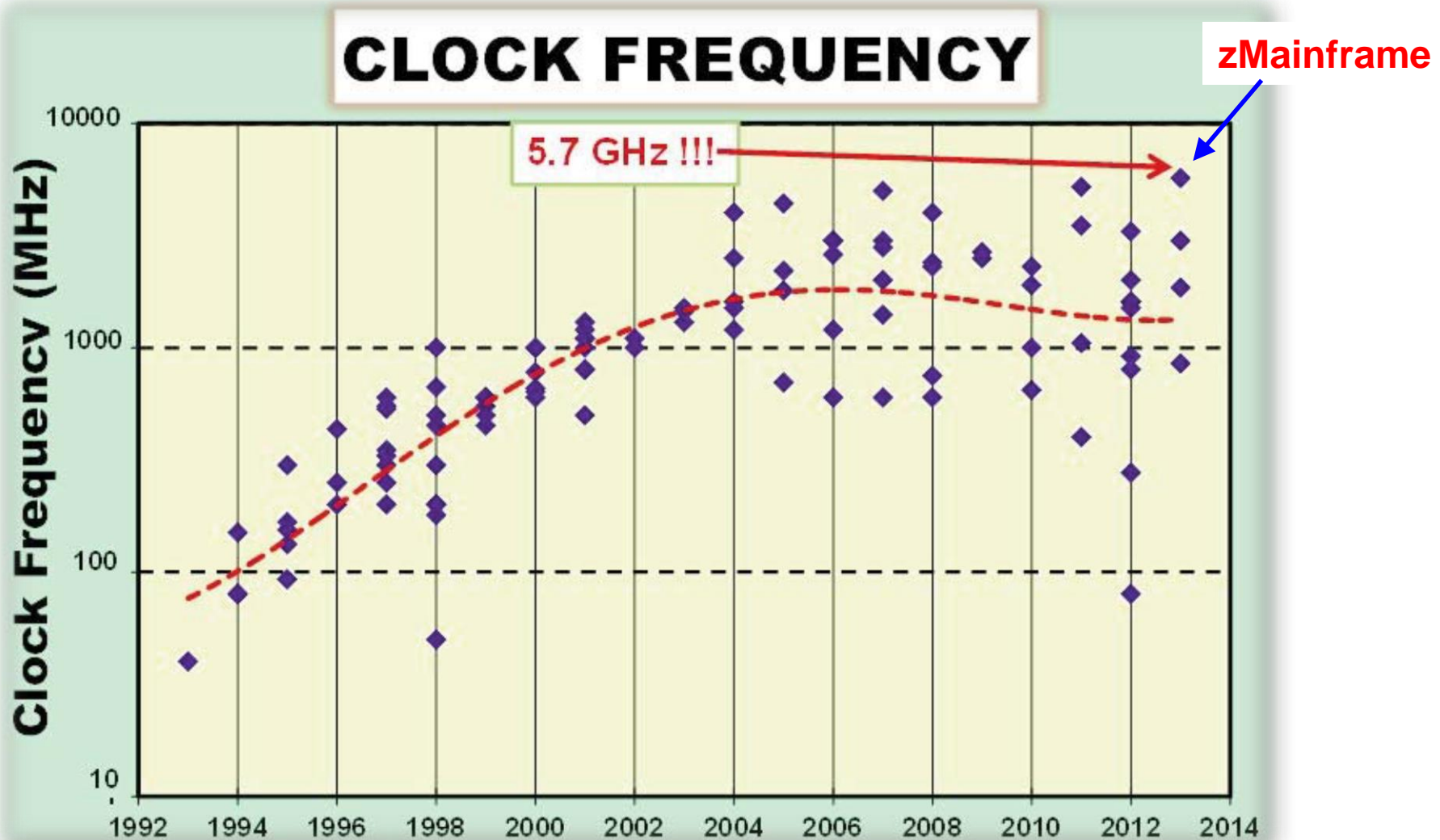
- **Transistor (1947), Bardeen, Brattain & Shockley**
- **First integrated circuit (1959), Kilby**
- **Moore's Law (1965)**
 „Cramming more components onto integrated circuits“
 Complexity of chips doubles every 24 months
 .
 .
 .
- **Cell Processor (2005)**
 234 Million Transistors in 90nm Technology
- **POWER 6 (2006)**
 790 Million Transistors in 65nm Technology
 .
 .
 .
- **POWER 7+ (2012)**
 2.1 Billion Transistors in 32nm Technology



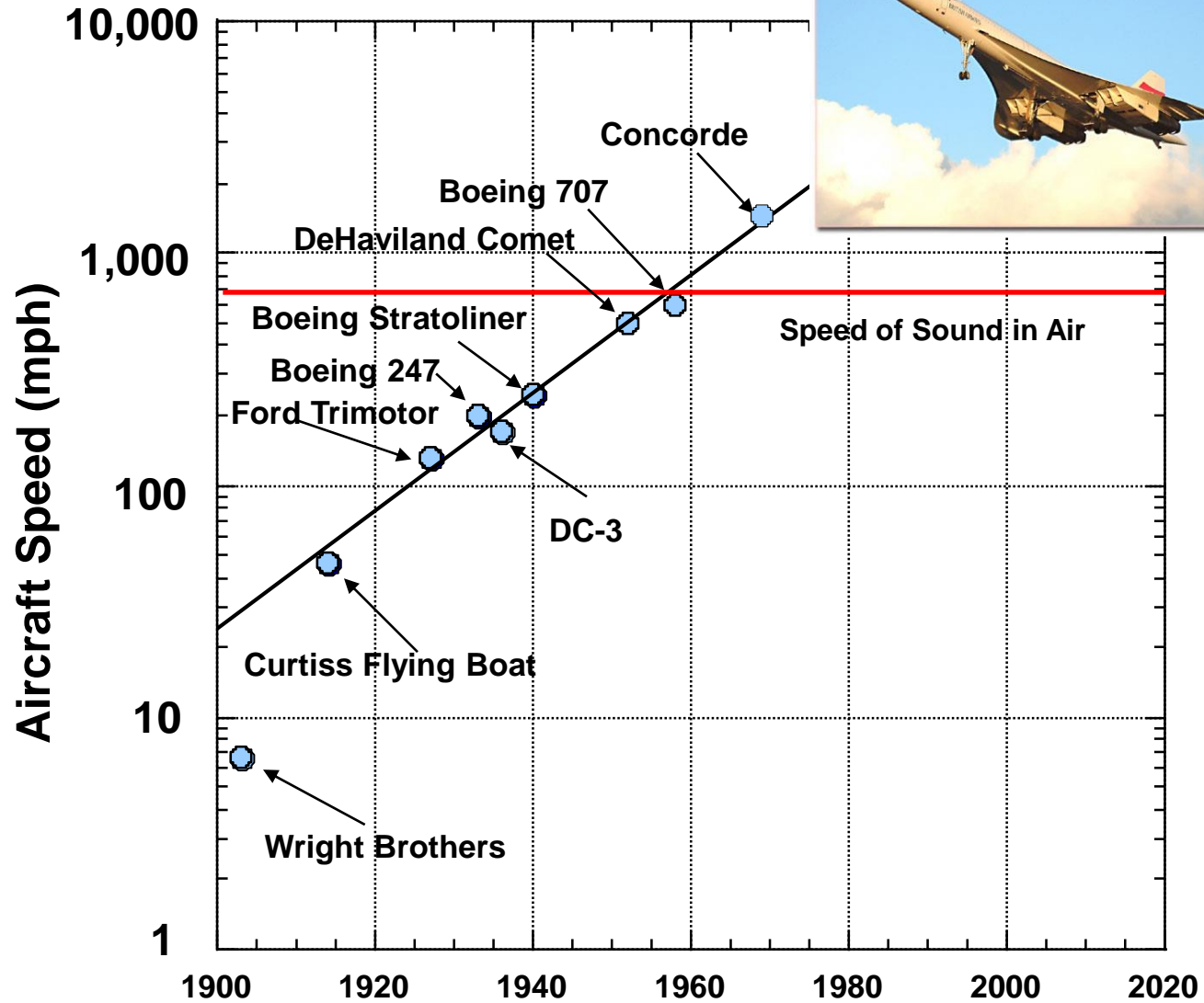
Trends Observed Across Industry (ISSCC 2013 Supplement)



Trends Observed Across Industry (ISSCC 2013 Supplement)

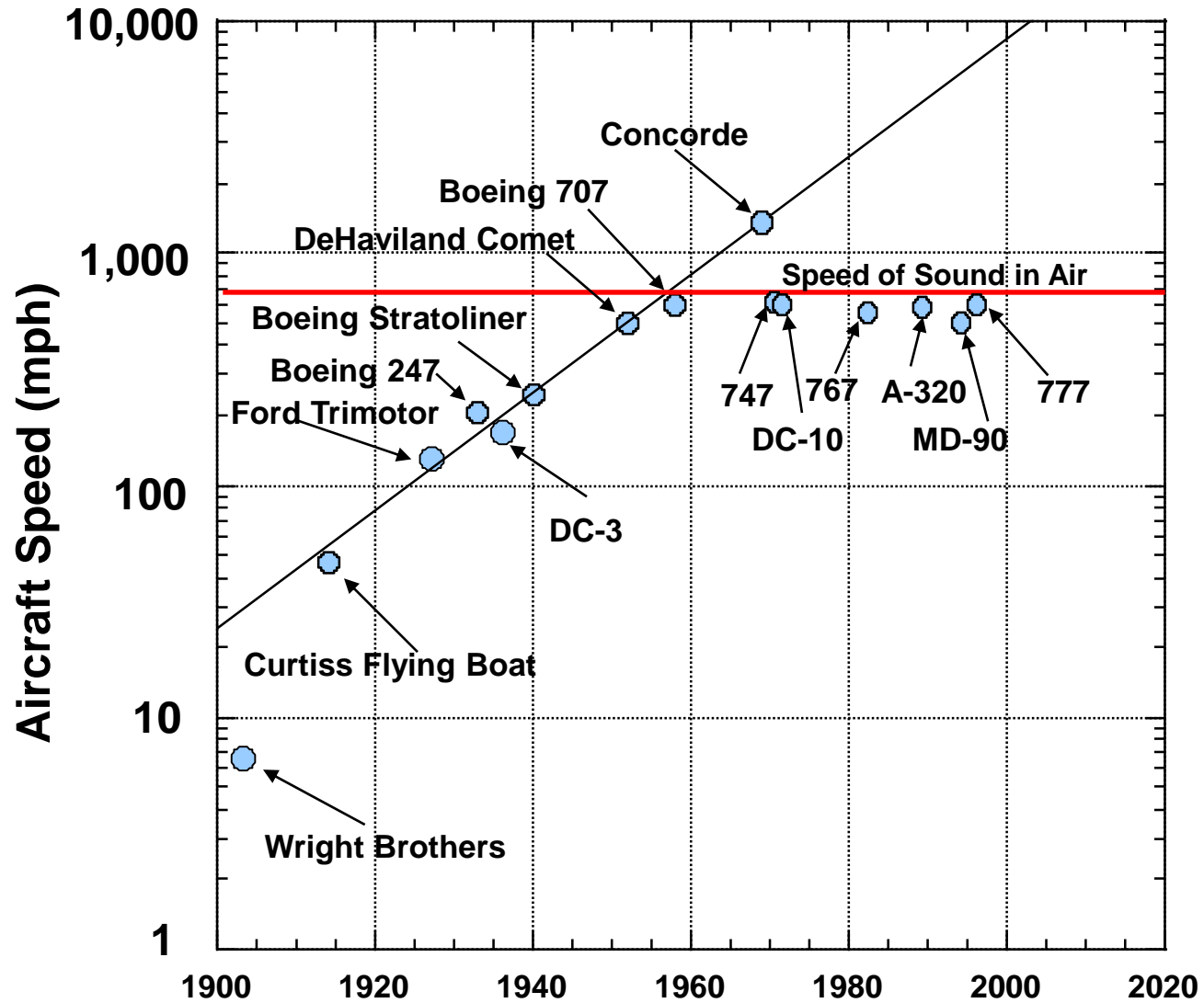


Development of Commercial Aircraft



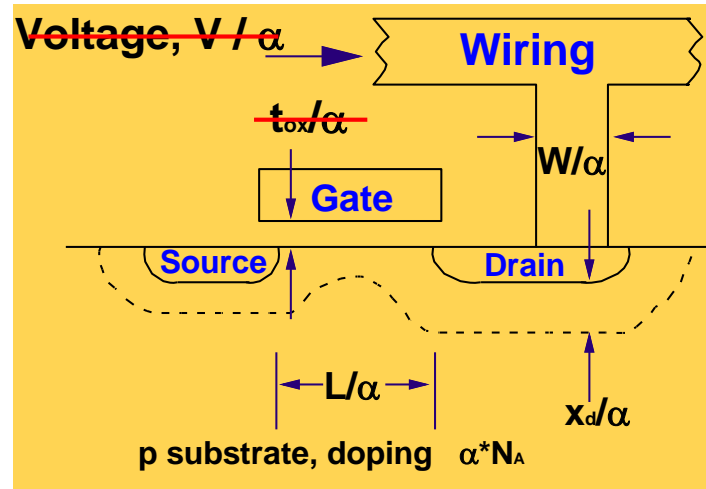
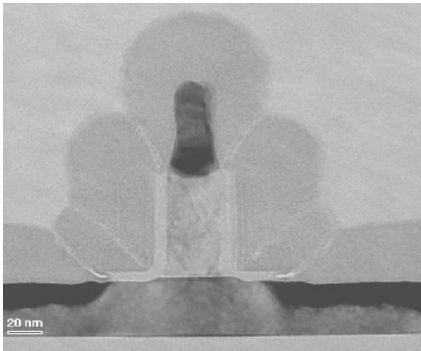
Source: F. M. Schellenberg, UCB Bodega Bay, 5-10-2007

Commercial Aviation



Source: F. M. Schellenberg, UCB Bodega Bay, 5-10-2007

Traditional CMOS Scaling (Dennard, 1974)



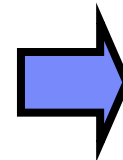
Channel Effects

- Drain Induced Barrier Lowering
- Increasing I_{off}
- V_t dependence on V_{ds}
- Sub-threshold slope

< 65 nm

SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha \cdot N_A$



Higher Density:	$\sim \alpha^2$
Higher Speed:	$\sim \alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	Constant

Improving Performance

No longer possible by scaling alone

New Device Structures

New Device Design point

New Materials

Before 90's

Since the 90's

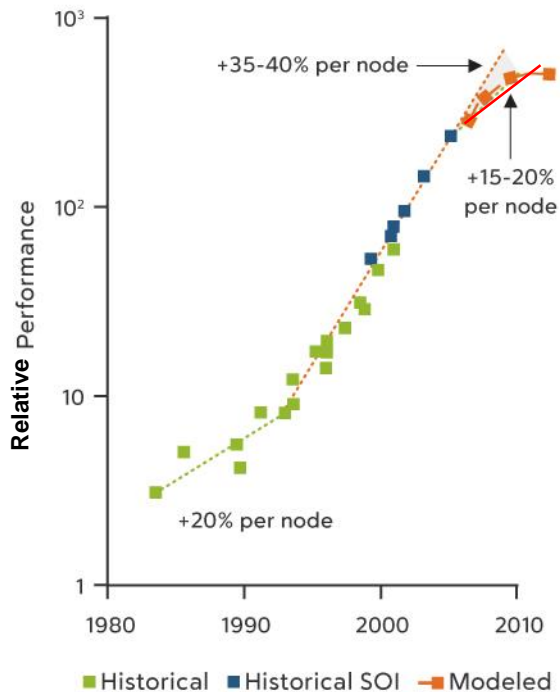
Beyond 2006

hydrogen 1 H																	helium 2 He				
lithium 3 Li 6.941	beryllium 4 Be 9.0122															boron 5 B	carbon 6 C	nitrogen 7 N	oxygen 8 O	fluorine 9 F	neon 10 Ne 20.180
sodium 11 Na 22.990	magnesium 12 Mg															aluminum 13 Al	silicon 14 Si	phosphorus 15 P	sulfur 16 S 32.065	chlorine 17 Cl	argon 18 Ar 39.948
potassium 19 K 39.098	calcium 20 Ca	scandium 21 Sc	titanium 22 Ti	vanadium 23 V	chromium 24 Cr	manganese 25 Mn 54.938	iron 26 Fe 55.845	cobalt 27 Co	nickel 28 Ni	copper 29 Cu	zinc 30 Zn	gallium 31 Ga 69.723	germanium 32 Ge	arsenic 33 As	selenium 34 Se 78.96	bromine 35 Br	krypton 36 Kr 83.80				
rubidium 37 Rb 85.468	strontium 38 Sr	yttrium 39 Y	zirconium 40 Zr	niobium 41 Nb	molybdenum 42 Mo	technetium 43 Tc [98]	ruthenium 44 Ru	rhodium 45 Rh	palladium 46 Pd	silver 47 Ag 107.87	cadmium 48 Cd 112.41	indium 49 In 114.82	tin 50 Sn 118.71	antimony 51 Sb 121.76	tellurium 52 Te 127.60	iodine 53 I 126.90	xenon 54 Xe 131.29				
caesium 55 Cs 132.91	barium 56 Ba	57-70 *	lutetium 71 Lu 174.97	hafnium 72 Hf	tantalum 73 Ta	tungsten 74 W	rhenium 75 Re 186.21	osmium 76 Os 190.23	iridium 77 Ir	platinum 78 Pt 195.08	gold 79 Au 196.97	mercury 80 Hg 200.59	thallium 81 Tl 204.38	lead 82 Pb 207.2	bismuth 83 Bi 208.98	polonium 84 Po [209]	astatine 85 At [210]	radon 86 Rn [222]			
francium 87 Fr [223]	radium 88 Ra [226]	89-102 **	lanthanum 57 La [138.905]	rutherfordium 104 Rf [261]	dubnium 105 Db [262]	seaborgium 106 Sg [266]	bohrium 107 Bh [269]	hassium 108 Hs [269]	meitnerium 109 Mt [268]	ununnium 110 Uun [271]	ununium 111 Uuu [272]	ununbium 112 Uub [277]	ununquadium 114 Uuq [289]								
			lanthanum 57 La	cerium 58 Ce	Praseodymium 59 Pr	neodymium 60 Nd	promethium 61 Pm [145]	samarium 62 Sm	europium 63 Eu	gadolinium 64 Gd	terbium 65 Tb	dysprosium 66 Dy	holmium 67 Ho	erbium 68 Er	thulium 69 Tm	ytterbium 70 Yb					
			actinium 89 Ac [227]	thorium 90 Th 232.04	protactinium 91 Pa 231.04	uranium 92 U 238.03	neptunium 93 Np [237]	plutonium 94 Pu [244]	americium 95 Am [243]	curium 96 Cm [247]	berkelium 97 Bk [247]	californium 98 Cf [251]	einsteinium 99 Es [252]	fermium 100 Fm [257]	mendelevium 101 Md [258]	nobelium 102 No [259]					

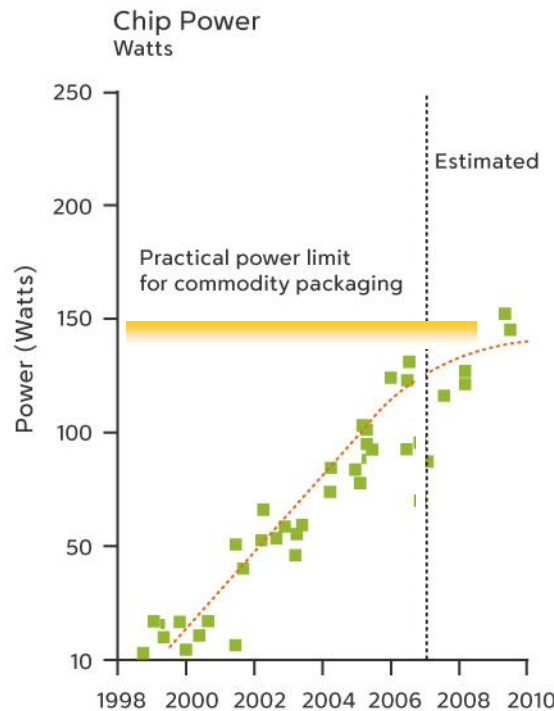
CMOS Technology Trends

Conventional CMOS scaling benefits are diminishing.

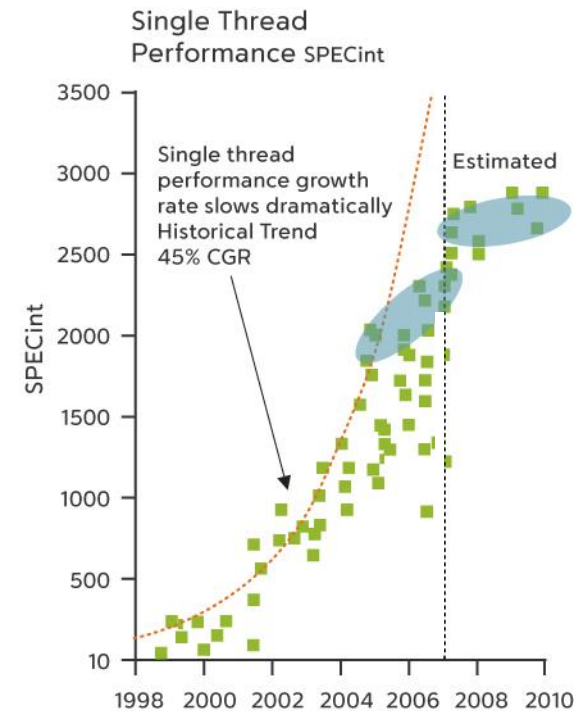
Transistor performance scaling to continue, but at a slower rate



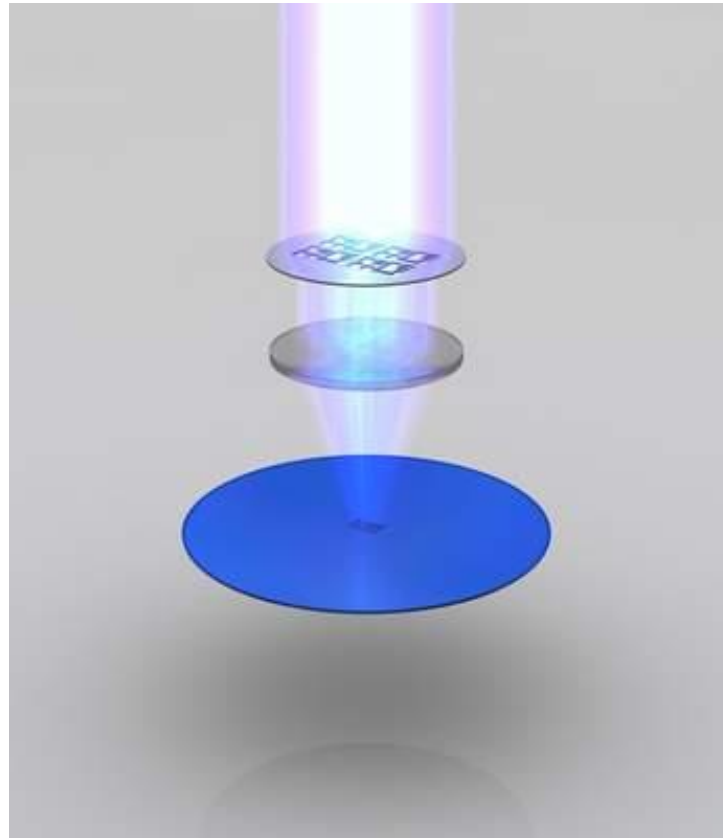
Power is limiting practical performance



Single thread performance growth is slowing dramatically

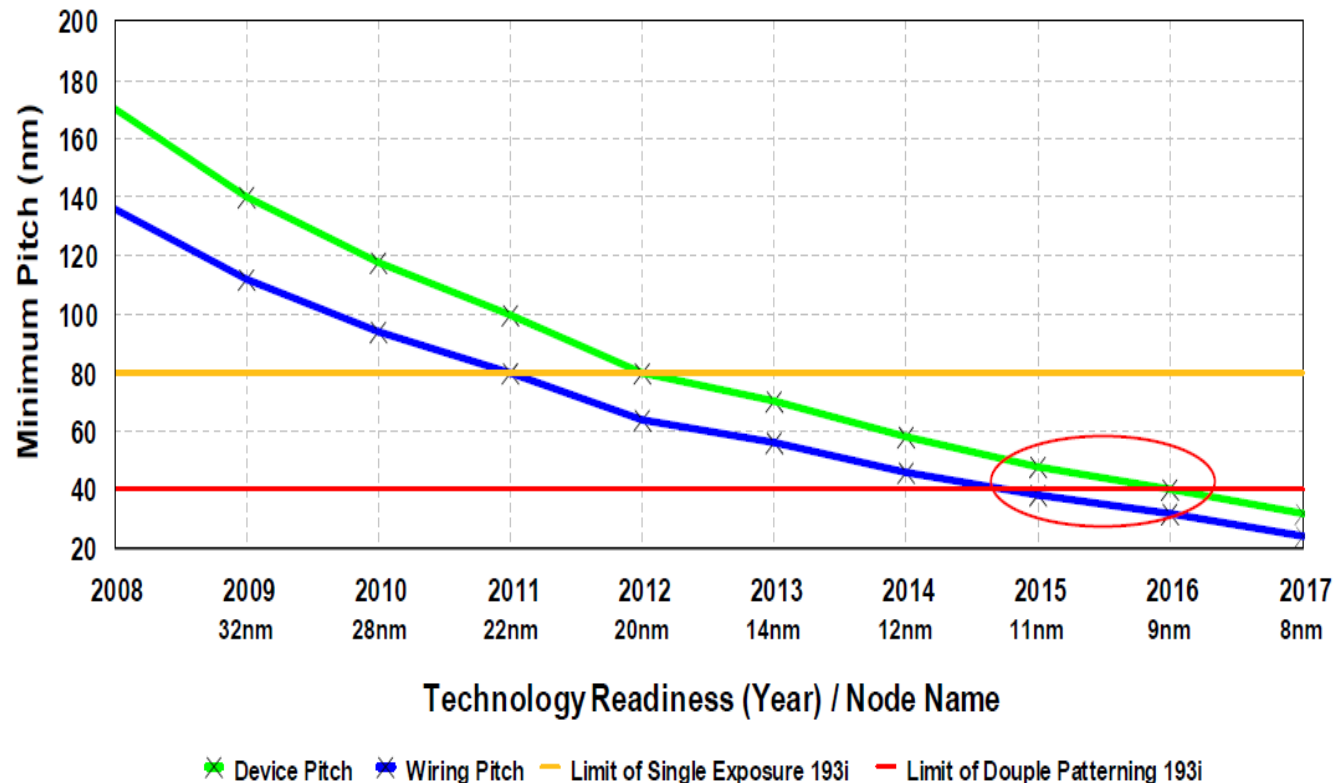


Lithography



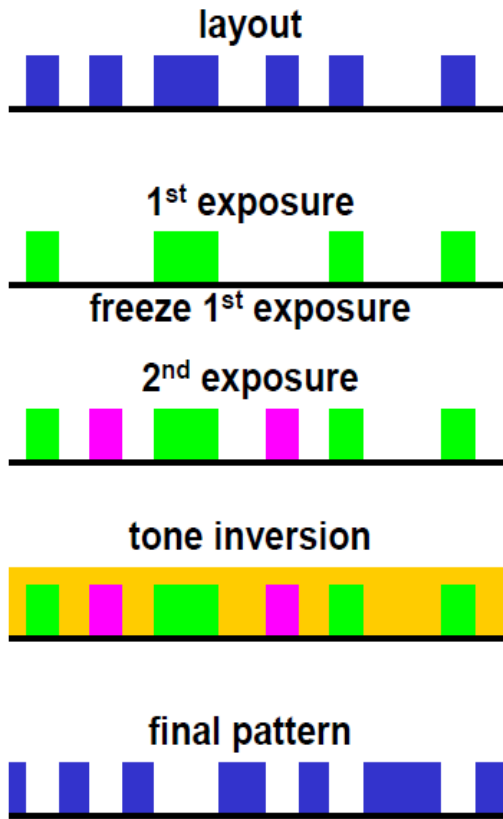
Pushing the Physical Limits of Optical Lithography

- Historically driven by lowering wavelength or increasing lens numerical aperture
- Immersion lithography with 193nm extended for five generation through 10 nm
 - double patterning, implementation of restricted design rules, etc...
- EUV offers a return to single patterning with 13.5nm wavelength
 - facing many delays in maturation (radiation source power output)
 - => EUV still carries significant risk going forward
- Targeting insertion of EUV at 7nm node
- “Invention required” past 5nm



Double pattern Variants

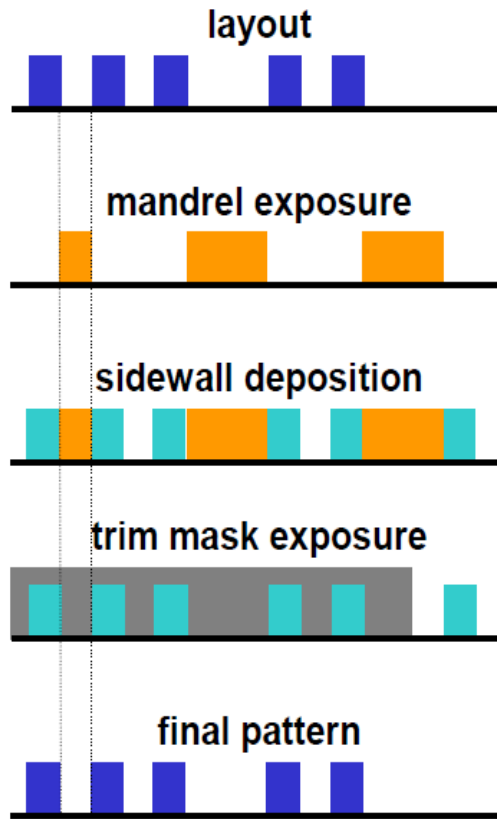
Pitch Split
(litho freeze litho etch = LFLE)



Overlay affects space, bimodal size distribution.

Useful for: local interconnect, via, wires

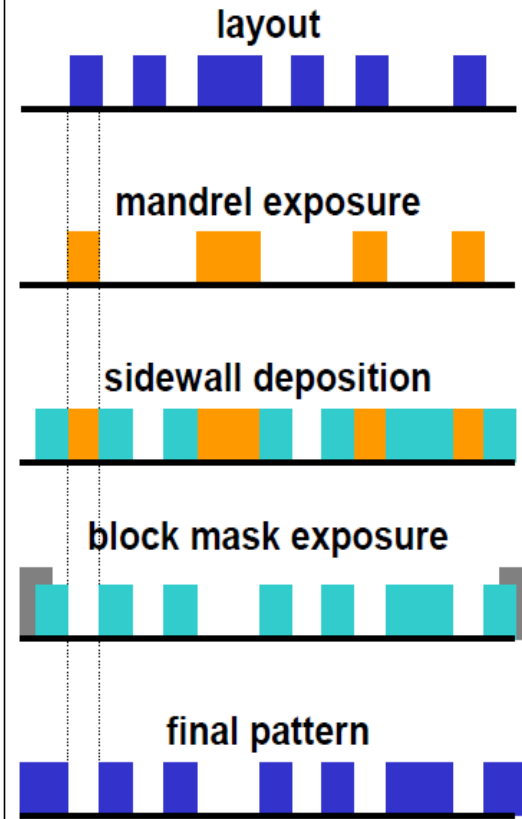
Sidewall Image Transfer
(background mode)



Fixed feature width.

Useful for: poly-gate

Sidewall Image Transfer
(foreground mode)



Discrete feature spaces, no stitching possible.

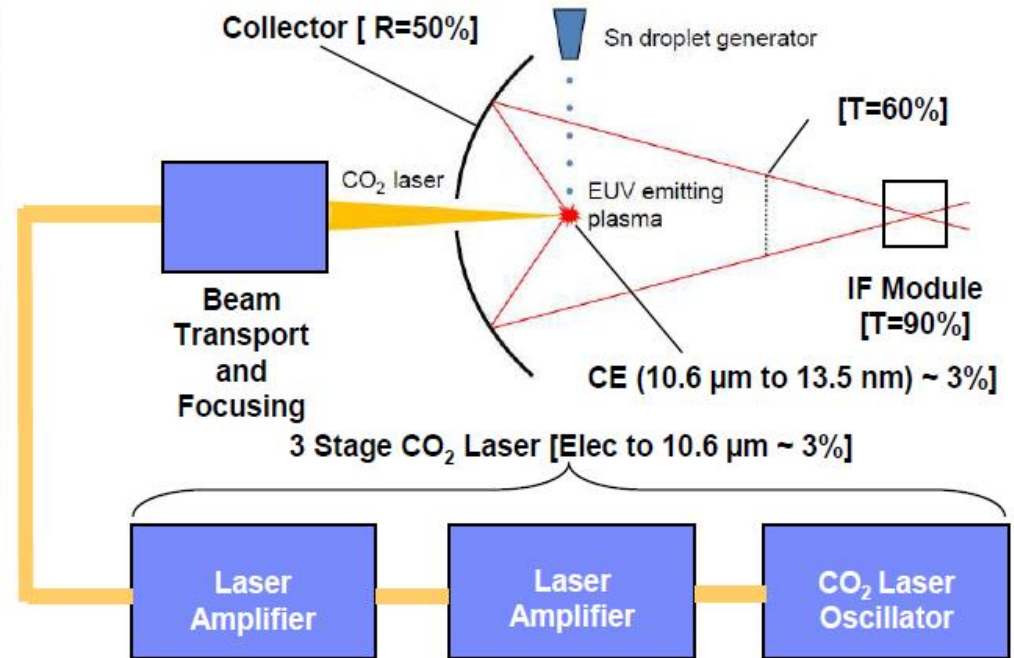
Useful for: wires

EUV: extreme ultra-violet lithography

ASML's exposure system



Cymer's EUV source

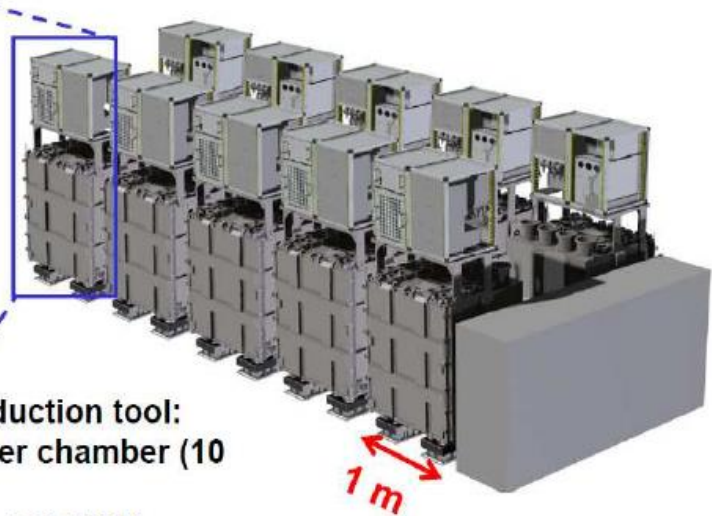
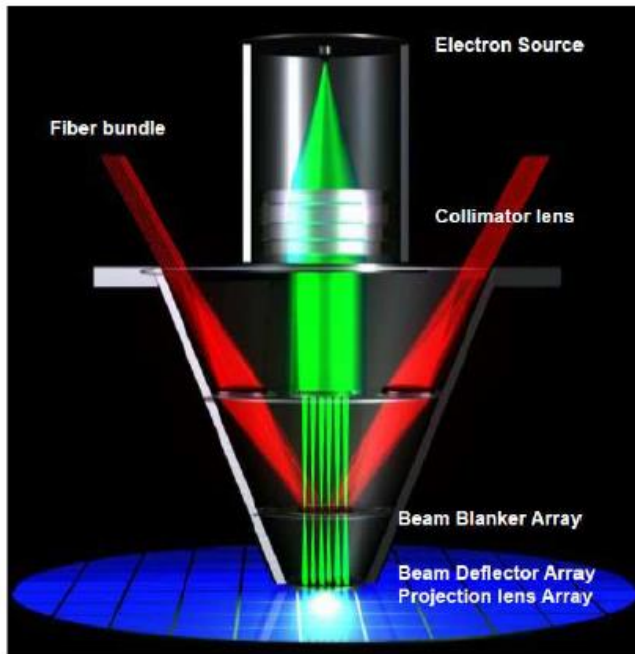


Conversion from wall plug to EUV: ~ 0.02%

Program is making steady progress.

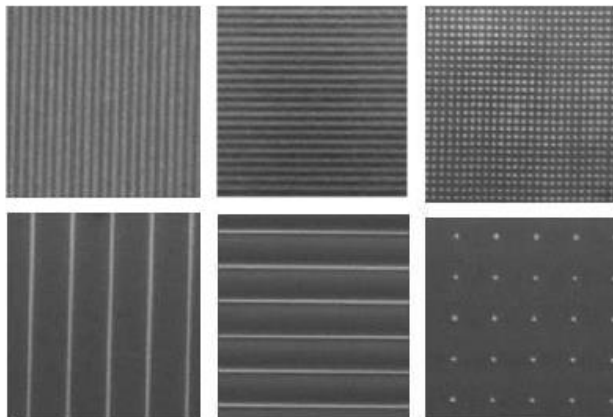
Source power, resist line-edge roughness, mask-blank defects, optics lifetime, overall system cost... remain a challenge

MAPPER: multiple e-beam mask-less lithography



HVM clustered production tool:

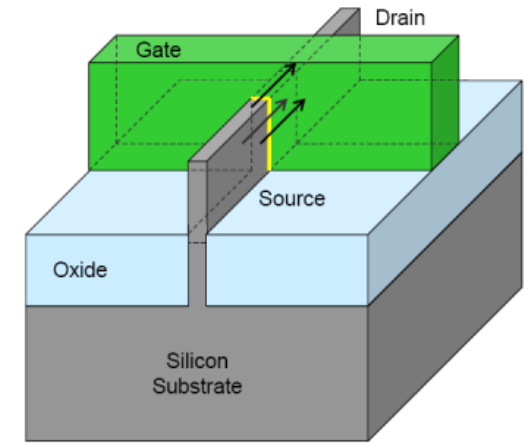
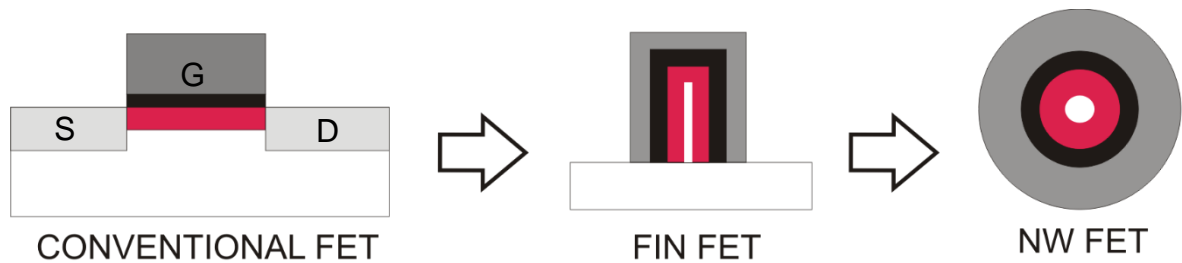
- >13,000 beams per chamber (10 WPH)
- 10 WPH x 5 x 2 = 100 WPH
- Footprint ~ArF scanner



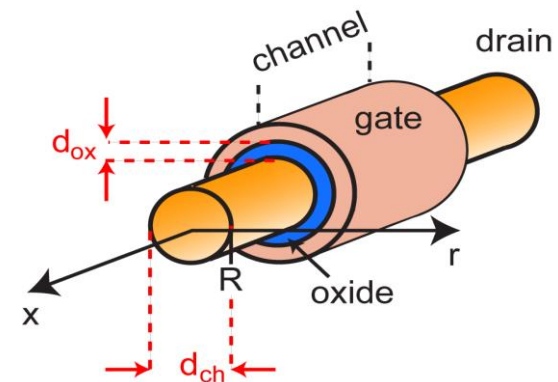
- 110 beams working
- Each beam covers a $2 \times 2 \mu\text{m}^2$ block
- Met CD mean-to-target & CDU spec

Devices innovation

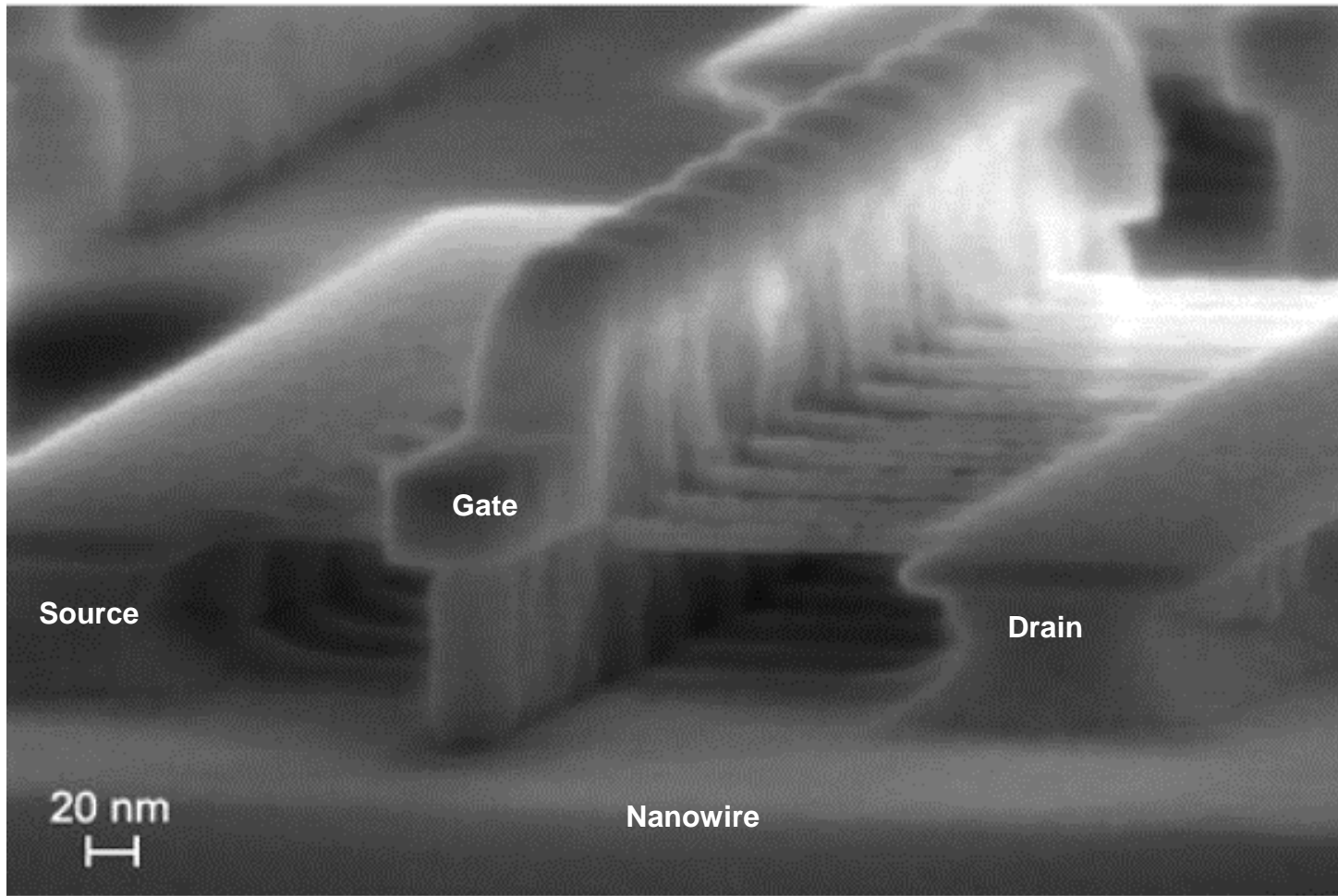
Electrostatic control of the channel depends on the gate architecture (gate control).



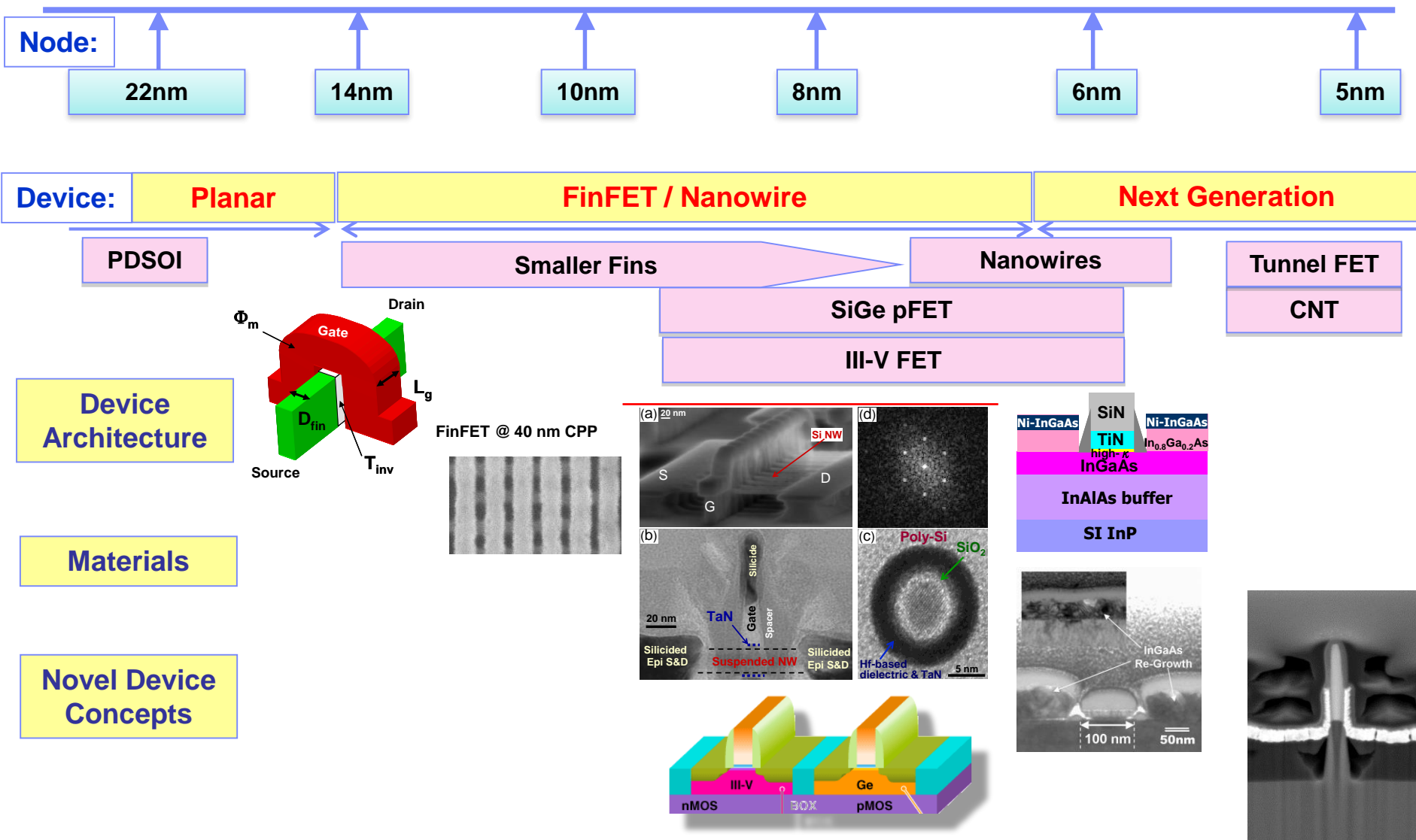
- **Nanowire offers optimum electrostatic gate control of channel**
- Improved scaling: $L_g \sim 1.5$ diameter
- Reduced leakage current/power



Silicon Nanowires, 5nm and beyond



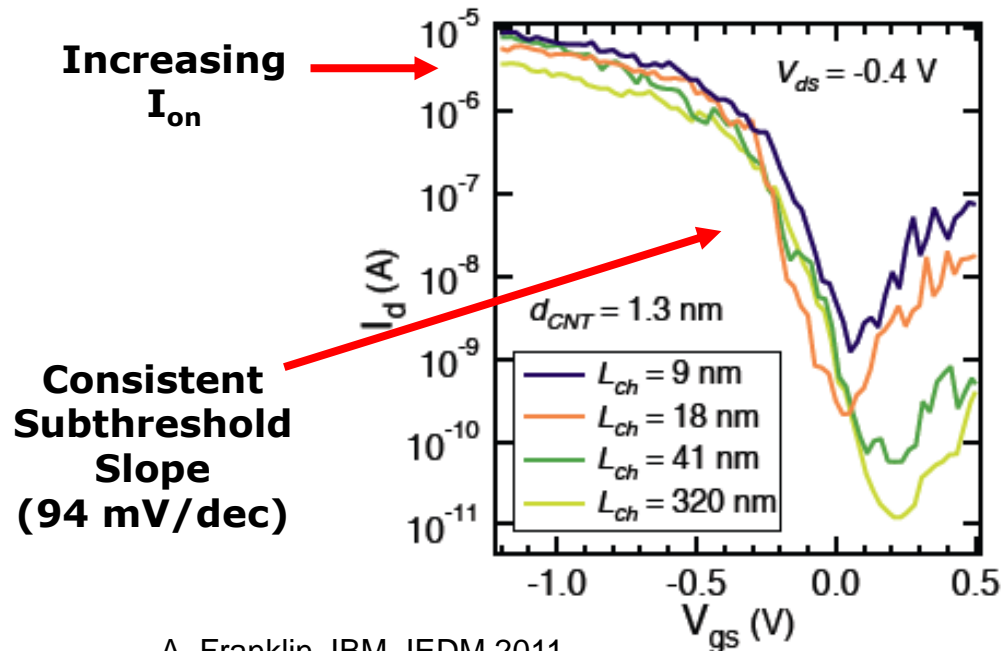
Potential device roadmap



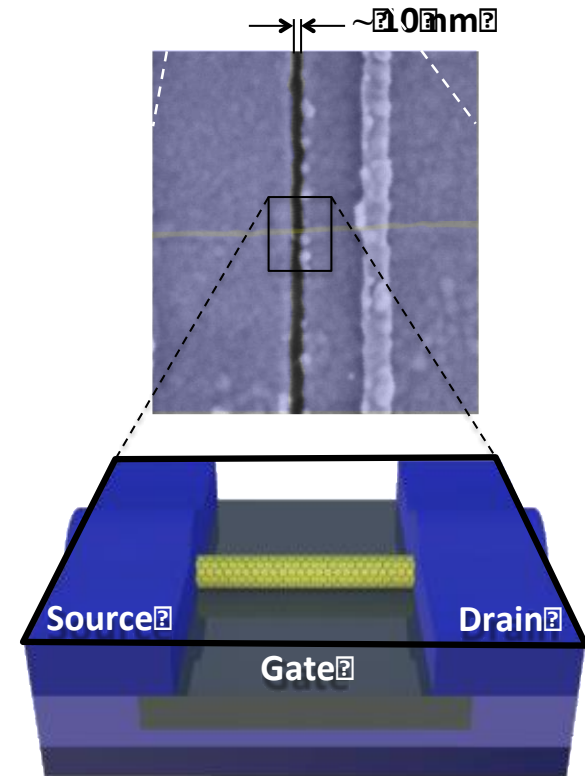
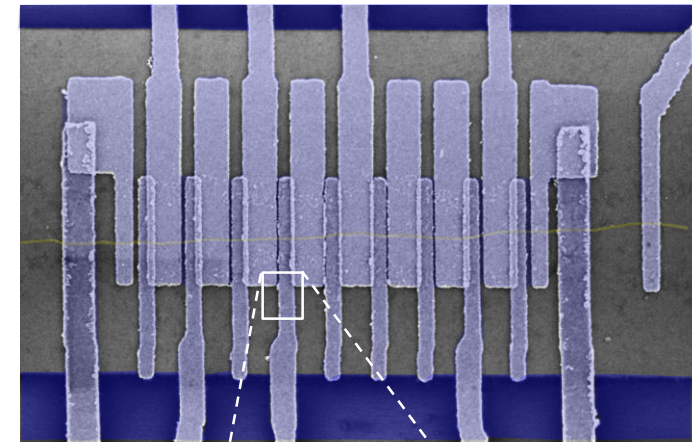
Sub-10nm CNT FET

CNT devices with scaled channel length are fabricated on one CNT

- Channel length was scaled: 320 nm to 9 nm
- First demo of sub-10 nm channel CNT FET
- Minimal short channel effects into the sub-10nm channel length region



A. Franklin, IBM, IEDM 2011.



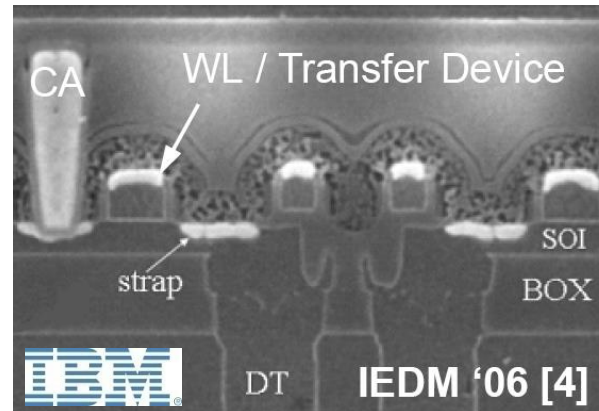
The Third Dimension

Despite all innovative materials/structures CMOS scaling loses benefits

- ***Large chips => long wires***
- ***Cache memory size limited => access time critical for performance***
- ***Power-Management, -Delivery, -Distribution, -Dissipation***
- ***I/O => Bandwidth, latency, on-chip integration***

- **Let's enter the 3rd dimension**

Embedded DRAM on SOI, 2006



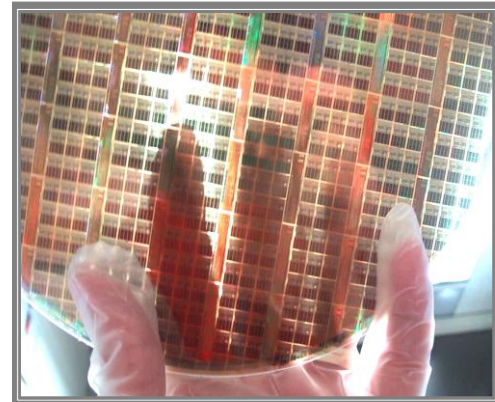
3D Chip Integration

Benefits

- *Density*
- *Memory access time*
- *Performance (Bandwidth, Latency)*
- *Heterogeneous components*

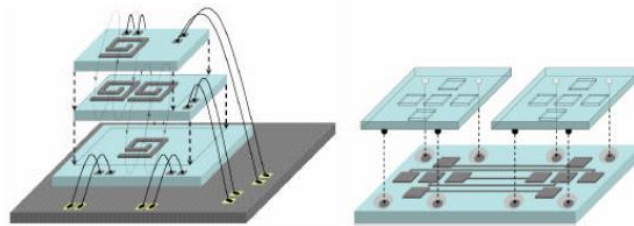
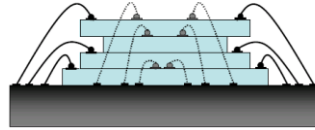
Challenges

- *Process*
- *3D Design / EDA Tools*
- *Heat Dissipation, Hotspots*
- *Test*
- *Yield / Reliability*

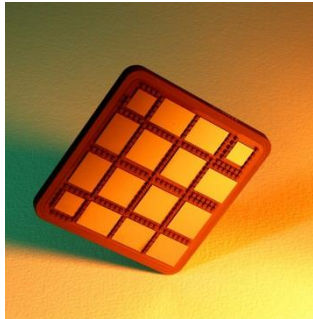


3D Interconnect schemes

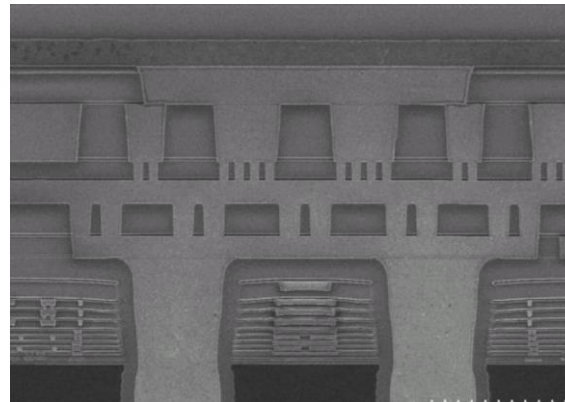
- **Wire Bonding**
- **Coupled virtual connections (capacitive, inductive)**



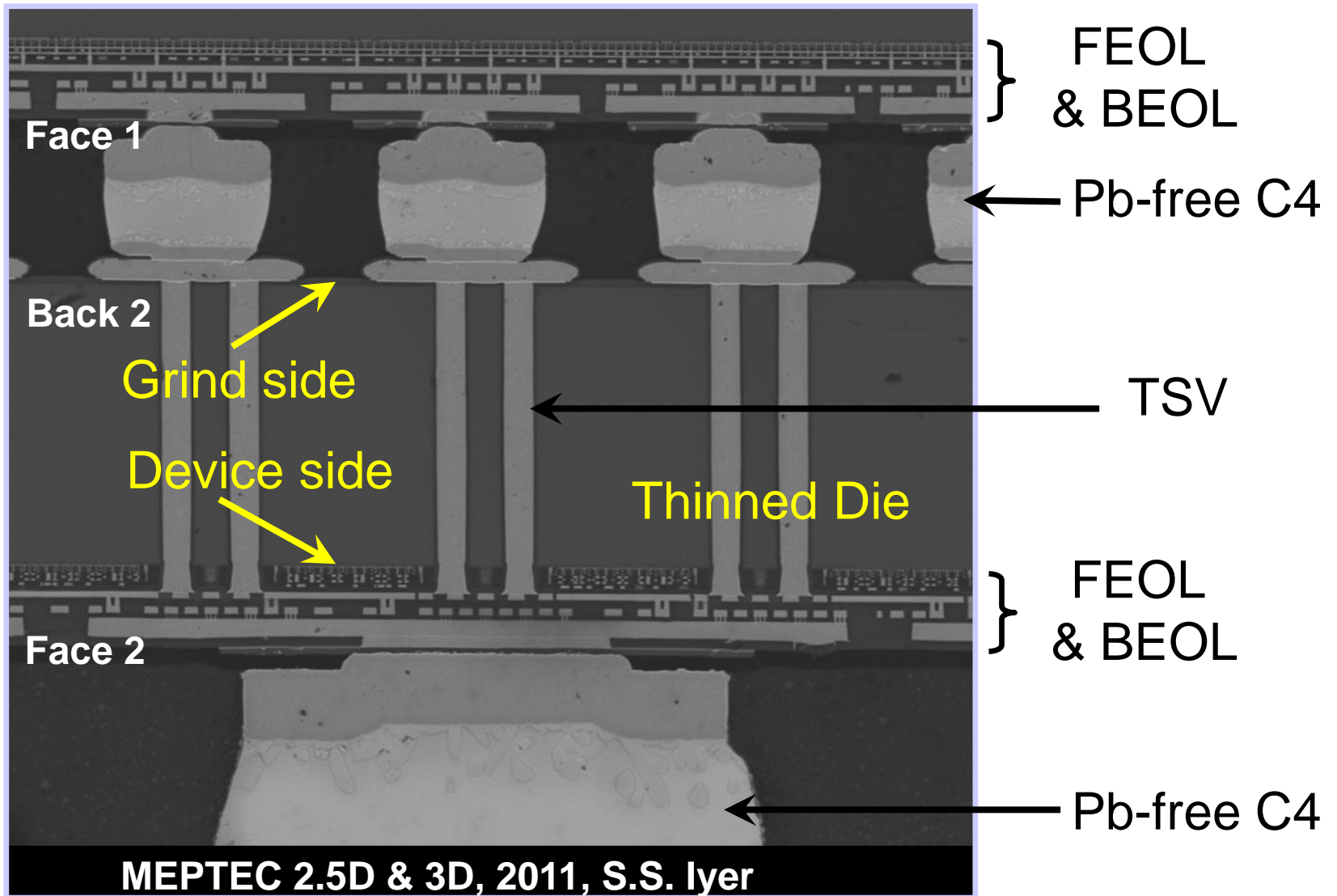
- **Microbump (C4)**



- **Through Silicon Vias (TSV)**



Close up of 45 nm 3D module (Face to Back)



Hybrid Memory Cube



Hybrid Memory Cube
C O N S O R T I U M



Microsoft Open-Silicon

ALTERA

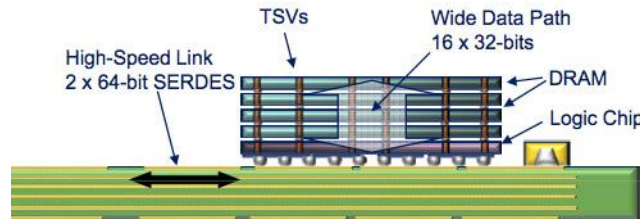
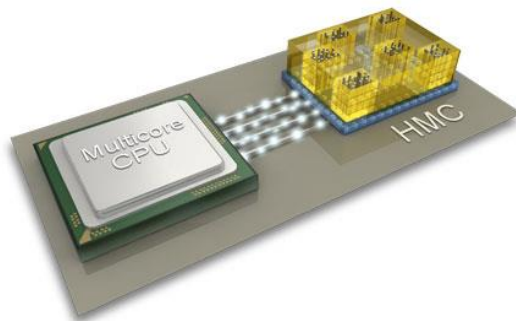
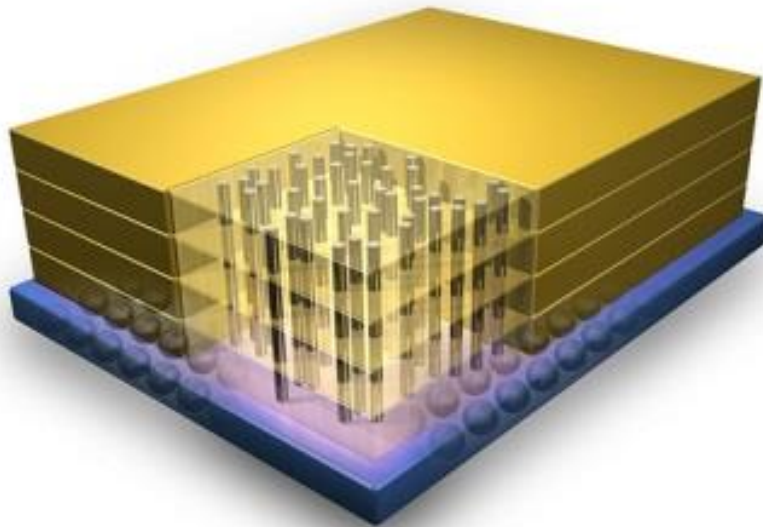


SAMSUNG

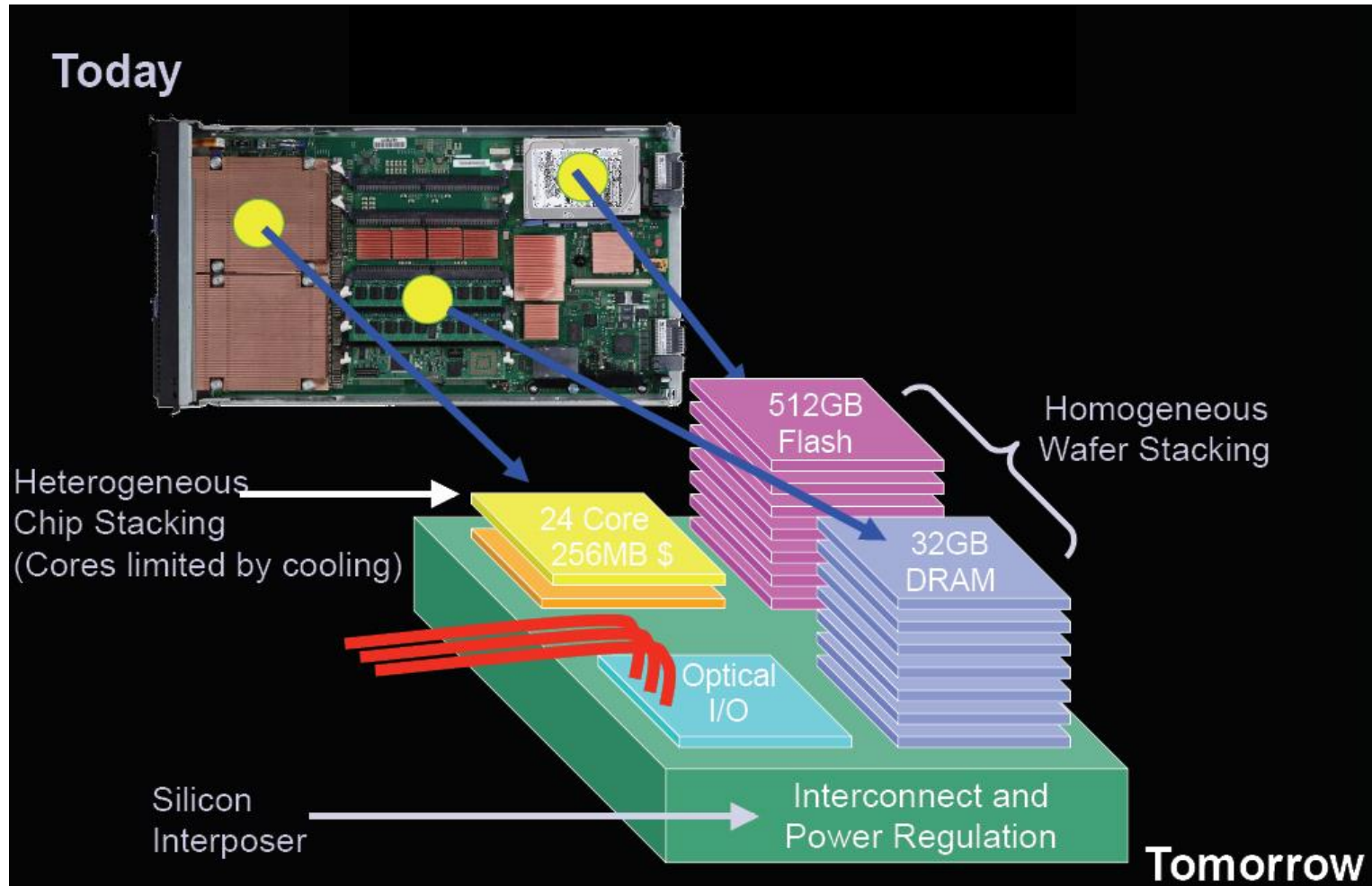
SK hynix

ARM

XILINX



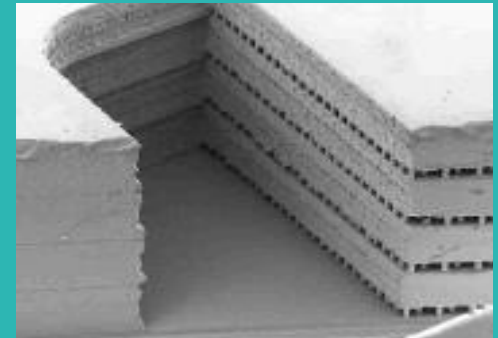
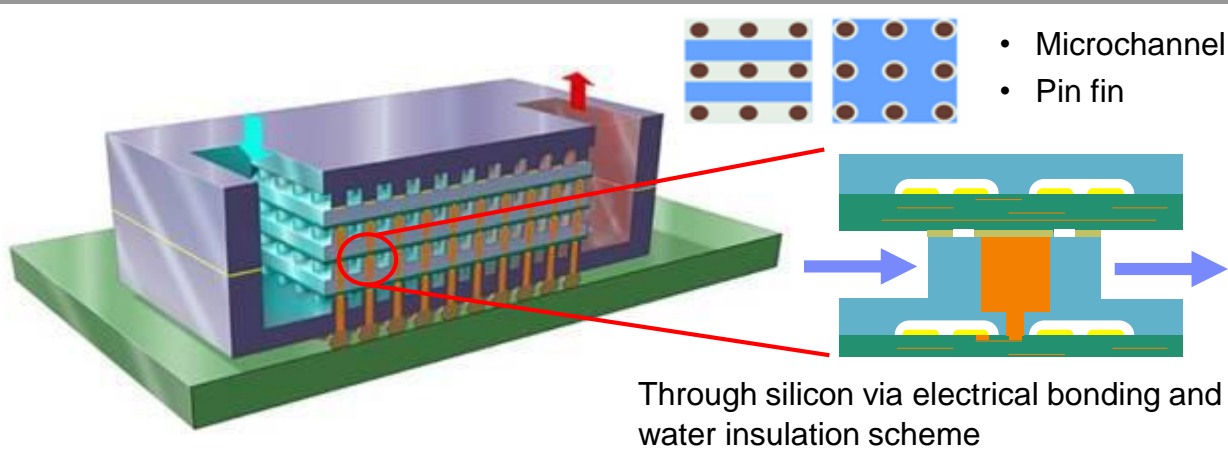
System on Silicon Interposer



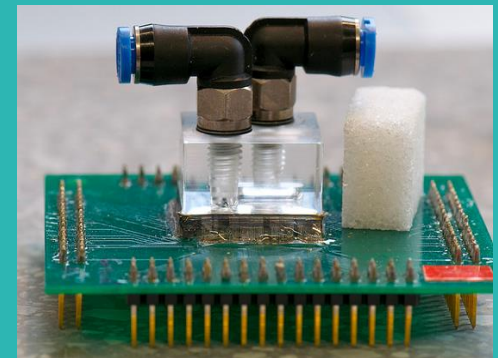
Barth et al, SRC 2011

3D-chips cooled with interlayer liquid cooling

A look inside a 3D-chip stack



cross-section through fluid port and cavities



Test vehicle with fluid manifold and connection

B. Michel et al, CeBIT 2011

**Exploit 3D to full extent
=> System in a Cube...**

IBM System & Technology Group

Vielen Dank
Thank You



Dieter Wendel
wendel@de.ibm.com
+49-7031-163019



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