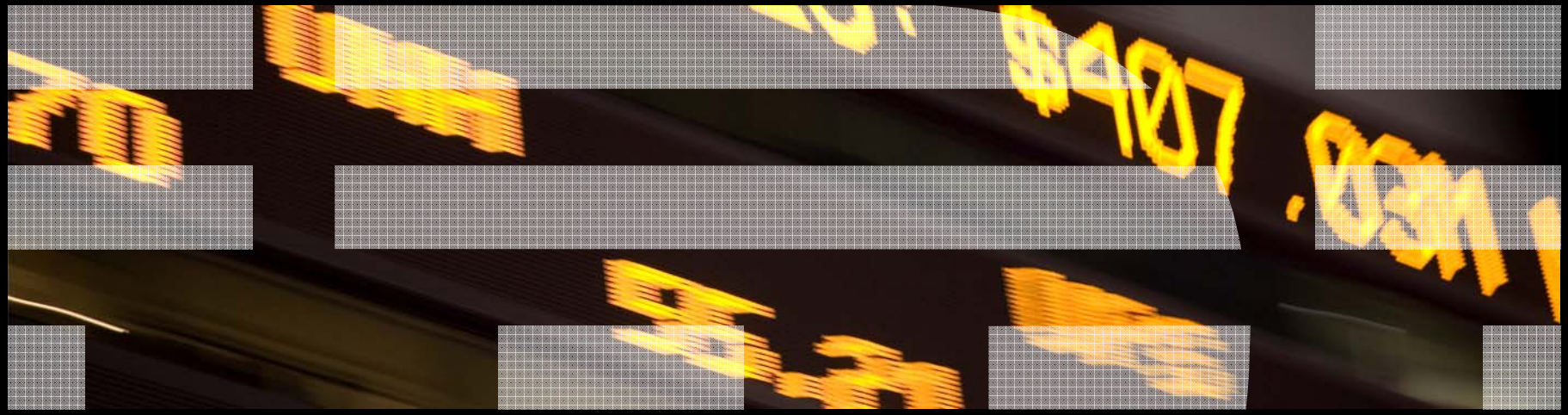
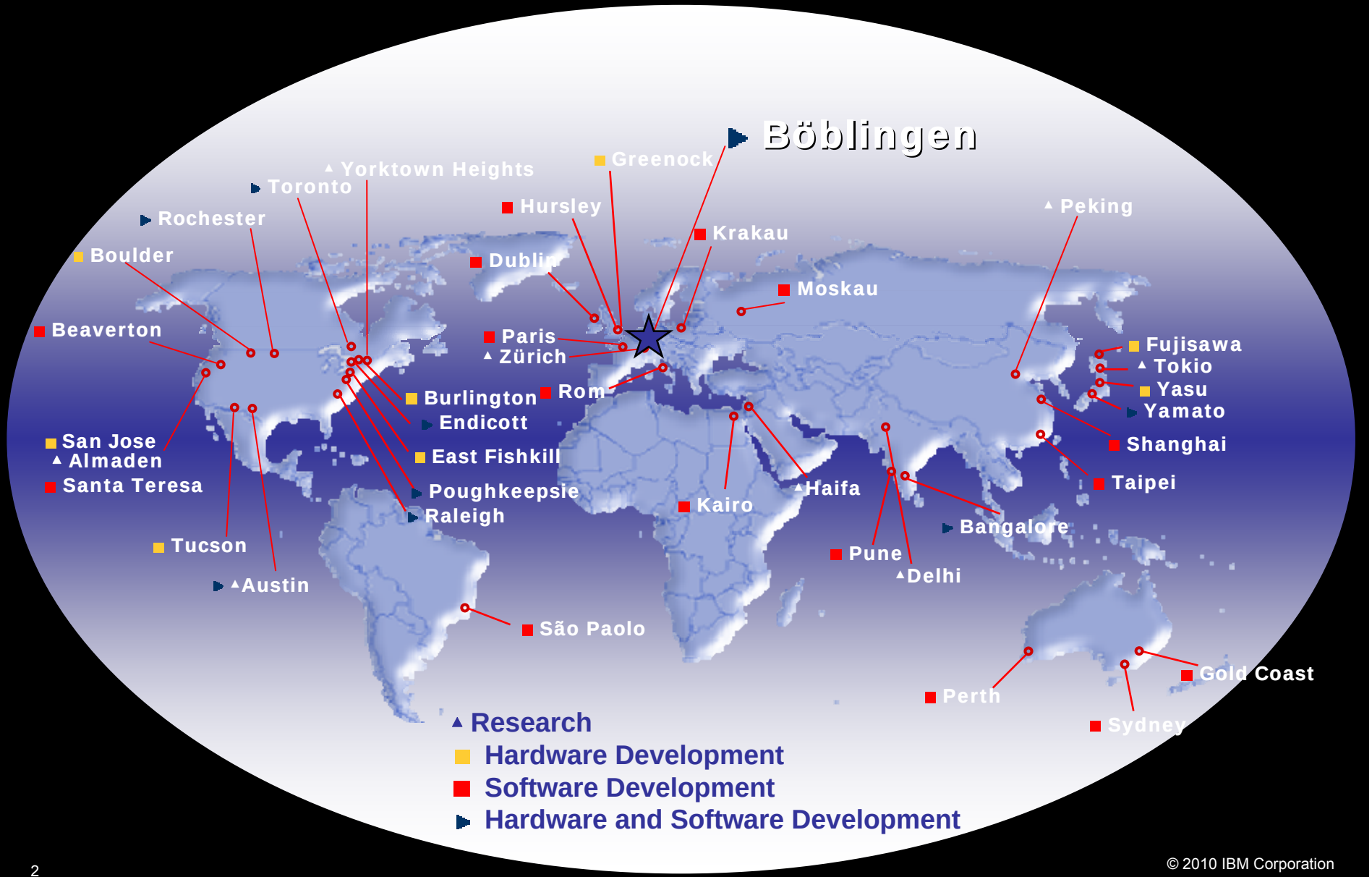
Dr. Harry Barowski, Technology Development, IBM Systems &Technology Group
Guide Share Europe „Frühjahrstagung 2010“ Würzburg (G10)

Aktuelle Entwicklungen auf Prozessor- und Speicherebene – ein Einblick in die IBM Forschung

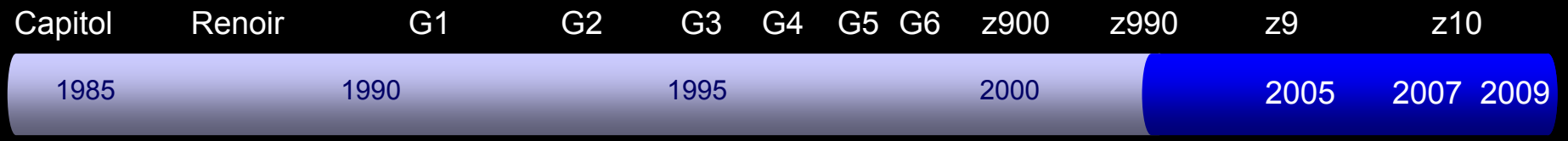


Die wichtigsten IBM Entwicklungs- & Forschungszentren

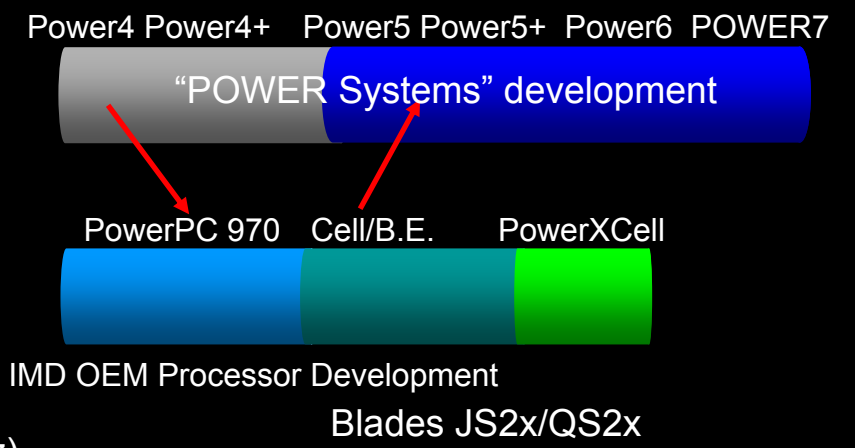


IBM R&D Boeblingen CMOS Hardware Development

"System z" Development (S/390)



- **Development**
  Technology
  Future product technology, optical interconnects
  cooperation w/ European universities
  Processor Architecture
  Logic Design
  Circuit Design
  Physical Design

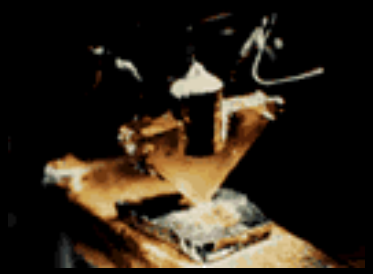


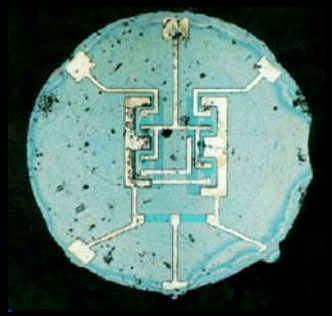
- **Chips**
  Processors, I/O chips (POWER Systems, System z)
  OEM processors (PowerPC 970 „G5" Apple,
  Sony-Toshiba-IBM Cell/B.E. ...)
  ASIC design center

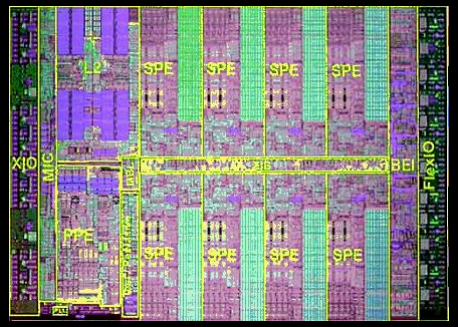
- **Systems/Boards**
  Modules
  Cards
  Blade (PowerPC 970 based JS2x, Cell based workstation)

Meilensteine der Halbleitertechnologie

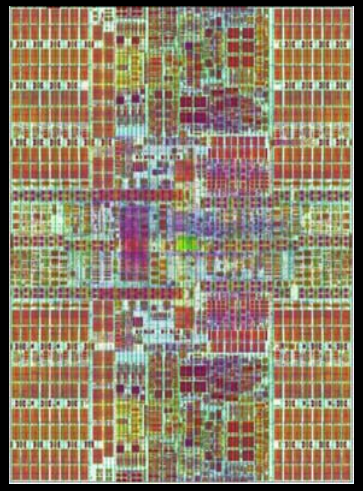
- ***Transistor (1947), Bardeen, Brattain & Shockley***
- ***Erste integrierte Schaltung (1959), Kilby***
- ***Moore's Law (1965)***
  - **„*Cramming more components onto integrated circuits*"**
  - **Komplexität der Chips verdoppelt sich alle 12, bzw. 24 (ab 1975) Monate**
- ***Cell/B.E. (2005)***
  - **234 Millionen Transistoren in 90nm Technologie**
  - ***Heterogene Multicore-Architektur***
- ***POWER6 (2006)***
  - **790 Millionen Transistoren in 65 nm Technologie**
  - **Geschwindigkeitsrekord: 5GHz Taktfrequenz**
- ***POWER7 (2010)***
  - **1,2 Milliarden Transistoren in 45nm**
  - **8core with 4way SMT**
  - **>4GHz Taktfrequenz**





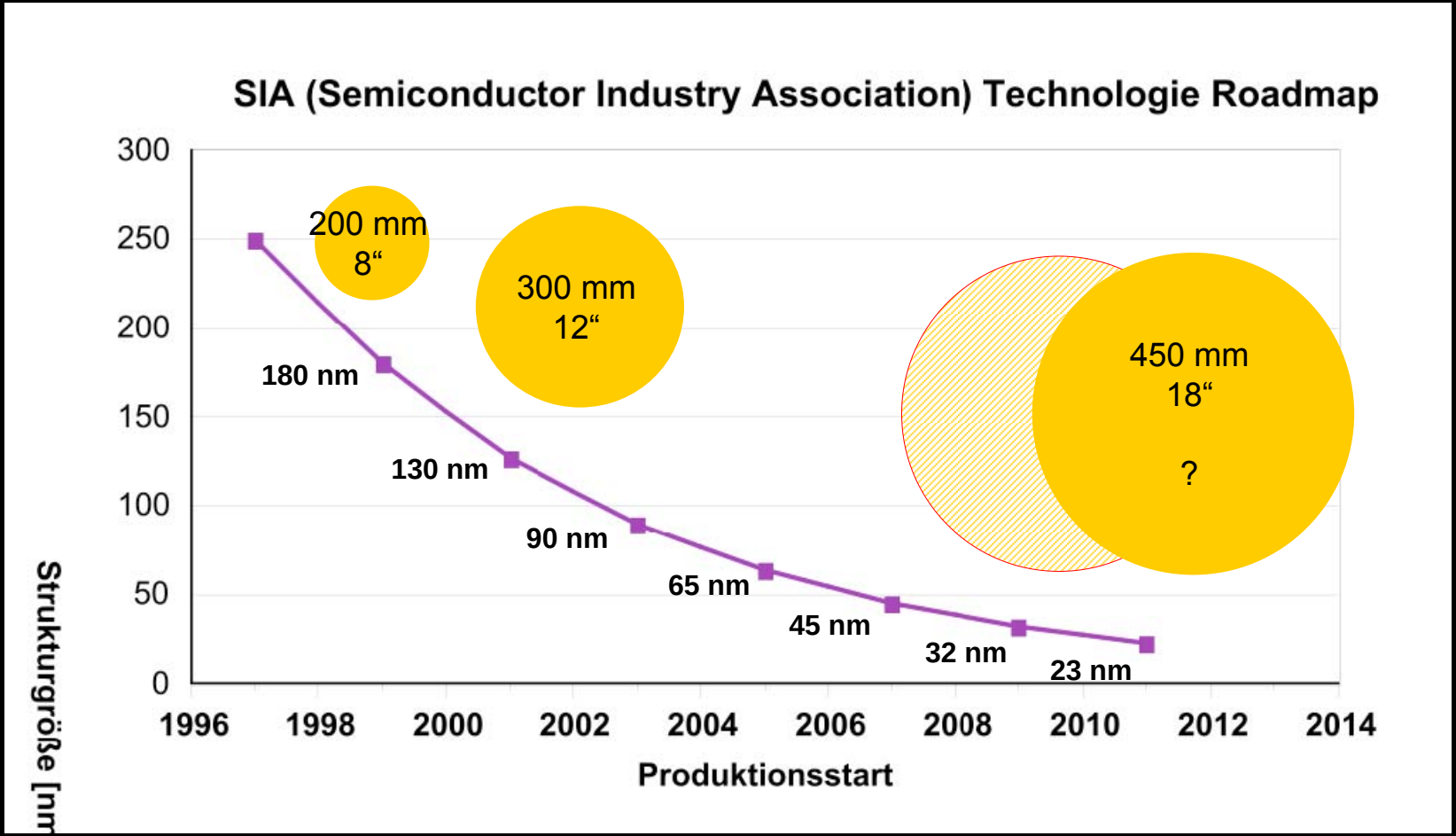


Cell/B.E.
9 cores! 1 PPE, 8 SPEs



POWER6
DualCore >>5GHz!

Siliziumtechnologie: CMOS Generationen und Wafergröße

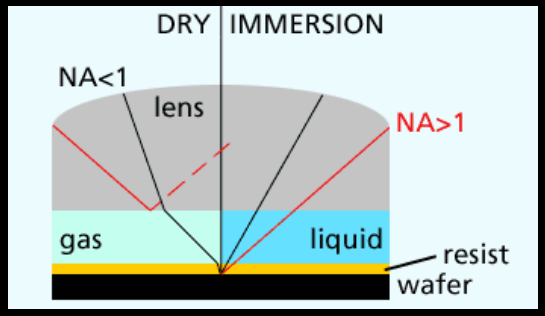


Photolithographie: UltraViolett => DeepUV => ExtremeUV?

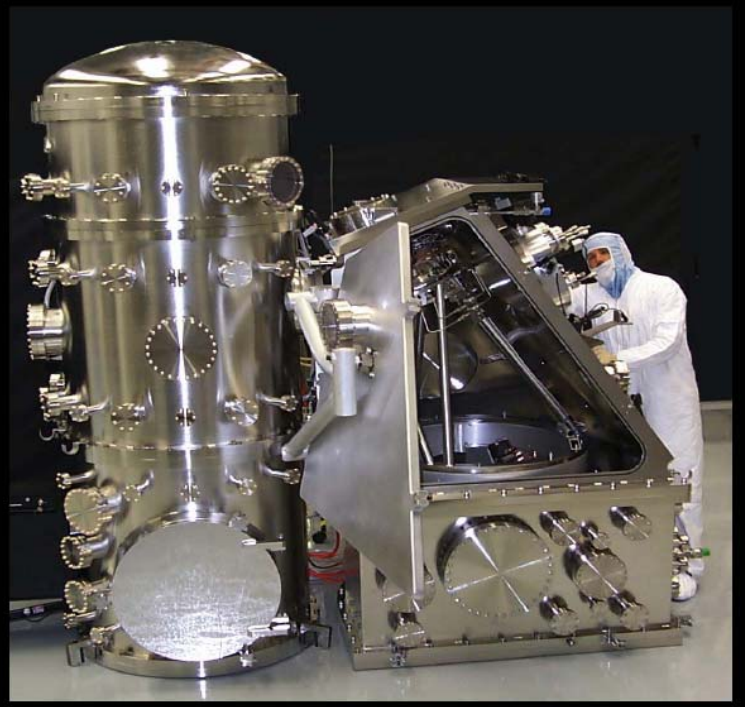
Jahr	Strukturgröße	Lichtquelle	Bereich	Wellenlänge
1993	0,5 µm	Hg	G-Linie	436 nm
1995	0,35 µm	Hg	I-Linie	365 nm
1997	0,25 µm	Excimer (Excited Dimer)	DUV (Deep UV)	248 nm
1999	0,18 µm	Excimer	DUV	248 nm
2001	130 nm	Excimer	DUV	248 nm
2003	90 nm	Excimer	DUV	193 nm
2005	65 nm	Excimer	DUV	193 nm PSM
2007	45 nm	Excimer	DUV	193 nm Immersion

Double patterning/exposure with 193nm immersion?

(According to ITRS)



Extreme Ultra-Violet (**EUV**)



CMOS: Sättigung der Technologie?

Technology	General Availability	Limits of technology	Technical limits	Solution/Forecast
45nm CMOS12	▪ **2009**	193nm: NA>1 required Gate leakage		▪ Immersion (water based) lithography ▪ High k, metal gate
32nm CMOS13	▪ **2011**	▪ 193nm (ArF) lithography at limits ▪ Variability control ▪ Low-k slowdown		▪ EUVlight? ▪ Double exposure/patterning ▪ UTB-FDSOI / DoubleGate (FinFET) ▪ AirGap
22nm CMOS14	▪ **2014**	▪ Economic limit? ▪ Deterministic doping ▪ Quasi-ballistic transport: ▪ 193nm lithography ends	▪ No performanc gains . ▪ Reduced density gain ▪ gate length ~ mean free path => current limited by contacts	▪ 450mm wafer production ▪ 3D integration ▪ New transistor models/designs ▪ high refractive index immersion lithography
15nm CMOS15	▪ **2017**	▪ EUV limits	▪ EUV destruction ▪ Photoresist limitations	▪ Emerging new devices: CNT FET / SET / spin devices
9nm CMOS16	▪ **2021**	Physical limits reached?		▪ New devices?
5nm CMOS17	▪ **2025**	Final frontier?		

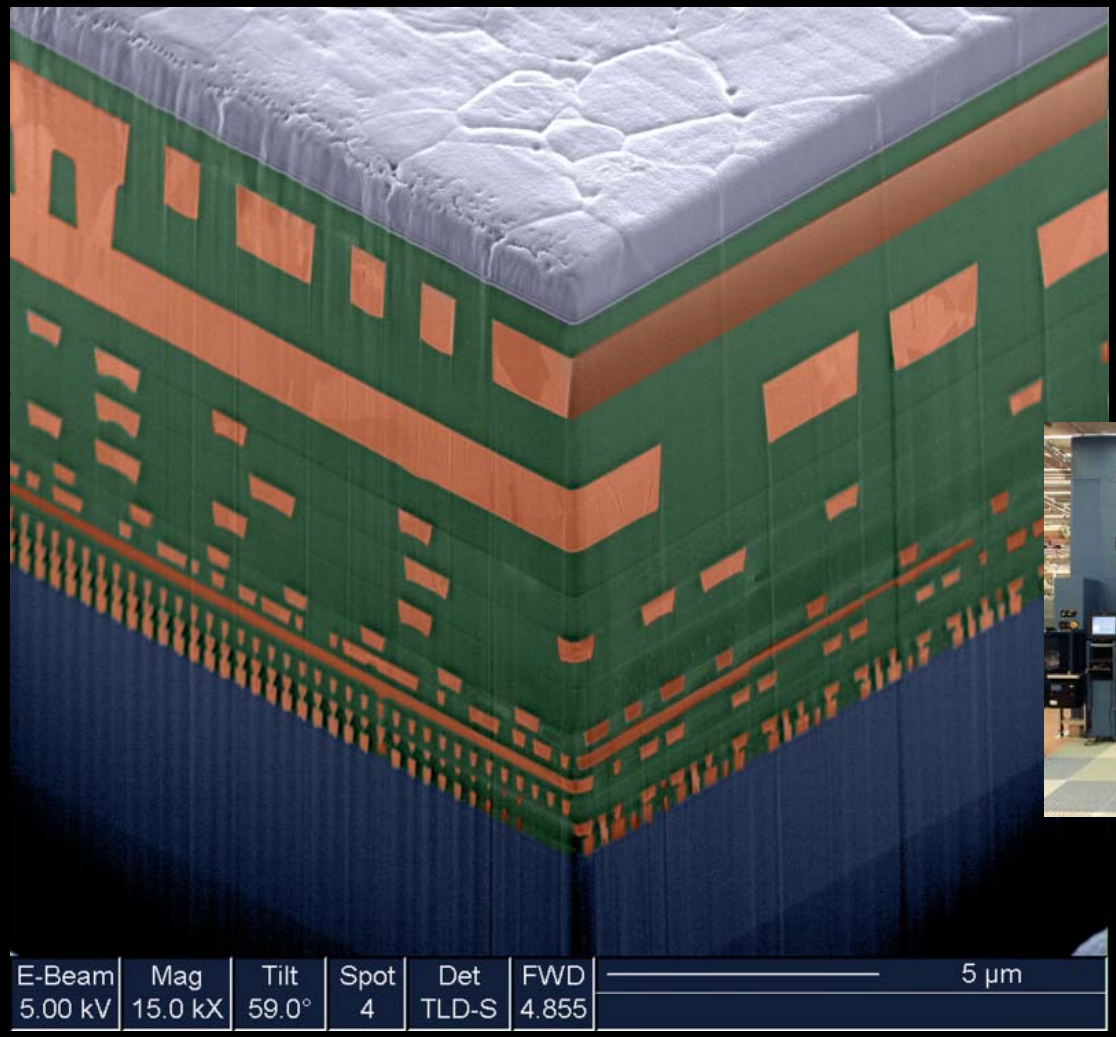
State-of-the-art Technologie, e.g. SEM of 10 Layers of Metal

Layer Thickness

6x (1.2µm)

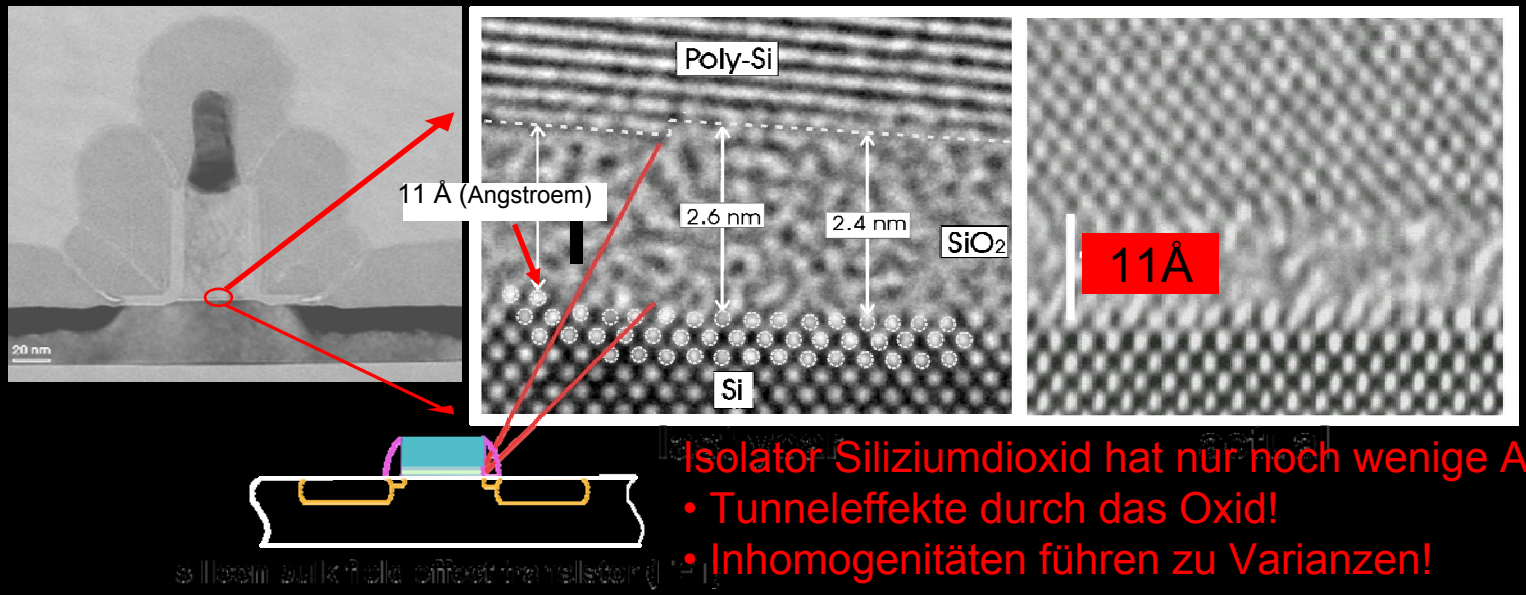
2x (0.50µm)

1x (0.25µm)



semiconductor INTERNATIONAL TOP FAB

Limit to Scaling: “Approaching Atomic Dimensions”



Isolator Siliziumdioxid hat nur noch wenige Atomlagen!

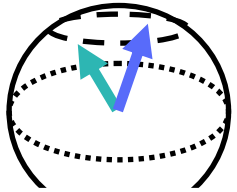
- Tunneleffekte durch das Oxid!
- Inhomogenitäten führen zu Varianzen!

Ende von Skalierung = *Neue Ära durch Quantencomputer???*

=> Bits und Schaltkreise erreichen atomare Dimensionen von Atomen & Molekülen

"Quantum computing begins where Moore's law ends."

Quantenzustände einzelner Atome/Moleküle als QuBits



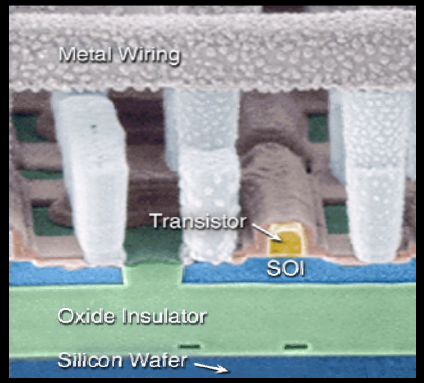
$|\neg\rangle = c_0|0\rangle + c_1|1\rangle$

$|\surd\rangle = c_0|0\rangle - c_1|1\rangle$

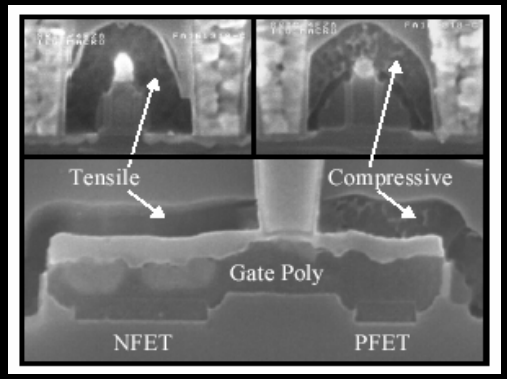
Das Ende der Skalierung: bisherige Innovationen

- **Neue Materialien**
- **Innovative Transistorstrukturen**

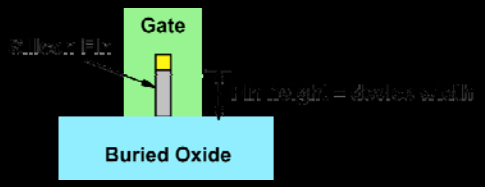
Kupfer-Verdrahtung, Low-K

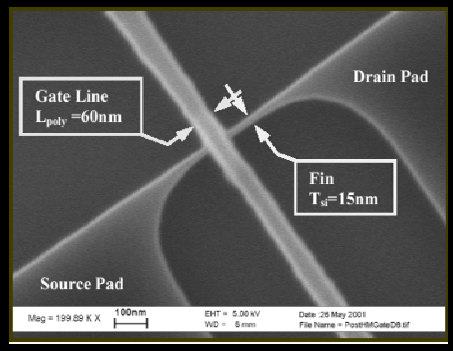


Silicon-On-Insulator



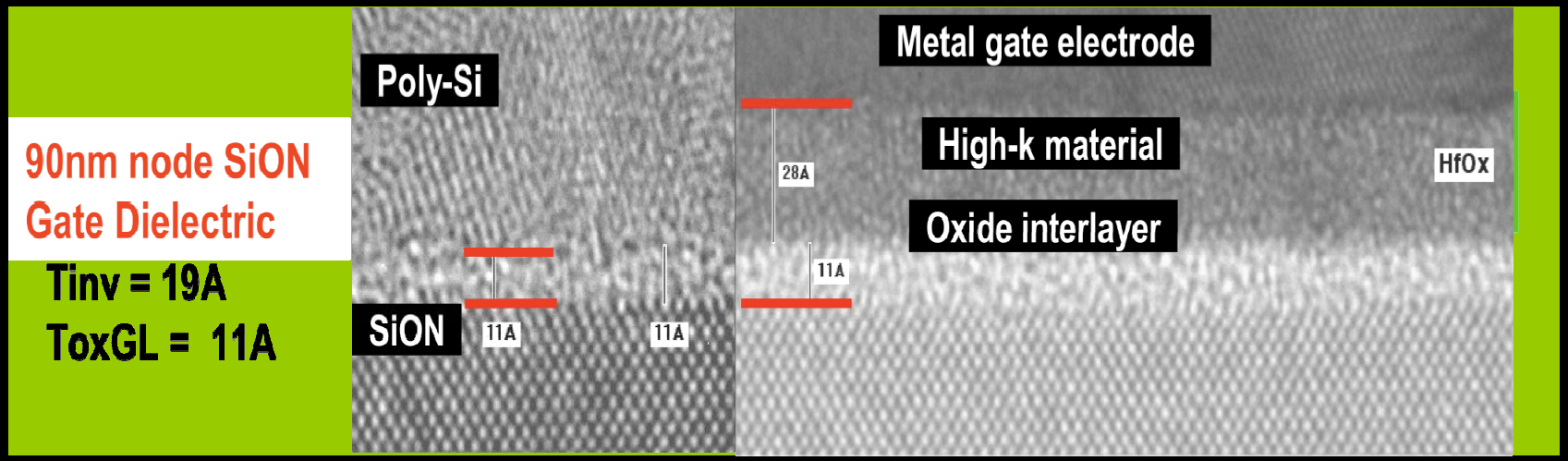
Verspanntes Silizium





Double-Gate Transistor (FinFET)

High-K Material und Metallgate im CMOS Transistor



Leckströme > 10x reduziert ➔ mehr aktive Leistung möglich (Takt)

Höhere Prozessorrechenleistung bei gleicher Leistungsaufnahme
durch z.B. komplexere Logik,
höhere Taktfrequenz

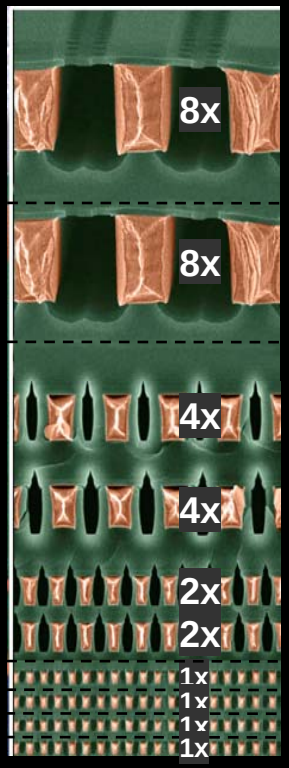
oder

Weniger Leistungsaufnahme bei gleicher Rechenleistung

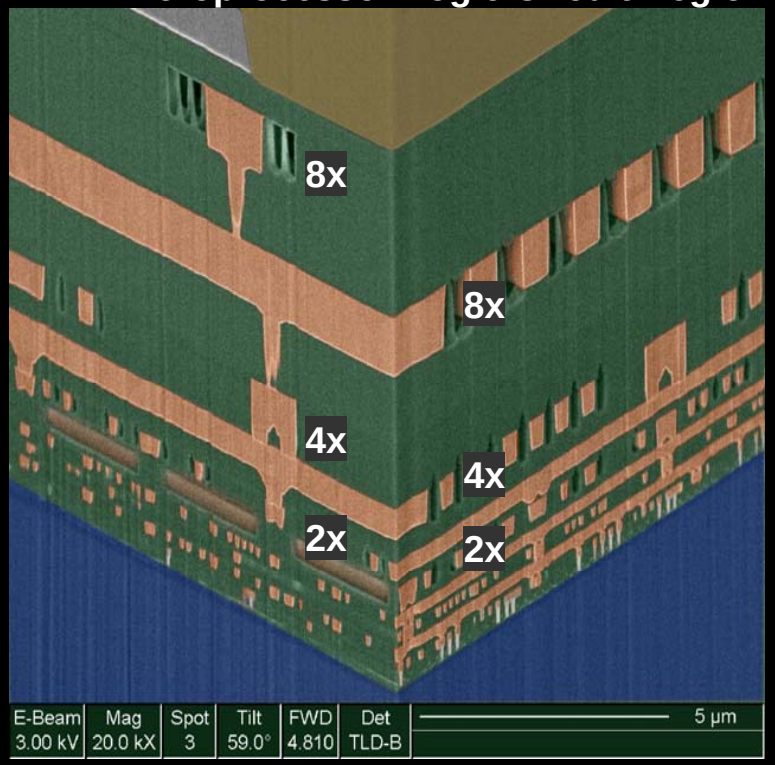
=> Gültigkeit von Moore‘s Law für 32nm, 23nm, ...

Innovation im Back End (Airgap-Technology)

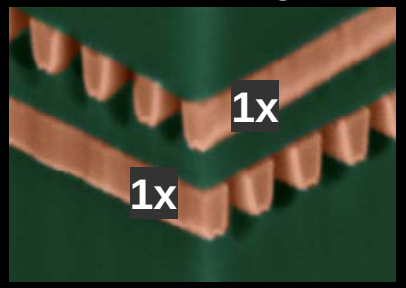
Mazes



Microprocessor Logic Circuit Region



Capacitance reduction 35 % 1x Wiring



Neuer Prozess erzeugt Milliarden von uniformen „Löchern“ in speziellen Geometrien

Reduziert kapazitive Kopplung der Leitungen, schnellere Signalübertragung, weniger Noise

Erste Technik, die **Selbstorganisation von Materialien** nutzt:

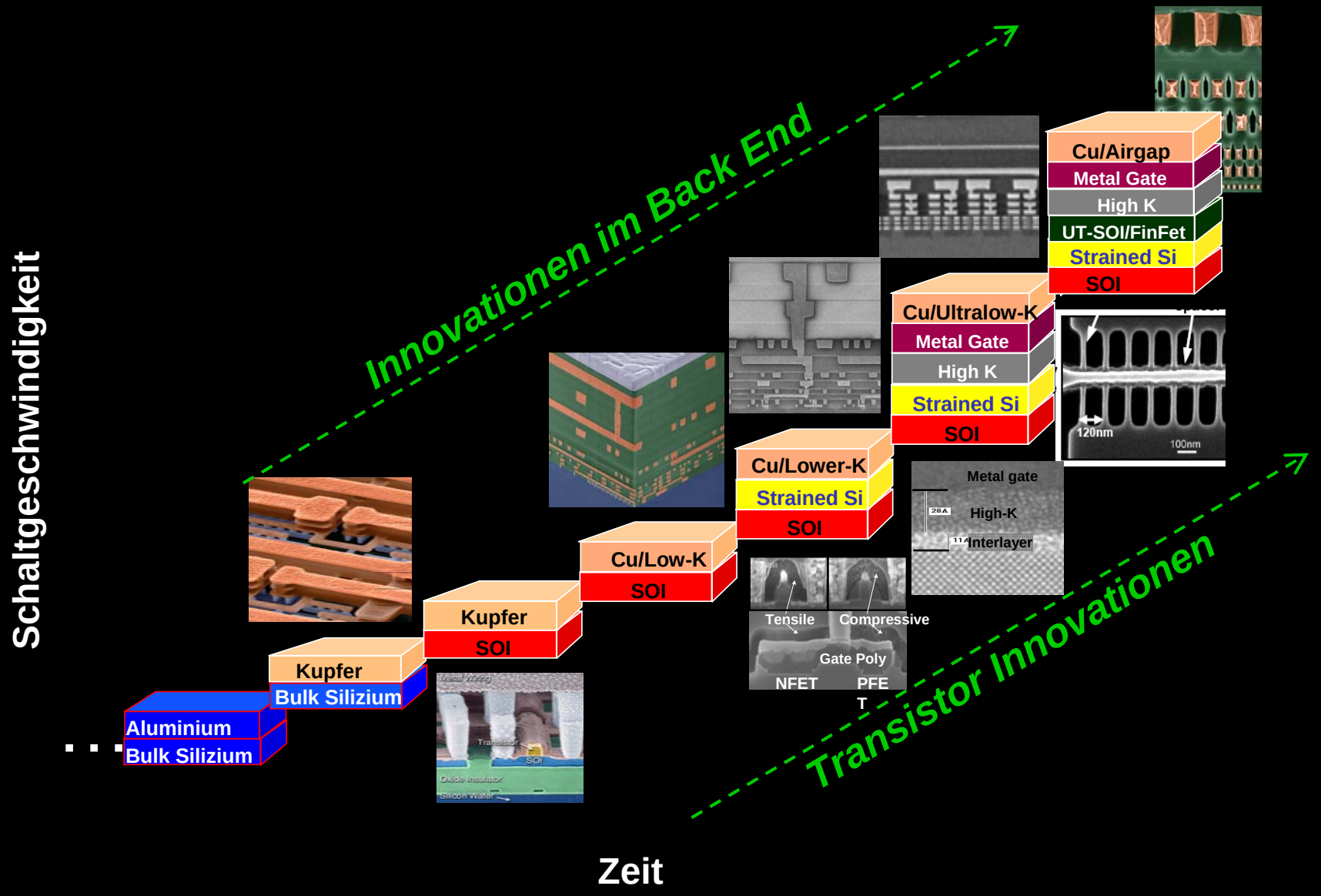
➔ Ausweg aus Lithographie?

Fazit:

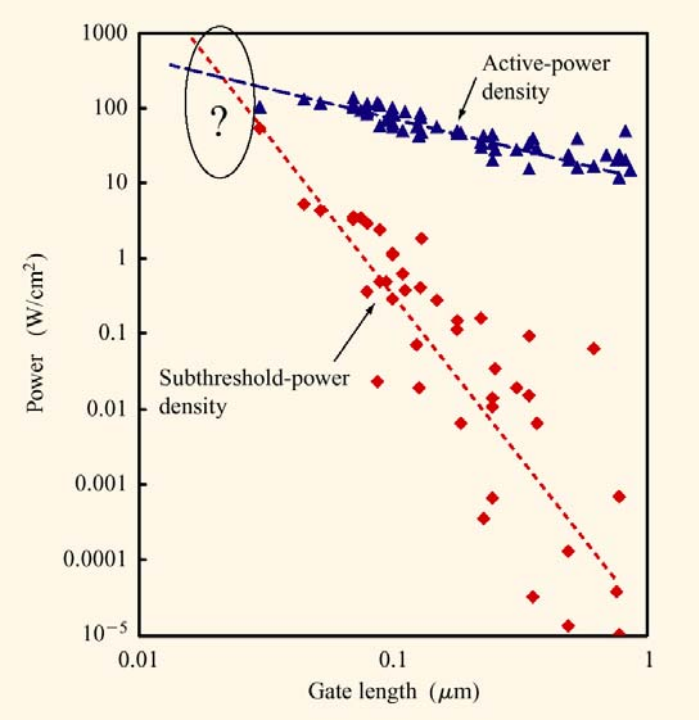
Höhere Prozessorleistung bei gleicher Leistungsaufnahme ODER weniger Leistungsaufnahme bei gleicher Rechenleistung!

http://www-03.ibm.com/press/us/en/photos.wss?rN=31&topic=6

IBM CMOS Innovationen

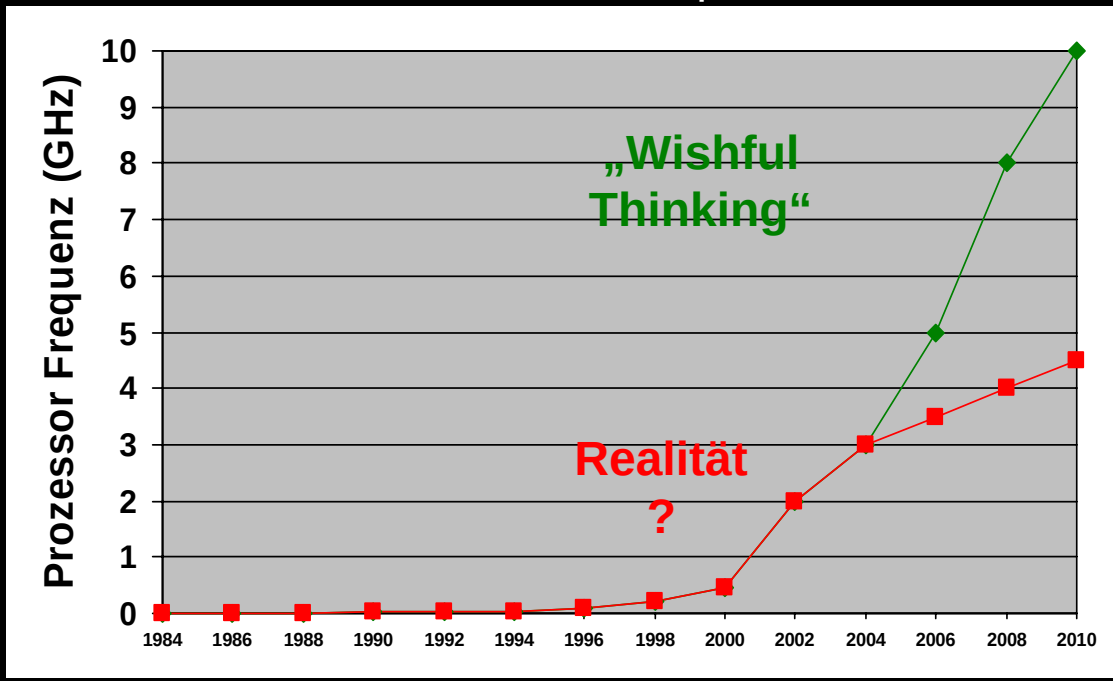


Energiedichte als Designhürde?



Skalierung erlaubt höhere Taktgeschwindigkeit
=> Lineare Zunahme der aktiven Verlustleistung

Skalierung führt zu unerwünschten Leckströmen
=> Drastische Zunahme der passiven Power



D.J. Frank et al., IBM J. RES. & DEV. VOL. 46 NO. 2/3 MARCH/MAY 2002

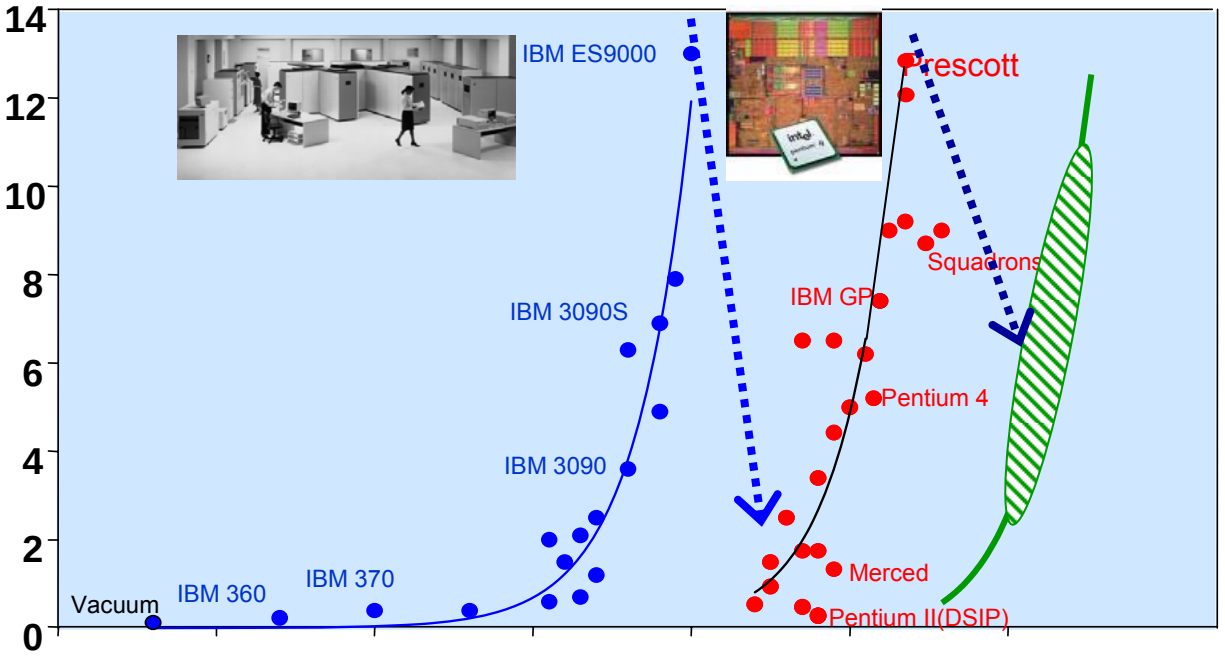
„Verlust“-Leistung formal

$$P_{active} = \alpha f C V_{dd}^2$$

$$P_{leakage} = I_{leakage} V_{dd} \ (\approx> V_{dd}^3)$$

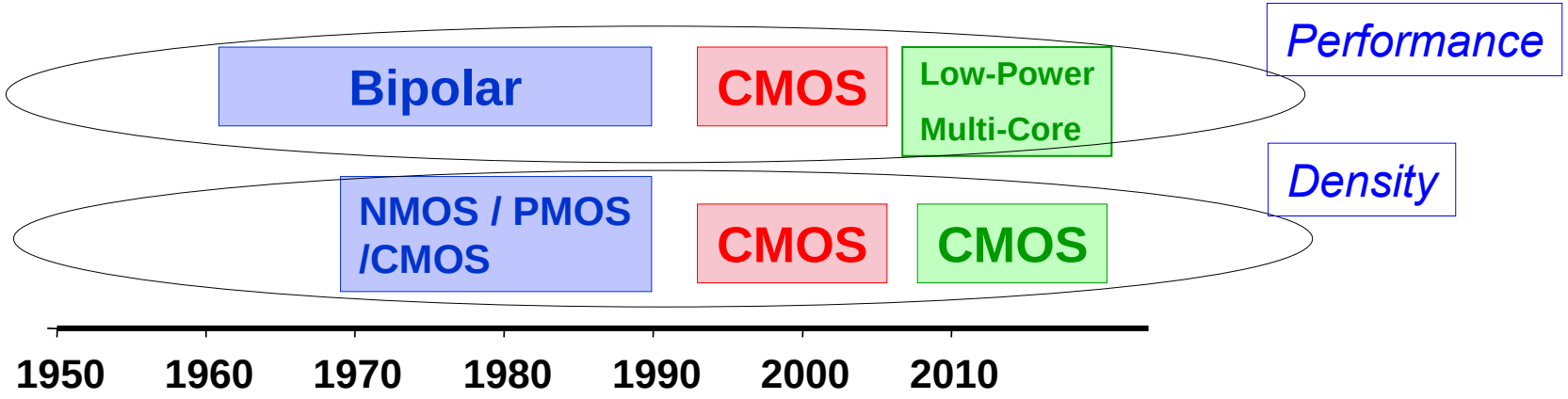
Fazit: ENERGIEDICHTE begrenzt Taktfrequenz!

System Performance durch Multicore-Technik

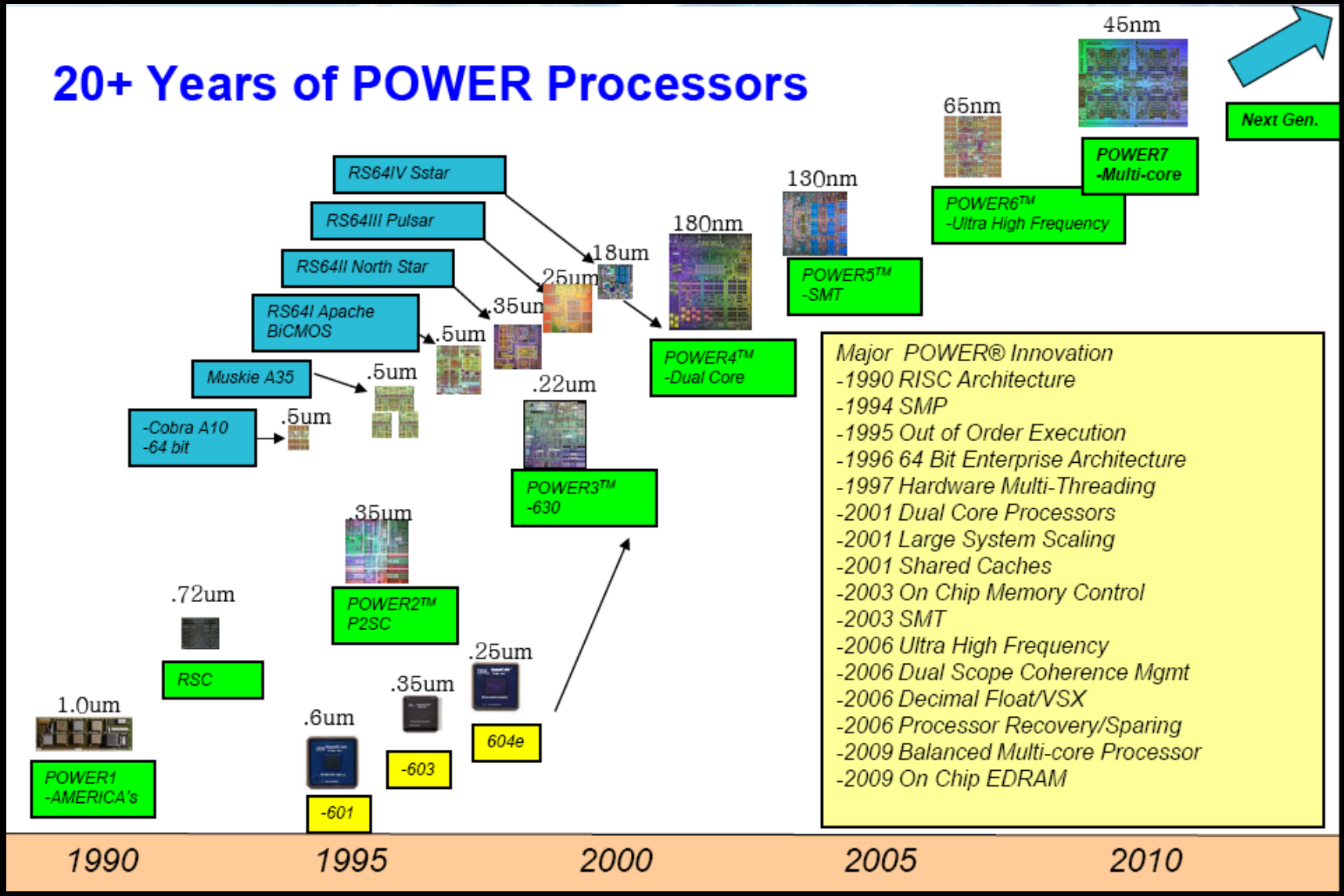


Disruptive Entwicklungen

„Phasenübergange“



POWER processor roadmap



IBM eServer Prozessoren

System z
(S/390)
Zero-Downtime

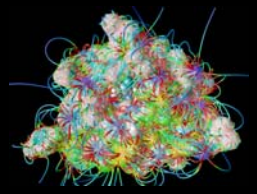
Z10

64 Prozessoren (16x QuadCore)

4,4 GHz, 65 nm

MultiChipModule:
~ 8 Milliarden Transistoren
18km Kupferdraht
8 Chips/MCM

Blue Gene/P

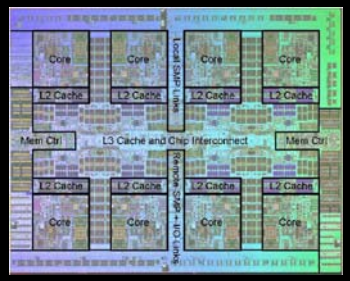


PowerPC450 core
850MHz, 4-way SMP node
- **100 000 cores**
- **1 Petaflops/s**

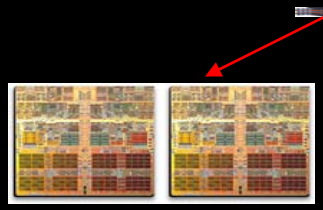
IBM Blades JS/QS-family

POWER systems
(System p, RS/6000)
Performance

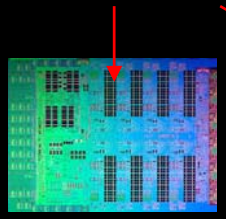
(System I, AS/400)
Integration



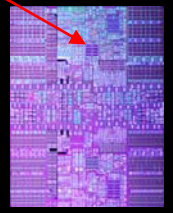
POWER7
1,2 Milliarden Transistoren
4,14 GHz, 45 nm
8 cores, each 4way SMT



PowerPC 970MP
2.7GHz, 90 nm
1MB L2 pro Kern



Cell/B.E.
3.2GHz, 65 nm

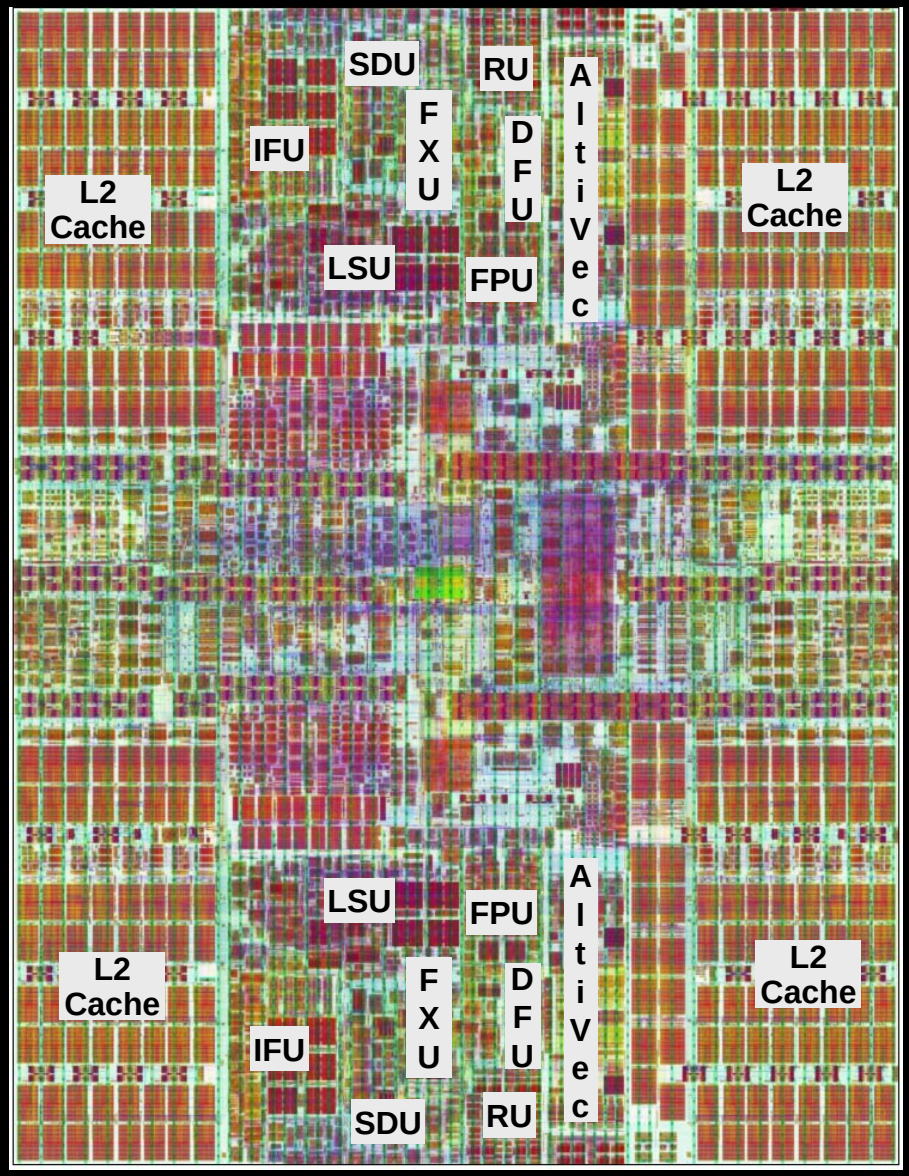


P6+
4.7GHz, 65 nm

IBM

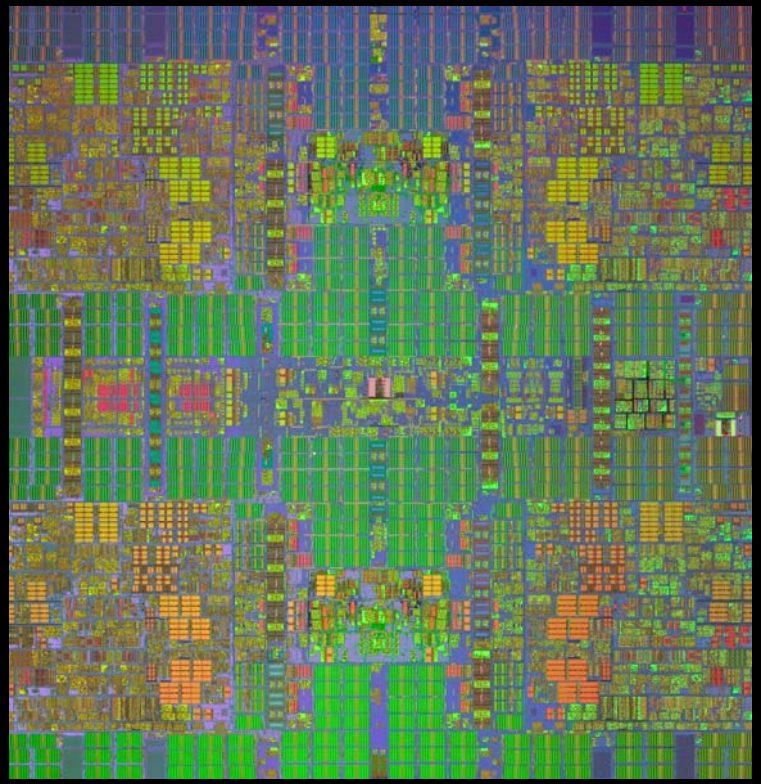
POWER6 Chip - DualCore

- **Dual Core Chip**
  - 2-way SMT Core
  - Frequency > 4 GHz
  - Superscalar
  - 8 MB on-chip L2, 32 MB off-chip L3
  - On-chip L3 directory & controller
  - Two memory controllers on-chip
- **Technology**
  - CMOS 65nm Lithography, Silicon-On-Insulator
  - 790 Million Transistors, 343 mm^2
  - 4,5 km Copper wire on 10 metall layers
  - 1953 Signal I/O, 5399 Power/GND I/O
- **Full error checking and recovery**



IBM System z10 – QuadCore

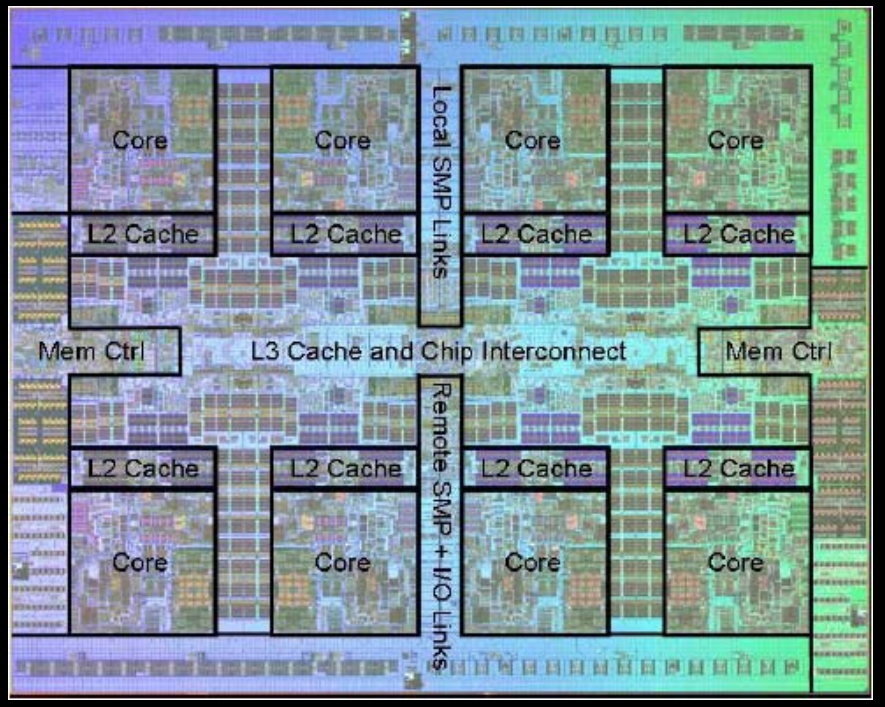
Implementation	**65nm SOI CMOS** **2way superscalar in-order**
Frequency	**4.4 GHz**
Architecture	894 instructions, 668 hardwired
Arithmetic	64bit ALU IEEE 754 floating point decimal floating point hex-floating point
Elements	5 quadcore processors on one MCM **994 mio transistors per processor** **8 billion transistors per MCM**
Memory	192kB L1 cache (128kB D/ 64kB I) per core 12MB (4x 3MB) L1,5 cache on die 48MB L2 cache on MCM (2x 24MB) 16GB up to 1,5 TB mainstorage
Power	10kW up to 27,5 kW



Source: http://www-03.ibm.com/systems/de/z/hardware/z10ec/specifications.html

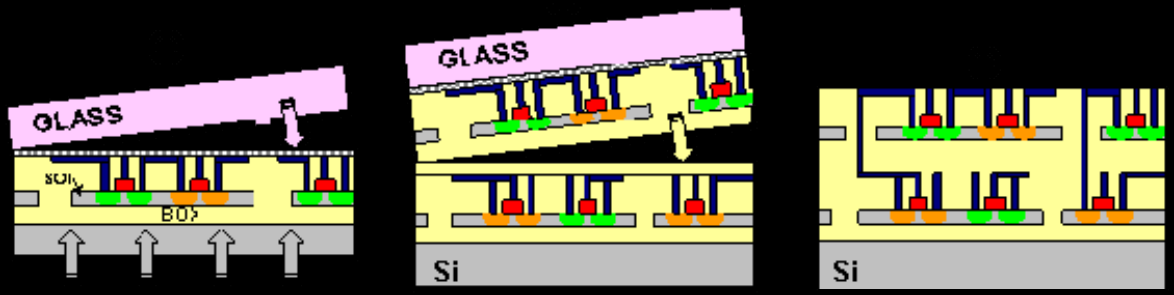
POWER 7 Processor Chip - OctoCore

- 567mm², 45nm lithography, Cu, SOI, eDRAM
- 1.2B transistors
  - Equivalent function of 2.7B
  - eDRAM efficiency
- Eight processor cores
  - 12 execution units per core
  - 4way SMT per core
  - 32 threads per chip
  - 256KB L2 per core
- 32MB on chip EDRAM shared L3
- Dual DDR3 Memory Controllers
  - 100GB/s memory bandwidth per chip sustained
- Scalability up to 32 sockets
  - 360GB/s SMP bandwidth/chip
  - 20,000 coherent operations in flight
- Advanced pre-fetching Data and Instruction
- Binary Compatibilty with POWER6

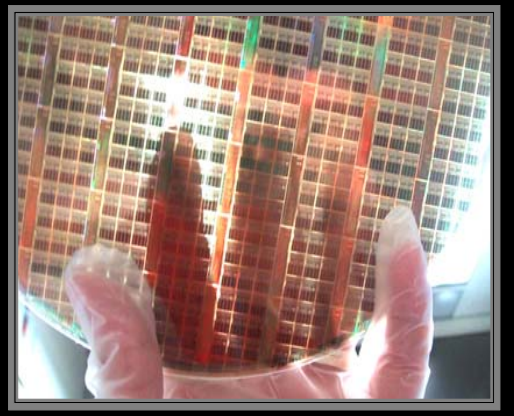


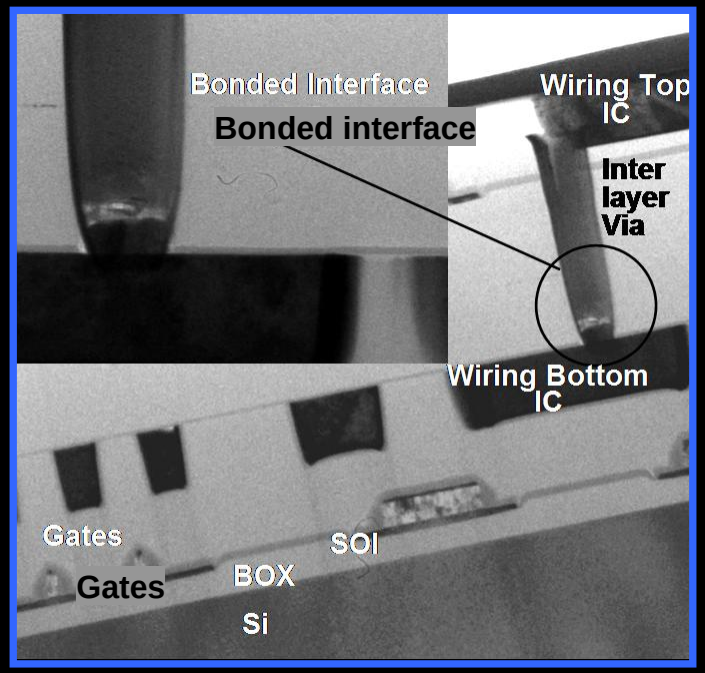
Ron Kalla, HotChips2009

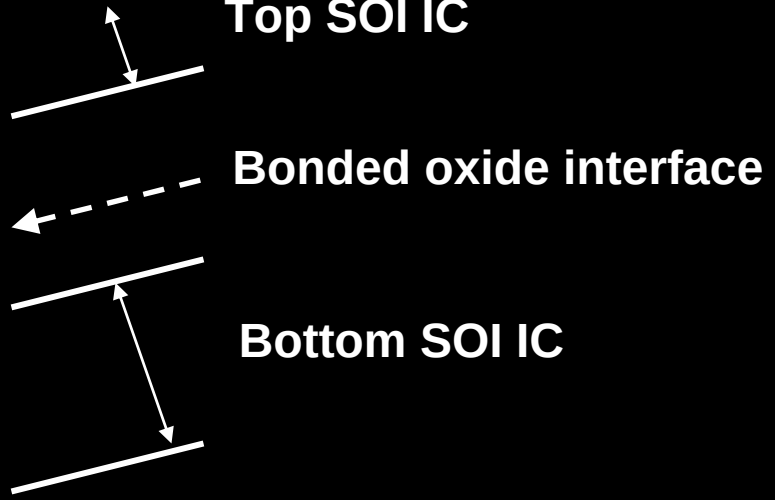
3D Integration



A.W. Topol (IBM), IEDM 2005.







I1 BM EXTENDS MOORE'S LAW TO THE THIRD DIMENSION: An IBM scientist holds a thinned wafer of silicon computer circuits, which is ready for bonding to another circuit wafer, where IBM's advanced "through-silicon via" process will connect the wafers together by etching thousands of holes through each layer and filling them with metal to create 3-D integrated stacked chips. The IBM breakthrough can shorten wire lengths inside chips up to 1000 times and allow for hundreds more pathways for data to flow among different functions on a chip. This technique will extend Moore's Law beyond its expected limits, paving the way for a new breed of smaller, faster and lower power chips.

IBM_USER; 04.10.2007

Forschung: 3D Chips und atomares Rechnen

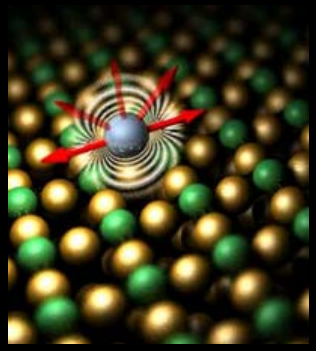
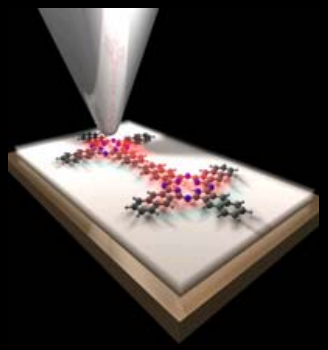
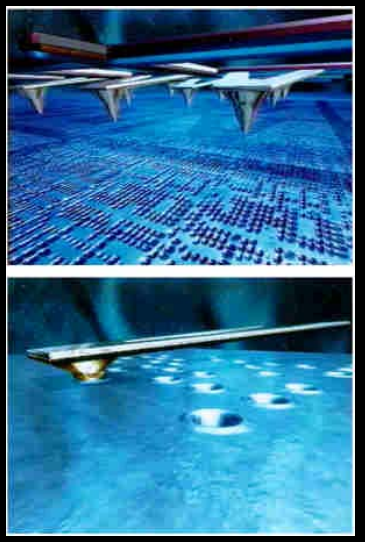


Illustration of the preferred magnetic orientation of an iron atom on a specially prepared copper surface. The stability of an atom's magnetic orientation can help determine that atom's suitability for storing data.



Schematic three-dimensional image of a molecular "logic gate" of two naphthalocyanine molecules, which are probed by the tip of the low-temperature scanning tunneling microscope.

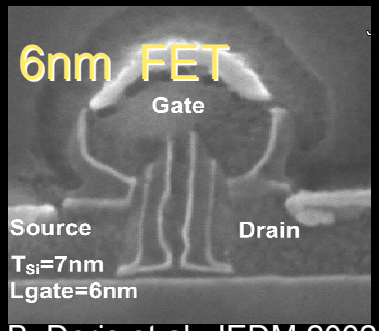
- Stand der Technik
  - Informationsträger besteht aus Mio Atomen.
  - Festplattengrösse: 1 TeraByte
- Forschung
  - 3D Chips
  - Speichern von Daten auf Atomen
  - Schalter basierend auf Molekülstrukturen
  - Speicherdichte 1000 mal höher
  - iPod könnte 30.000 Spielfilme speichern.
- Andere Forschungsbereiche:
  - Millipede
  - …



An animated view of the Millipede nanomechanical storage device illustrates how an individual tip creates an indentation in a polymer surface (bottom) and how a large number of such tips are operated in parallel (top).

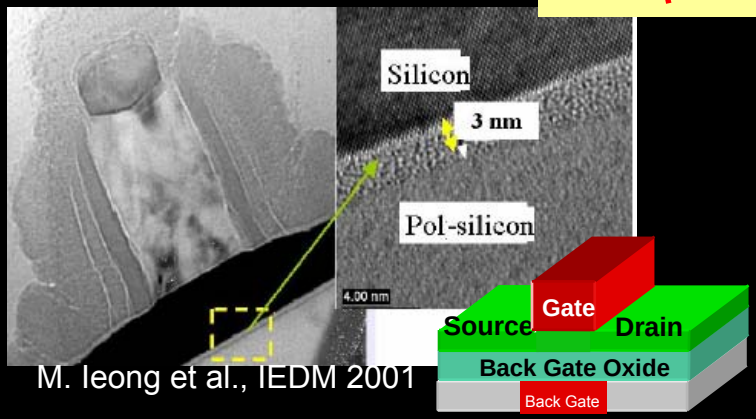
Neue Transitorstrukturen für die Zukunft

UTSOI



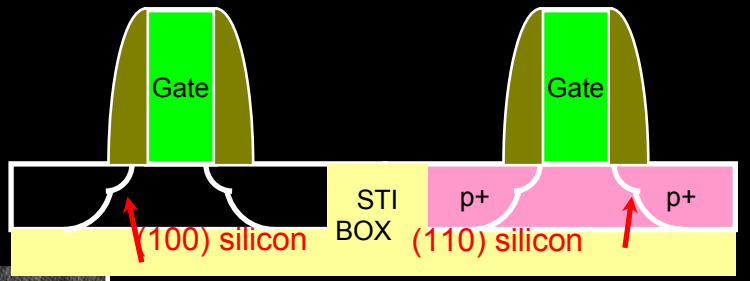
B. Doris et al., IEDM 2002

Back-Gate

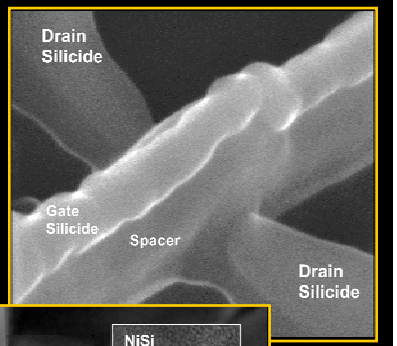


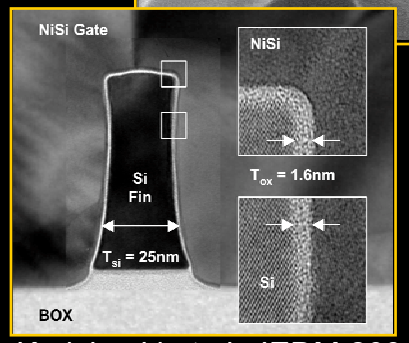
M. Ieong et al., IEDM 2001

Super-HOT



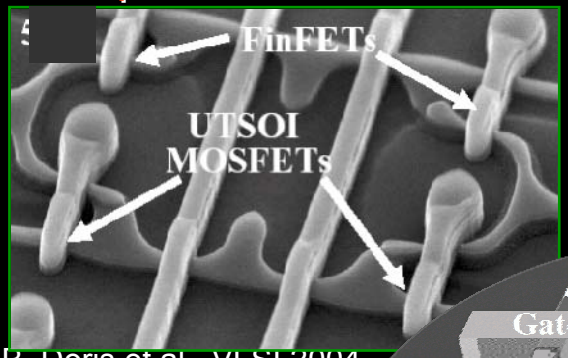
FinFET



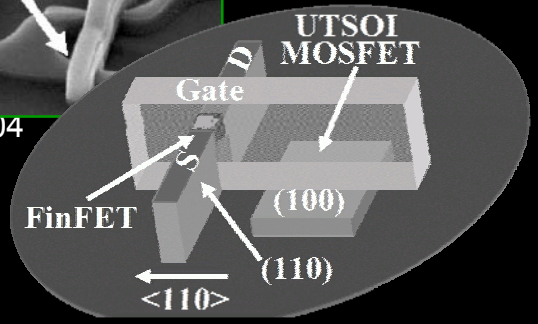


Kedzierski et al., IEDM 2001-3

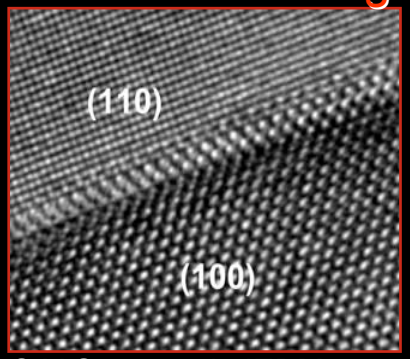
Simplified HOT



B. Doris et al., VLSI 2004

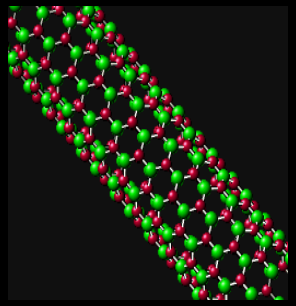


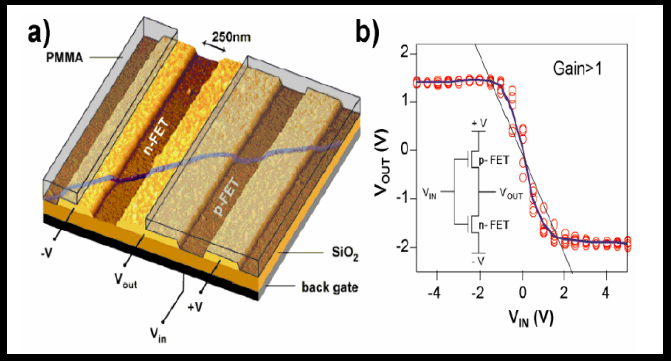
Direct Substrate Bonding

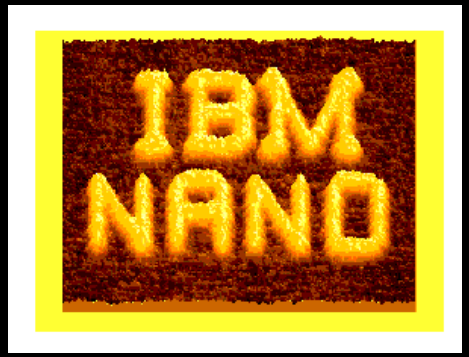


C-Y Sung et al., IEDM 2005

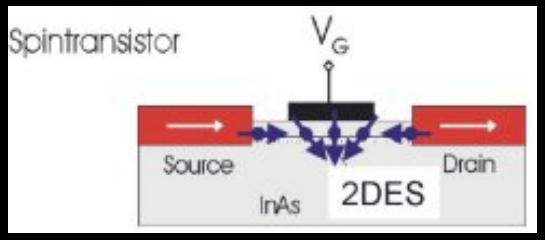
Zukünftige Chiptechnologien

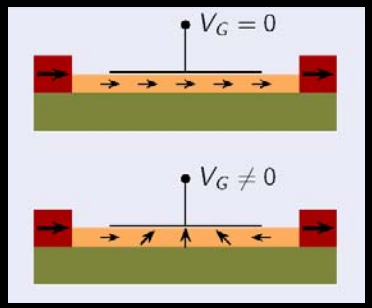




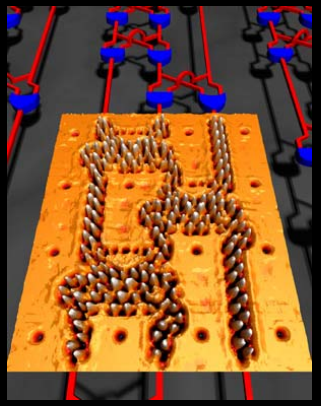


Carbon Nanotubes for FET



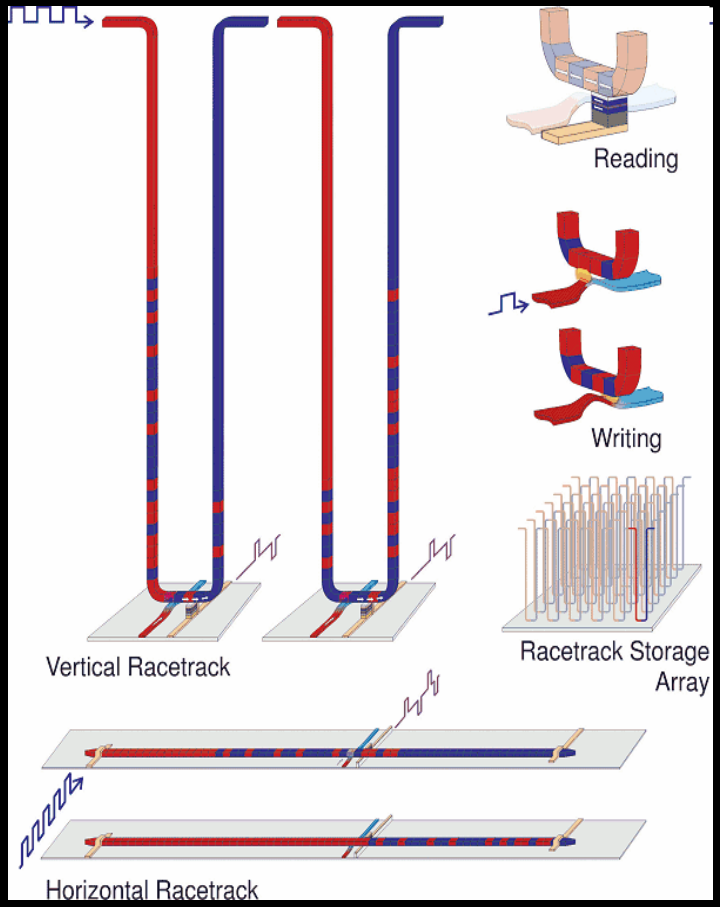


Spintronics



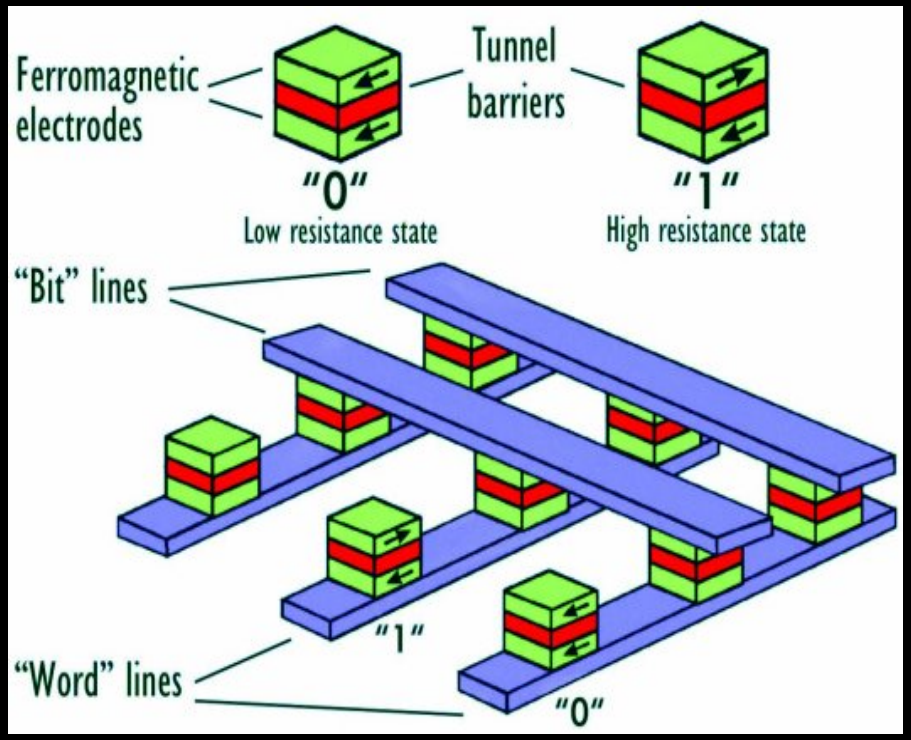
Molecular Logic

Magnetische Speicher: Racetrack und Magnetisches-RAM (MRAM)



Racetrack Memory

- store information in magnetic domain walls
- interaction of spin polarized current with magnetization in the domain walls
- current is moving across the racetrack providing the information in spin states



M-RAM

- store information in magnetization of ferromagnetic layers
- tunneling currents are dependent on parallel or antiparallel magnetization
- write access: currents exceed coercitive forces to change magnetization

I2

For nearly fifty years, scientists have explored the possibility of storing information in magnetic domain walls, which are the boundaries between magnetic regions or "domains" in magnetic materials. Until now, manipulating domain walls was expensive, complex, and used significant power to generate the fields necessary to do so. In the paper describing their milestone, "Current Controlled Magnetic Domain-Wall Nanowire Shift Register," Dr. Parkin and his team describe how this long-standing obstacle can be overcome by taking advantage of the interaction of spin polarized current with magnetization in the domain walls; this results in a spin transfer torque on the domain wall, causing it to move. The use of spin momentum transfer considerably simplifies the memory device since the current is passed directly across the domain wall without the need for any additional field generators.

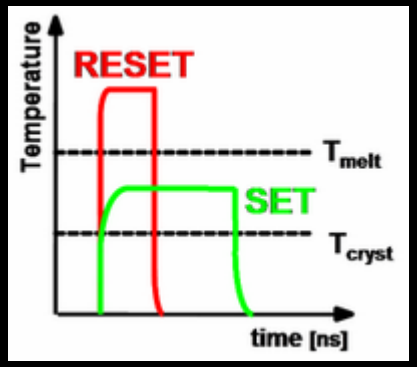
In the review paper that describes the fundamentals of racetrack, "Magnetic Domain-Wall Racetrack Memory," Dr. Parkin and colleagues describe the use of magnetic domains to store information in columns of magnetic material (the "racetracks") arranged perpendicularly or horizontally on the surface of a silicon wafer. Magnetic domain walls are then formed within the columns delineating regions magnetized in opposite directions (e.g. up or down) along a racetrack. Each domain has a "head" (positive or north pole) and a "tail" (negative or south pole). Successive domain walls along the racetrack alternate between "head to head" and "tail to tail" configurations. The spacing between consecutive domain walls (that is, the bit length) is controlled by pinning sites fabricated along the racetrack.

IBM_USER; 08.09.2009

Phase Change Memory

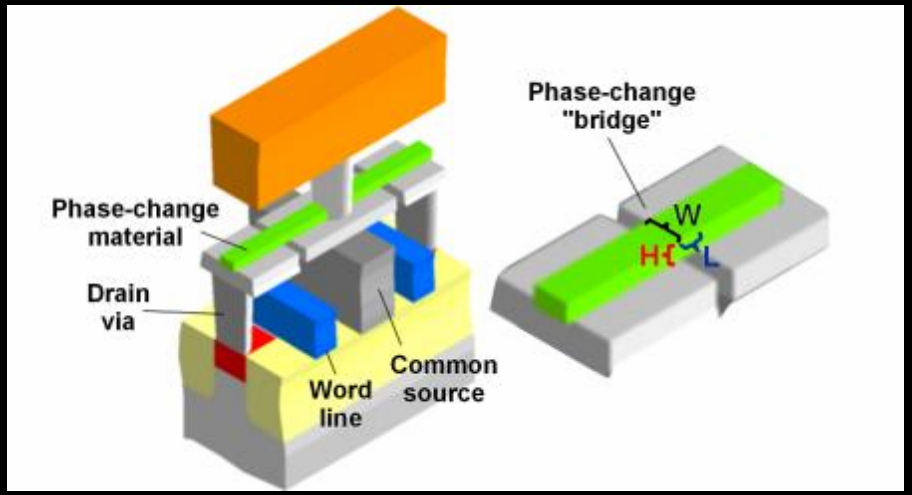
In phase change memory, data are stored by switching small regions of a "phase-change" material between one of two phases:

- a highly resistive amorphous phase, and
- a highly conductive crystalline phase.
- Switching is done by using voltage/current pulses to control time temperature within this small volume.



Phase change memory has a number of advantages as a prospective next-generation solid-state memory, including

- Solid-state memory array &
- potential for CMOS compatibility
- Large resistance contrast
- Media familiarity from CD-RW
- Inherently fast transformation



Trend: Mehrkern- und anwendungssoptimierte Systeme

Spieleprozessoren

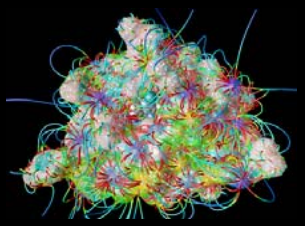
Anwendung
- Spiele
- 3D rendering

BladeCenter

Anwendung
- Netzwerk
- Data Mining
- XML
- Cell blades

Supercomputer

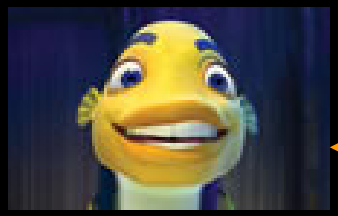
Anwendung
- Proteinfaltung
- DOE Anwendung
- Modelierung des Neocortex

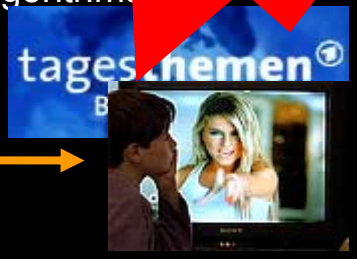


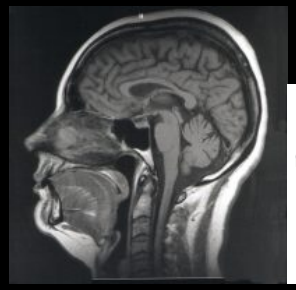
Changing Paradigmas in a Digital World/Future

- Multimedia is key! -era everywhere
  - Search engines (like Google, Inktomi)
  - extend search for document files, images, streaming media
- Natural information processing (like human brain)
  - Information wrapped in multimedia containers ➔ needs for high bandwidth and compute power
  - New killer applications: video processing and digital entertai ent
- Realistic information processi (o
- Surveillance support (i.e. Videocams on airport
- Simulation/Visualisierung: polygon modelling > rea
- Media/streaming service High bandwidth, new algorithm

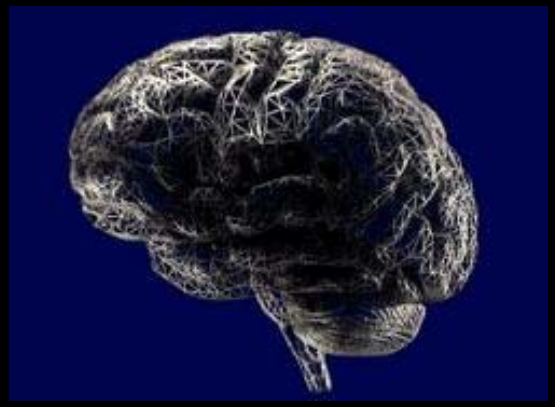
Compute power up to 10^{18} – 10^{20} FLOPs and high bandwidth needed!

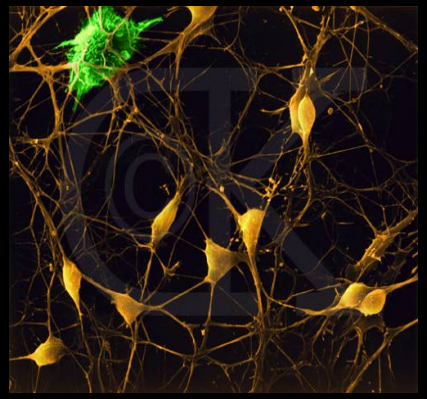






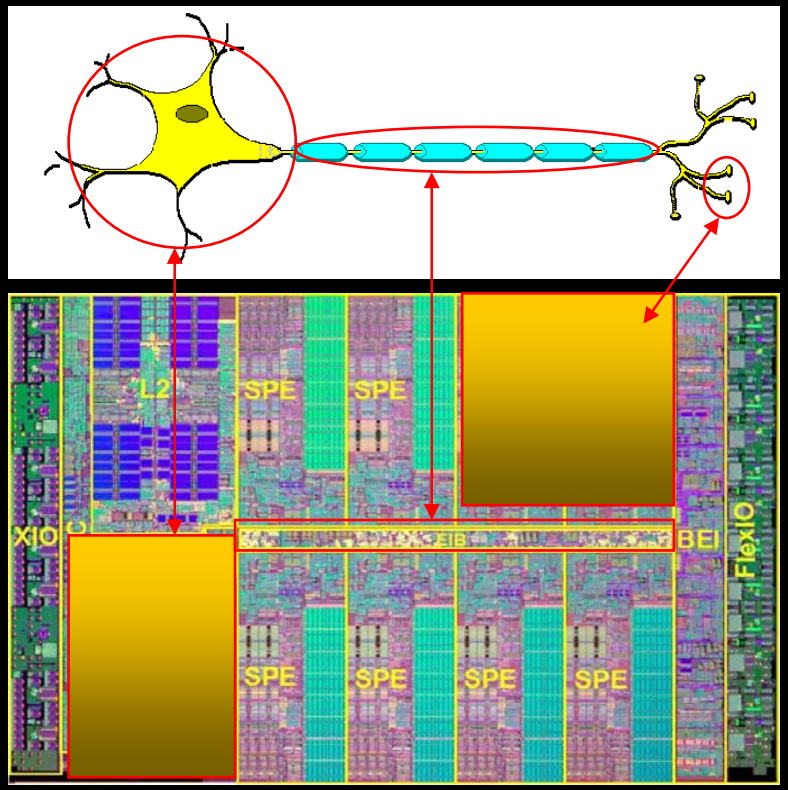
Natur als Vorbild?





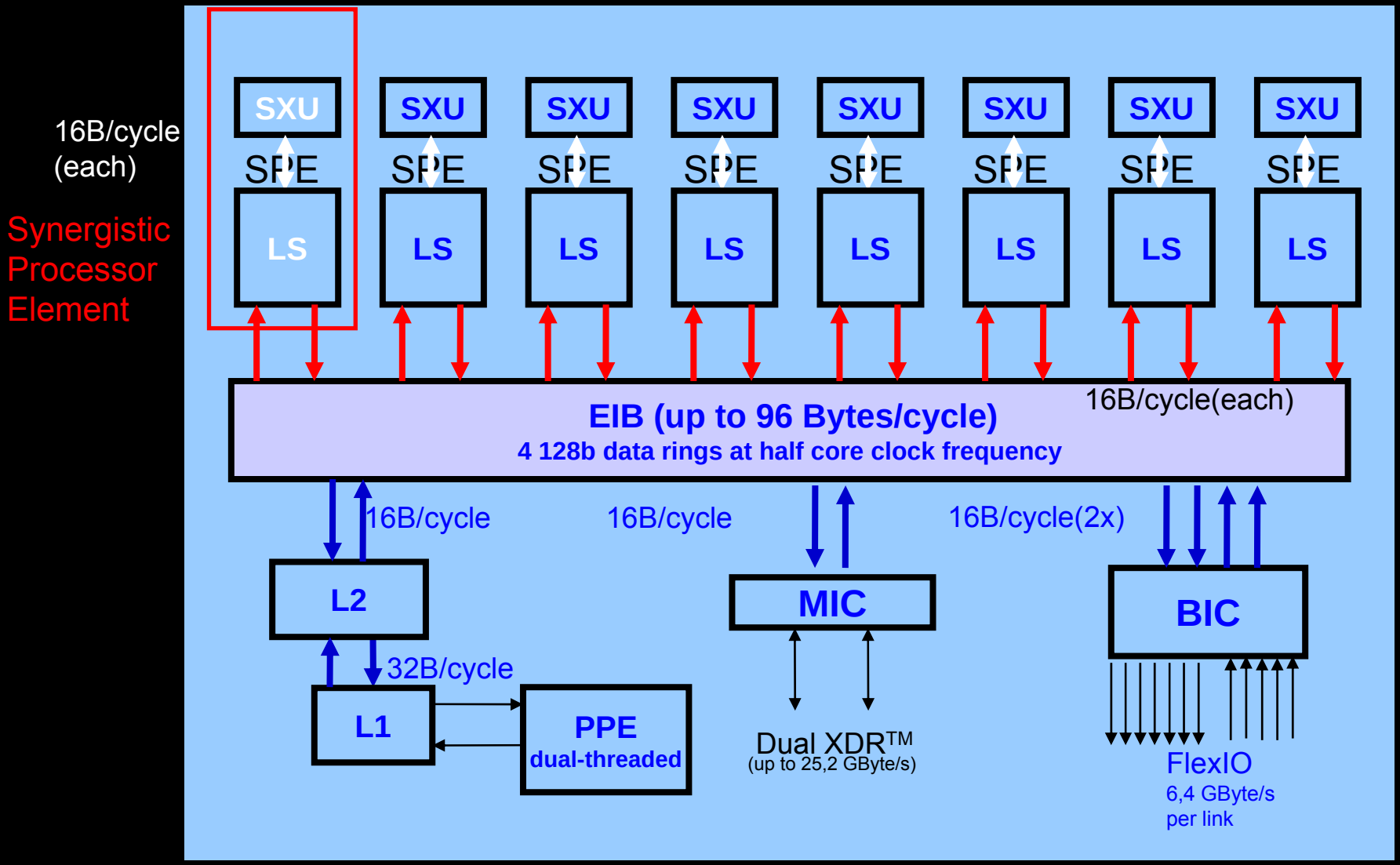
100 Milliarden Neuronen
100 Billionen Synapsen

Bis 10000 Synapsen pro Neuron

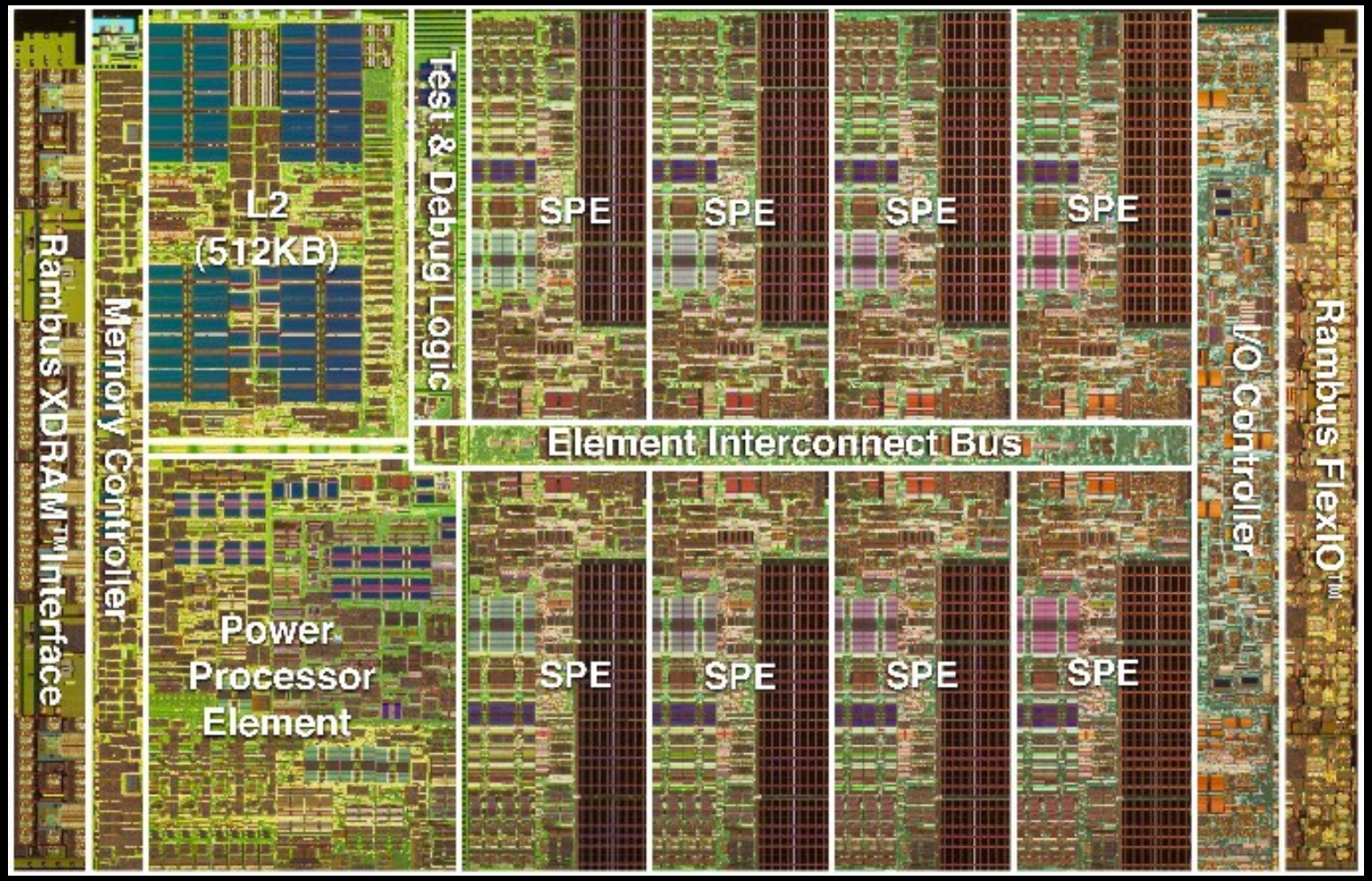


234 Millionen Transistoren
4 GHz
PowerPC + 8x Synergetisches Prozessor Element

Cell Architektur & System-Struktur



Cell Broadband Engine – 235mm²



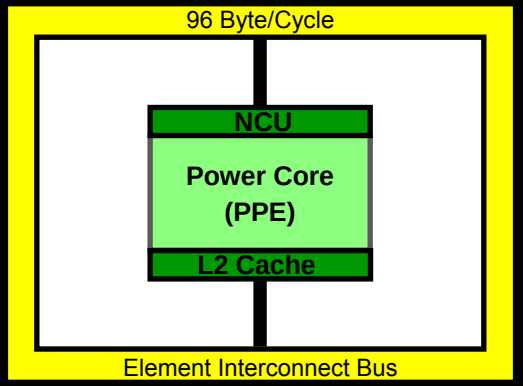
234 million transistors, 90nm SOI, 1.4 million nets, 8 levels of copper wiring

Cell Processor Components

Power Processor Element (PPE):

- General purpose, 64-bit RISC processor (PowerPC AS 2.0.2)
- 2-Way hardware multithreaded
- L1 : 32KB I ; 32KB D
- L2 : 512KB
- Coherent load / store
- VMX-32
- Realtime Controls
  - Locking L2 Cache & TLB
  - Software / hardware managed TLB
  - Bandwidth / Resource Reservation
  - Mediated Interrupts

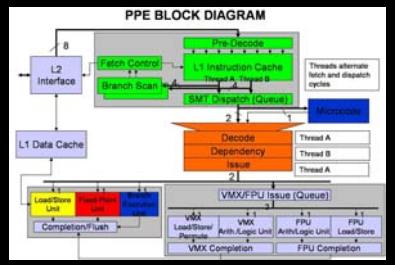
In the Beginning
– the solitary Power Processor

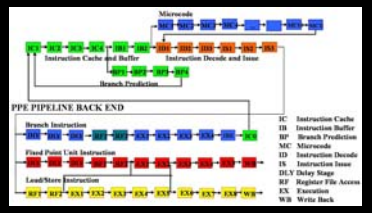


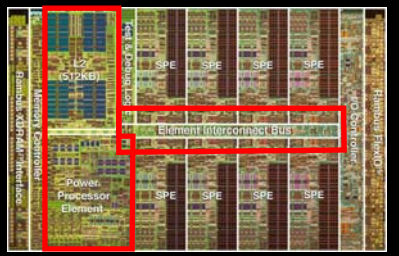
Custom Designed
– for high frequency, space, and power efficiency

Element Interconnect Bus (EIB):

- Four 16 byte data rings supporting multiple simultaneous transfers per ring
- 96Bytes/cycle peak bandwidth
- Over 100 outstanding requests





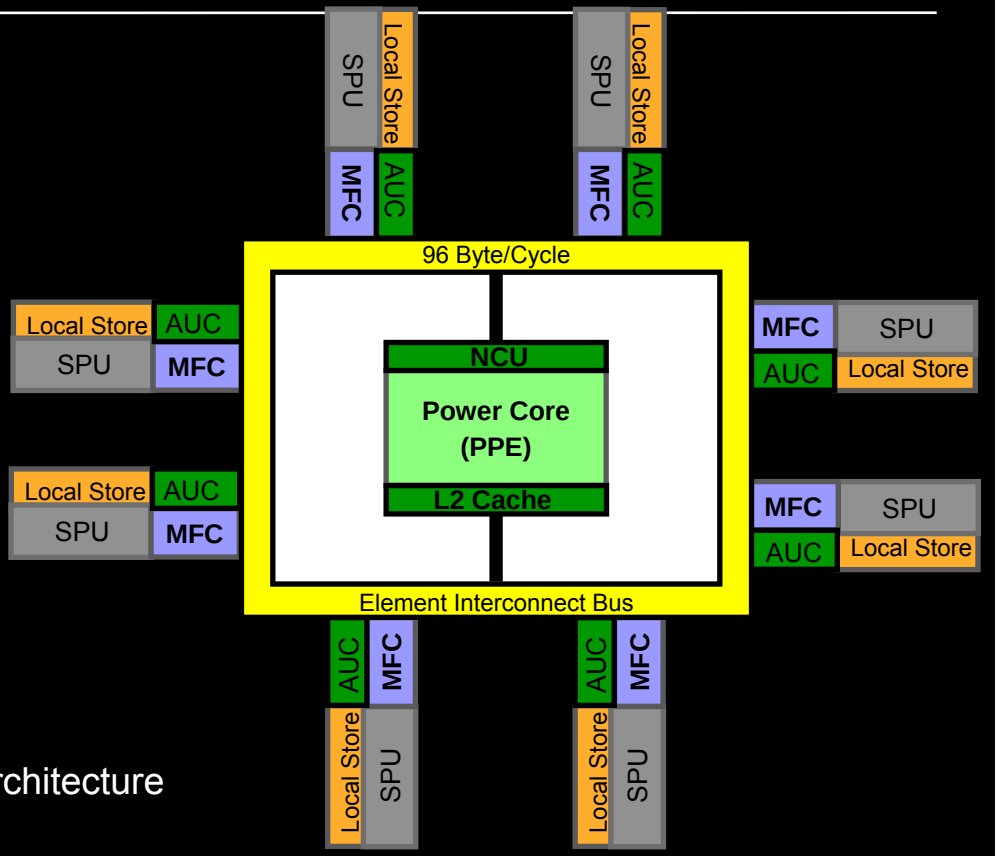


Source: „The cell processor“ J. Leenstra, IBM Entwicklung GmbH, technical talk CeBit 2006

Cell Processor Components

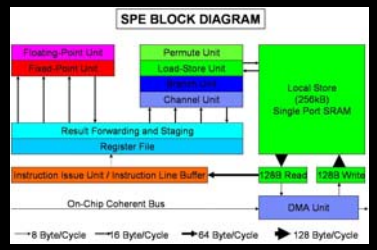
Synergistic Processor Element (SPE):

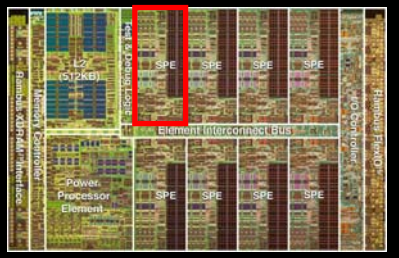
- Provides the computational performance
- Simple RISC User Mode Architecture
- Dual issue VMX-like
- Graphics SP-Float
- IEEE DP-Float
- Dedicated resources: unified 128x128-bit RF, 256KB Local Store
- Dedicated DMA engine: Up to 16 outstanding requests



Memory Management & Mapping

- SPE Local Store aliased into PPE system memory
- MFC/MMU controls / protects SPE DMA accesses
  - Compatible with PowerPC Virtual Memory Architecture
  - SW controllable using PPE MMIO
- DMA 1,2,4,8,16,128 -> 16Kbyte transfers for I/O access
- Two queues for DMA commands: Proxy & SPU





Source: „The cell processor“ J. Leenstra, IBM Entwicklung GmbH, technical talk CeBit 2006

Accellerator-Beispiel: Cell Synergistic Processor Element (SPE)

Synergistic Processor Element (SPE):

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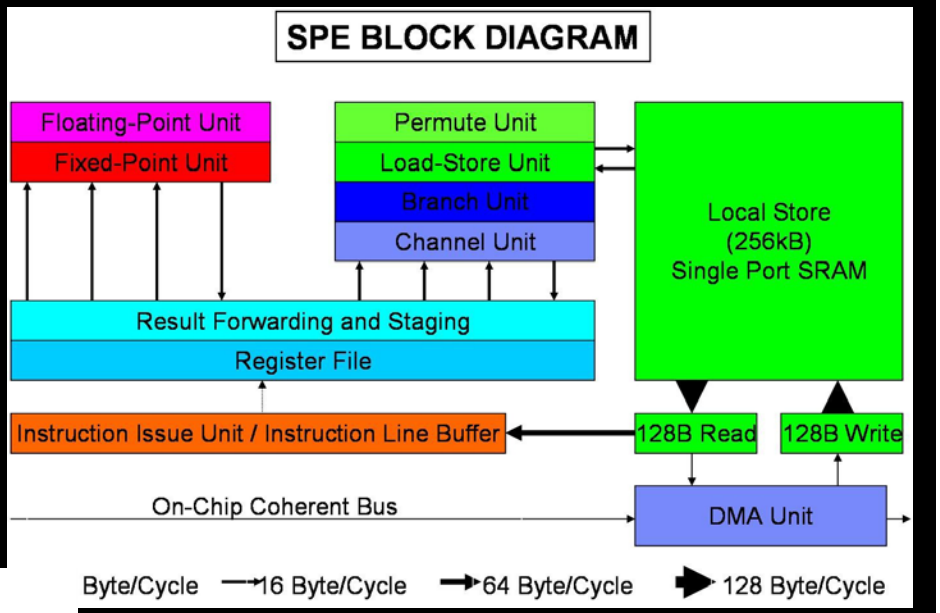
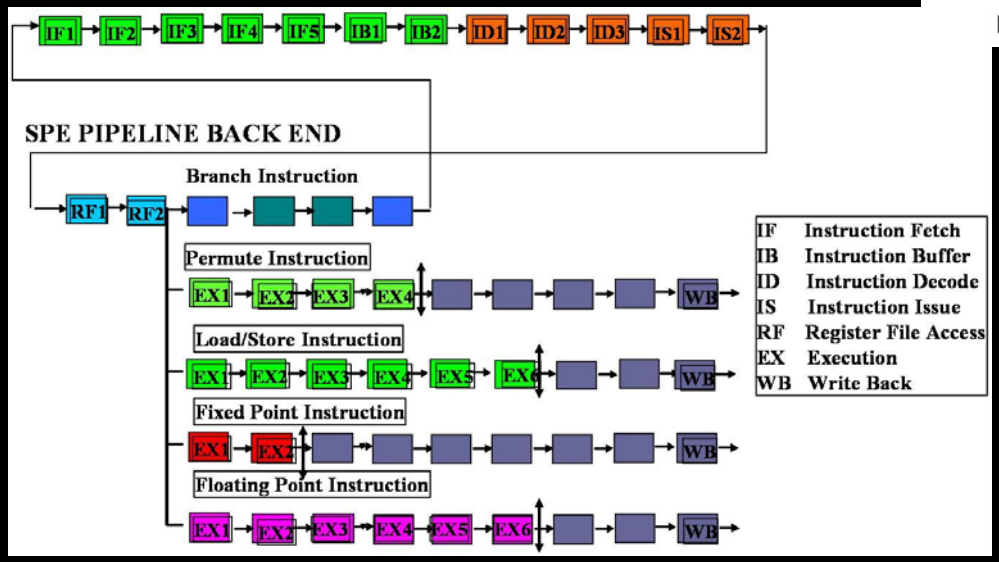
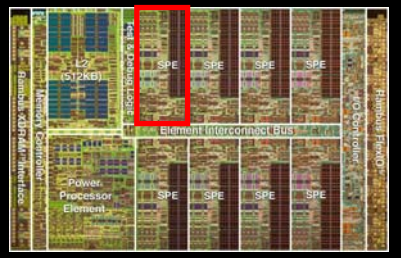


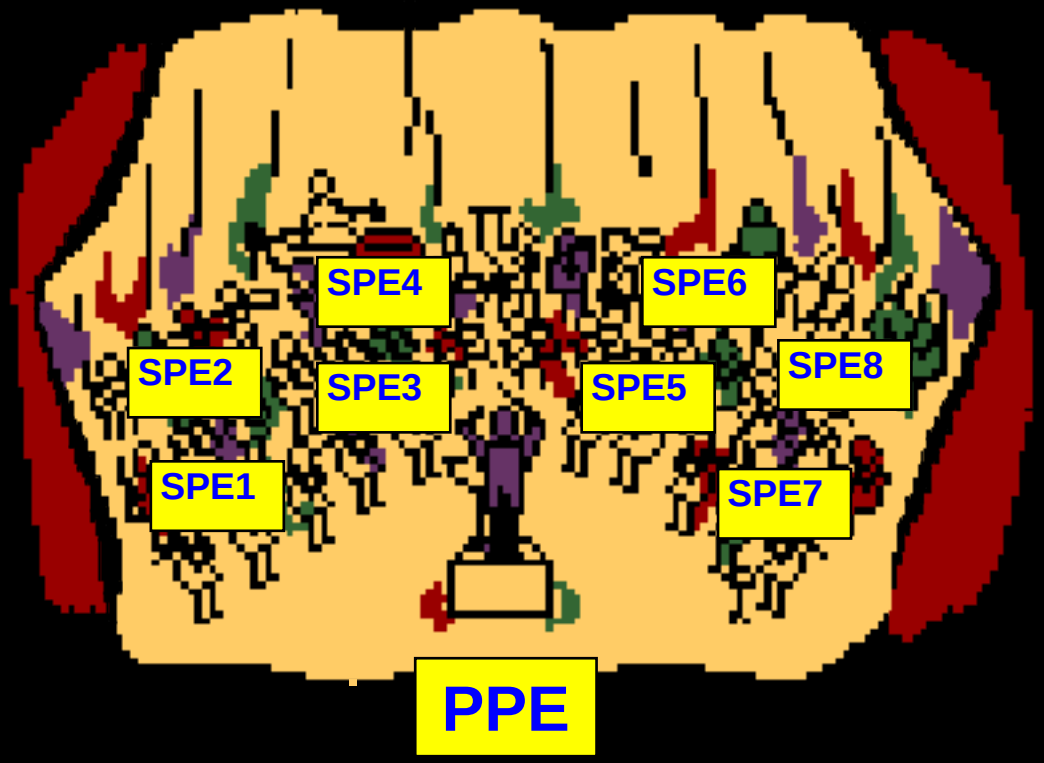




Source: „The cell processor“ J. Leenstra, IBM Entwicklung GmbH, technical talk CeBit 2006

IBM

Flexible Programmierung



Anwendungs-Programmierer

Historie der Schnellsten Supercomputer der Welt

10 billion neurons

10,000

1,000

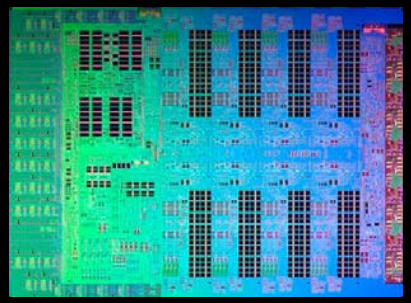
750

500

250

0

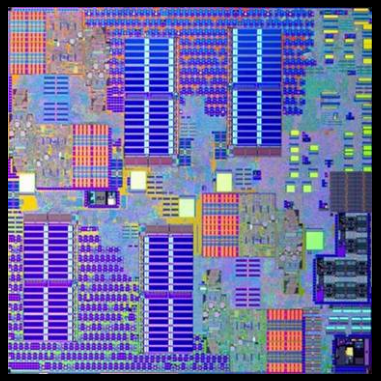
PowerXCell 8i



Enhanced Cell/B.E.
45nm lithography, 3.2 GHz

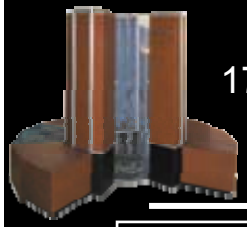
RoadRunner

BlueGene/L



Chip technology based
on standard PPC440
(700MHz BG/L) (850MHz BG/P)

Blue
Gene/L



170 MFlops

ASCI
Red

Blue
Pacific

ASCI
White

Earth
Simulator

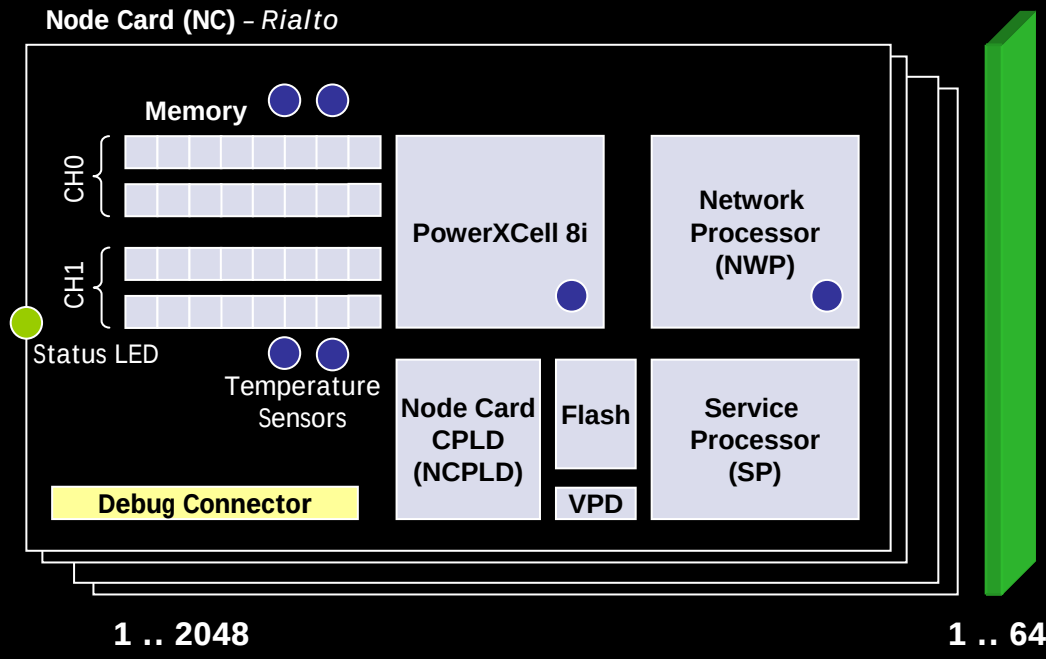
1994 1996 1998 2000 2002 2004 2006 2008 2010 ……

Sources: www.top500.org; not drawn to scale; all statements regarding IBM future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only

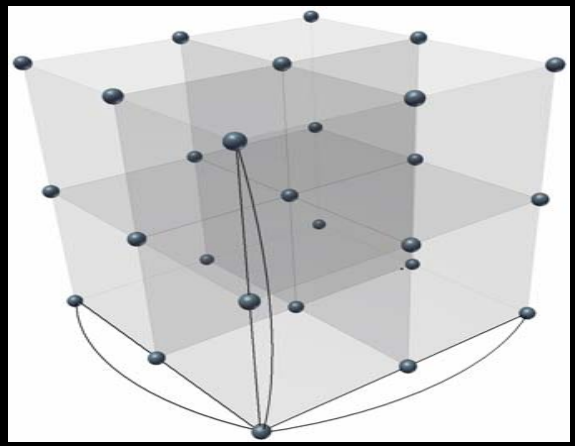
IBM

QPACE – energieeffizientestes HPC System basiert auf PowerXCell!

Quantum Chromodynamics Parallel computing on Cell

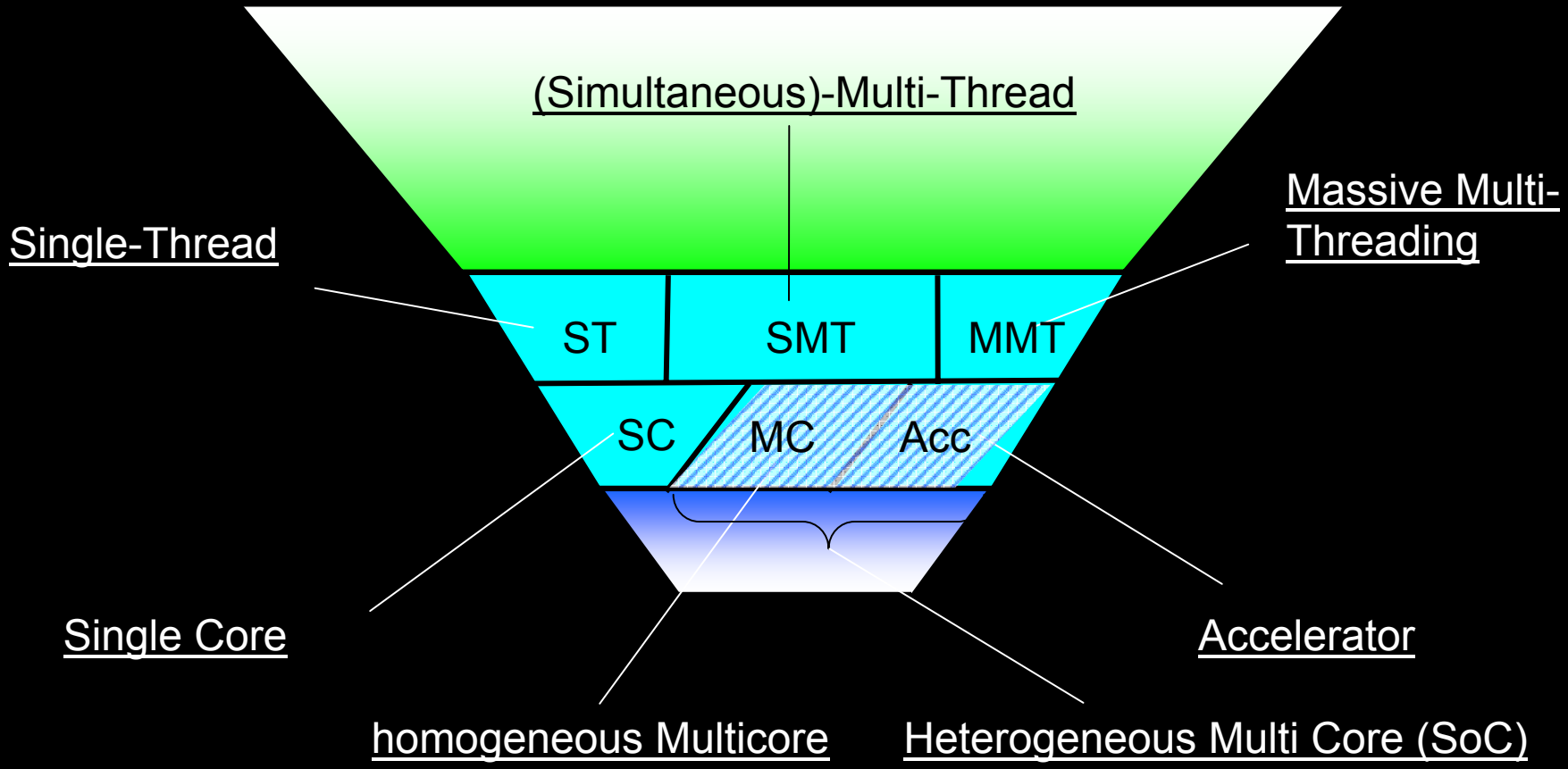


$$\psi'_x = D_h\psi \qquad (1)$$
$$= \sum_{\mu=1}^{4} \left\{ U_{x,\mu}(1+\gamma_\mu)\psi_{x+\hat{\mu}} + U^\dagger_{x-\hat{\mu},\mu}(1-\gamma_\mu)\psi_{x-\hat{\mu}} \right\} .$$

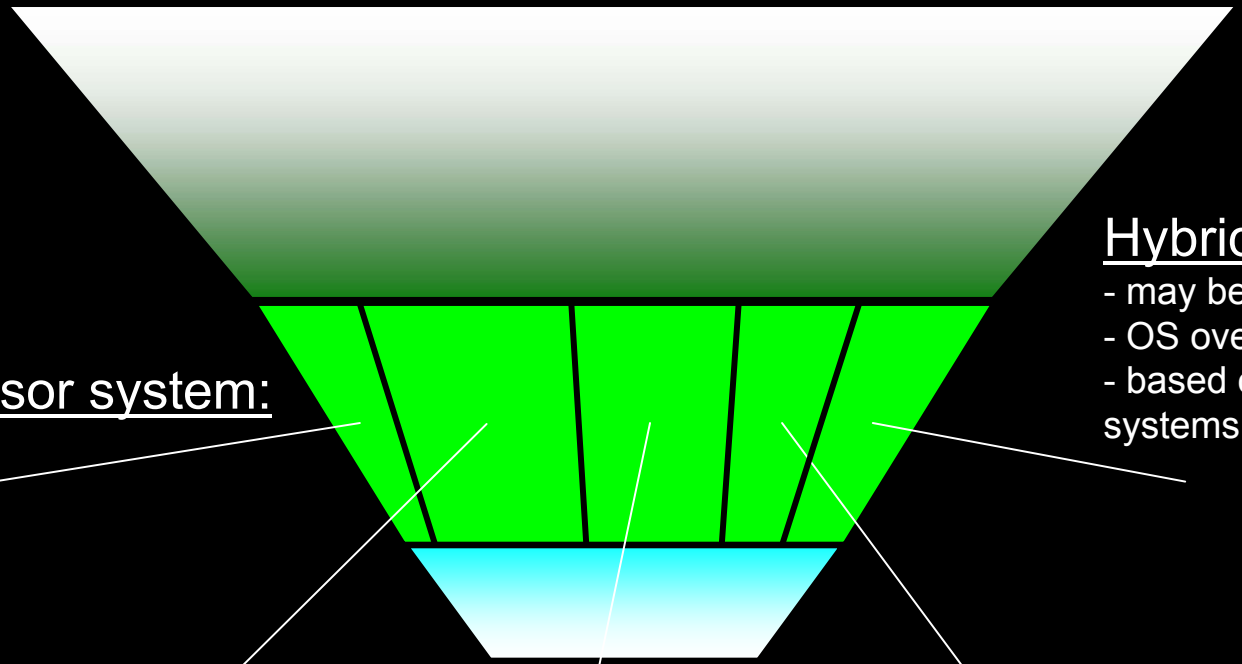


- 200 TFLOPs Spitzenleistung
- 50 TFLOPs durchgängige Rechenleistung
- Factor > 4 niedrigere Systemkosten als State-of-the-Art-Supercomputer
- Bessere Energieeffizienz als State-of-the-Art-Supercomputer (d.h. 770 MFlops/W)
- 3D Torus Topologie mit 6 nächsten Nachbarn-Anbindung der PowerXCell-Prozessoren

Trends der Prozessorarchitektur



Trends der Rechnersystem-Architektur



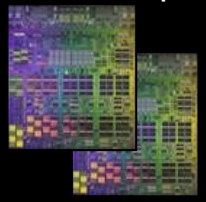
Uni processor system:

Hybrid setup:

- may be blade center based
- OS over various systems
- based on various kinds of systems

SMP system:

- single thread orientated
- superscalar structures
- classic scale-up system



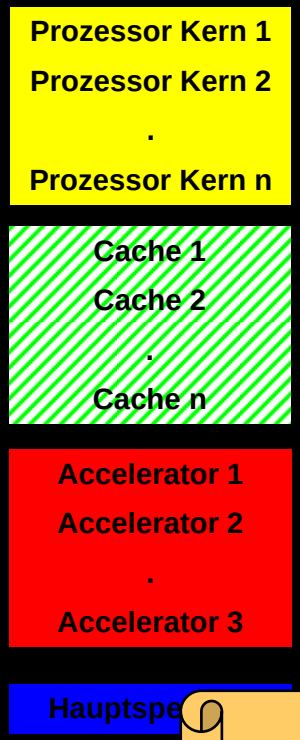
Many Core:

- still coherent memory

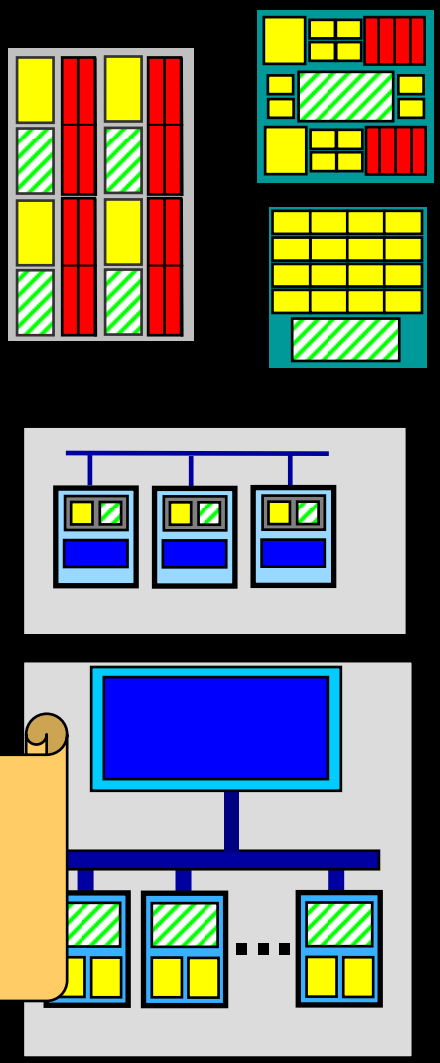
Massive Parallel cluster:

- blade center based
- several possible OS in same chip/blade
- OS-based assignment of resources

Ausblick:
Hybrid Systeme und heterogene ManyCore-Systeme

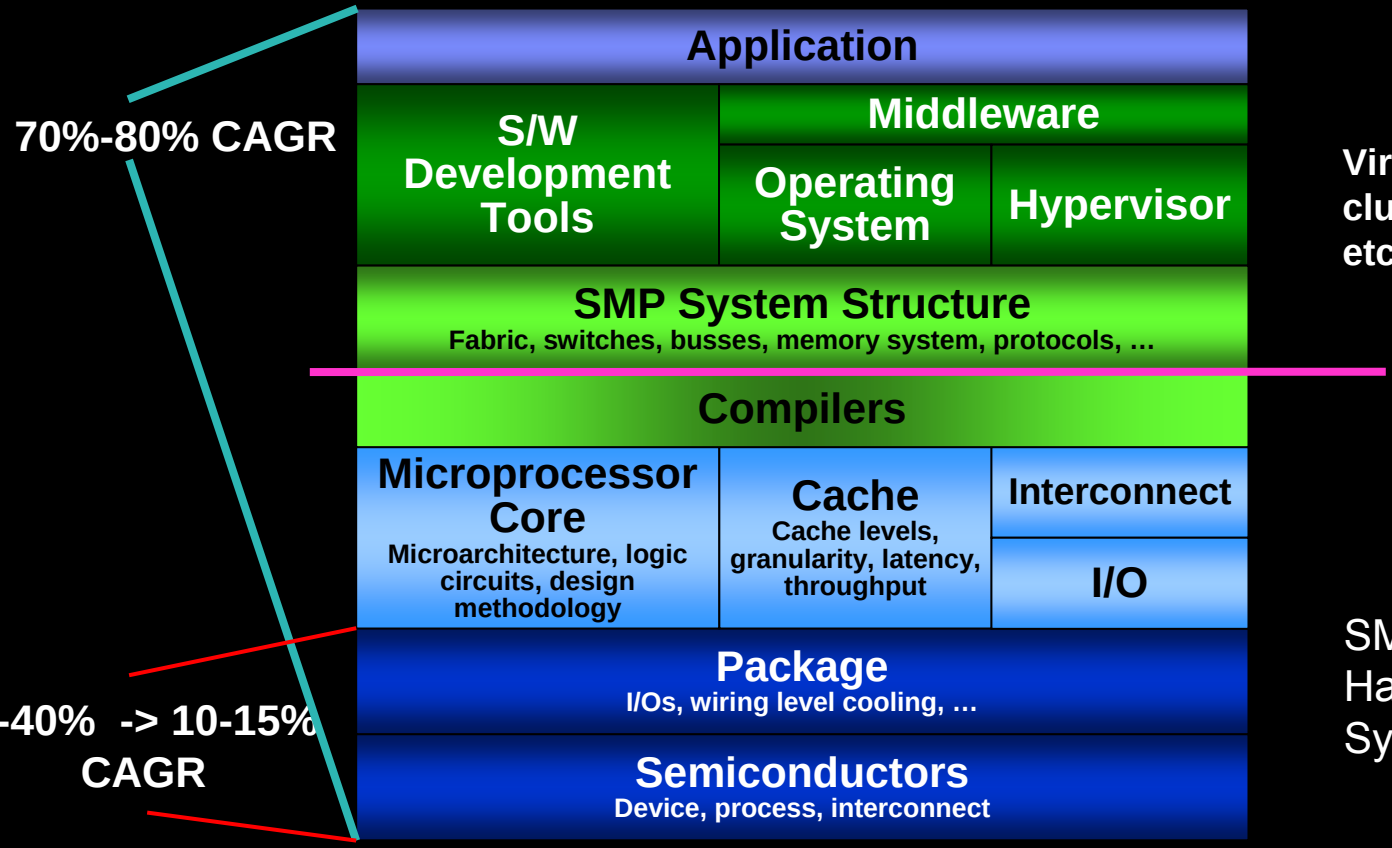


- **Parallelität (Multi-Core)**
- **Accelerator-Cores**
- **Integration (System on Chip, SoC)**
- **Modularität**
- **Software Optimierung**
- **Nanotechnologie**

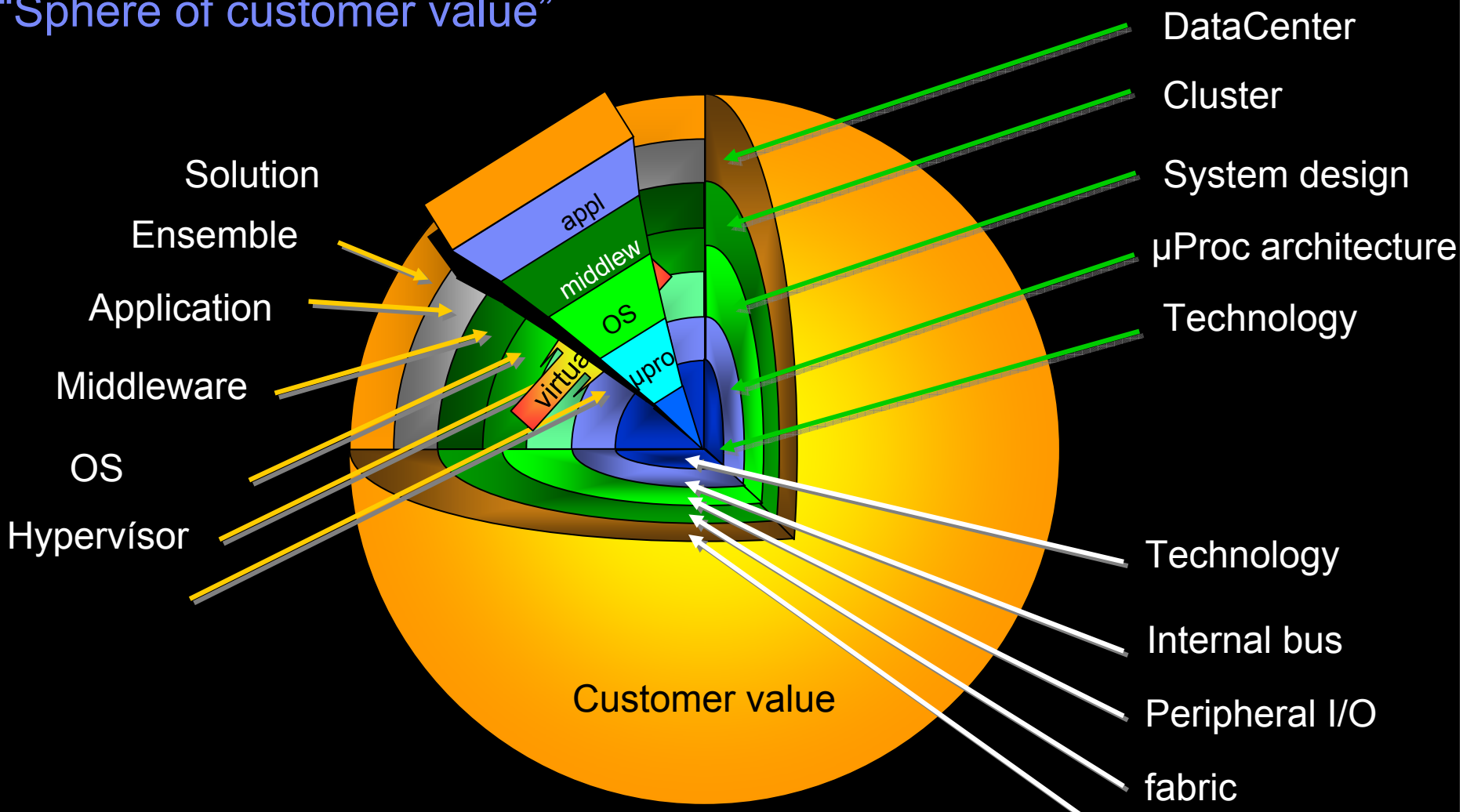


„post von Neumann“ era begins!

Vorteil IBM: System Performanz “von Atomen bis zur Anwendung”



“Sphere of customer value”



Holistischer Ansatz für energieeffiziente und performante IT-Systeme der Zukunft!

Zusammenfassung

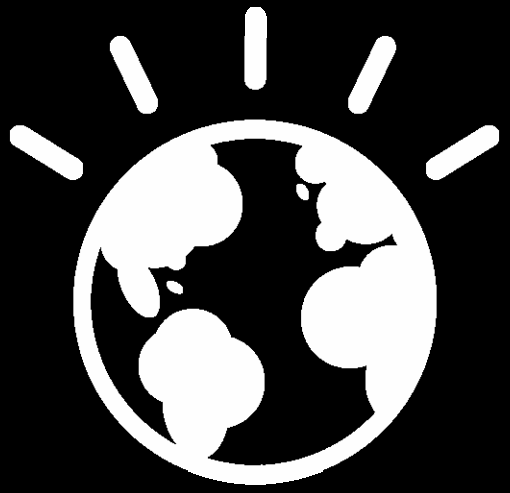
- Performanz wird dem Moore‘schen Gesetz noch den nächsten Jahren entsprechend wachsen!

- Technologie: CMOS-Ablöse ist noch nicht in Sicht!
  - Einsatz neuer Materialien im Frontend (Transistoren) und Backend (Leitungen), neue Transistorgeometrien und –strukturen
  - Skalierung zu Strukturen im Bereich < 25 nm durch neue Techniken
  - Neue Speichertechniken! Magnetische Speicher und PhaseChange-Memory?

- Signifikante technische Herausforderungen
  - Manufacturing Defects, Yield
    - Extreme hohe DC- und AC-Fehlerabdeckung in Kombination mit “on-speed” -Selbsttests
  - “Soft Errors” und Recovery
    - “On-line”-Erkennung von Soft Errors wird wichtiger denn je!
    - Recovery/Availability beginnt mit Fehlererkennung (Error detection)!
  - Power Density, Energiedichte
    - Aufwendigere Techniken zur Reduzierung des Energieumsatzes, bzw Energiedichte

- Mikro-Architektur/System-Architektur
  - Rethinking paradigms!
  - Hohe Pipelinetiefe und hohe Taktgechwindigkeit ODER hohe Instruktions-Parallelität mit Multicore-Technikenpipeline,
  - Systemperformanz durch hybride Rechnerarchitekturen UND/ODER heterogene Multicore-Prozessoren

Vielen Dank!



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Publicly Available Information

- Introduction to the Cell Broadband Engine White Paper
- Cell Broadband Engine Public Registers Guide (subset of CDA version)
- Cell Broadband Engine Linux Reference Implementation Application Binary Interface Specification
- SPU C/C++ Language Extensions Software Reference Manual
- SPU Application Binary Interface Specifications
- SPU Assembly Language Specifications
- Broadband Engine Linux Application Binary Interface Specification
- Cell Broadband Engine SDK Libraries, Overview and User's Guide
- Cell Broadband Engine Architecture
- Cell Broadband Engine Datasheet
- SPU Instruction Set Architecture Specifications
- Cell Broadband Engine Processor Full System Simulator
- XLC Alpha Edition for Cell Broadband Engine
- IBM Cell Broadband Engine Software Sample and Library Source Code
- GCC Toolchain for Cell Broadband Engine
- Cell Broadband Engine SPE Management Library
- Linux Kernel patch for Cell Broadband Engine
- SDK Installation script

- Introduction to the Cell Microprocessor, Article
- A 4.8GHz Fully Pipelined Embedded SRAM in the Streaming Processor of a Cell Processor, Article
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