PowerPC™

Preliminary

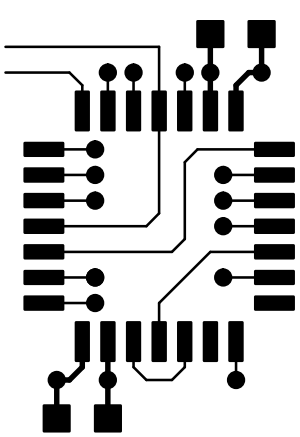
The 660 Bridge FAQ – 4/11/96

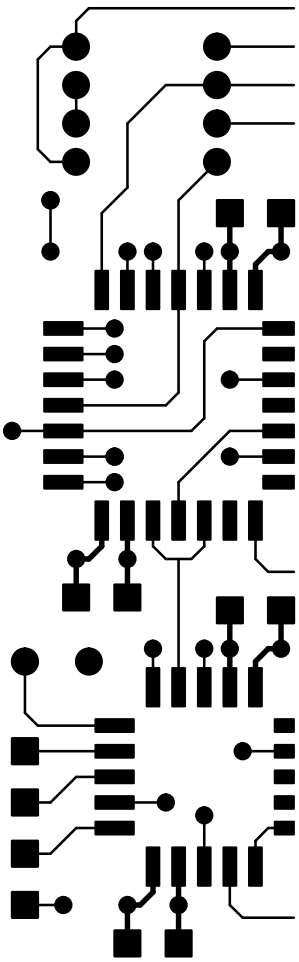
Frequently Asked Questions about the IBM27-82660 PowerPC to PCI Bridge and Memory Controller. This is a living document, which was last updated on the date shown in the title.

Application Note AN-PPC-011

This FAQ contains 660 bridge information which the PowerPC Application Engineering team believes to be of interest to the PowerPC community, and which are too short to be the subject of individual application notes.

MPRA11APU-01
Dale Elson





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The 660 Bridge FAQ – 4/11/96

Dale Elson

In this document, the IBM27-82660 is referred to as the 660 bridge or the 660. Likewise, the IBM27-82663 and IBM27-82664 are referred to as the 663 and the 664. The *IBM27-82660 PowerPC to PCI Bridge User's Manual* (MPR660UMU–02) is often referred to as the 660UM.

1) Where can I get 660 information ?
2) What are the access times for 50ns, 60ns, & 70ns EDO DRAM ?
3) Can the 660 address and data buses be left tristated ?
4) Is my DRAM fast enough to do 660 RMW cycles in ECC mode ?
5) How do interrupt acknowledge cycles work ?

1 Where can I get 660 information ?

Date 4/9/96

Description . . Currently, 660 data is located in several places. IBM employes (such as your FAE or other IBM technical representative) can access this information using the addresses marked *Internal*. This information can be accessed externally using the other addresses.

660 Bridge – User's Manual and other information.

Internal . . . . . /afs/awd/work/PowerPC/support_chips/660_bridge/
. . . . . From AIX, rftp ftp.austin.ibm.com/pub/PPC_support/660_bridge
External . . . . . ftp://ftp.austin.ibm.com/pub/PPC_support/660_bridge/
. . . . . the IP address is (192.35.232.38)

Reference Designs – Technical Specifications and design files showing how to use the 660 and other PowerPC products.

Internal . . . . . /afs/awd/work/PowerPC/reference_designs/
. . . . . From AIX, rftp ftp.austin.ibm.com/pub/PPC_support/reference_designs
External . . . . . ftp://ftp.austin.ibm.com/pub/PPC_support/reference_designs/
. . . . . the IP address is (192.35.232.38)

Application Notes – Technical articles from the PowerPC Application Engineering team about the 660 and other PowerPC products.

Internal . . . . . /afs/awd/work/PowerPC/app_notes/
. . . . . From AIX, rftp ftp.austin.ibm.com/pub/PPC_support/app_notes
External . . . . . ftp://ftp.austin.ibm.com/pub/PPC_support/app_notes/
. . . . . the IP address is (192.35.232.38)

2 What are the access times for 50ns, 60ns, & 70ns EDO DRAM ?

Date 4/9/96

Description . . Additional access times are now available for 50ns, 60ns, and 70ns EDO DRAM (see Table 1 and Table 2). These timings are presented in the same manner as the ones in Section 5 of the 660UM. Notice that the column in Table 2 for 60ns aggressive timing corrects an error in some copies of the 660 UM.

Table 1. General Case EDO DRAM Timing Summary

Transfer	70ns EDO Conservative	70ns EDO Aggressive	60ns EDO Conservative	Note
Memory Timing Register 1	32	32	31	
Memory Timing Register 2	0A	06	06	
Bridge Chipset Options 3	0C	0C	0C	
Initial Read Burst	12-4-4-4	11-3-3-3	11-3-3-3	(3)
Initial Write Burst	5-4-4-4	5-4-3-3	5-4-3-3	
For a pipelined burst transfer immediately following a read:				
Page Hit Read	-5-4-4-4	-5-3-3-3	-5-3-3-3	(3)
Page Hit Write	-3-3-4-4	-3-3-3-3	-3-3-3-3	
Page Miss & Bank Miss Read	-9-4-4-4	-8-3-3-3	-8-3-3-3	(1,3)
Page Miss & Bank Hit Read	-11-3-3-3	-10-3-3-3	-9-3-3-3	(2,3)
Page Miss & Bank Miss Write	-3-3-4-4	-3-3-3-3	-3-3-3-3	(1)
Page Miss & Bank Hit Write	-3-5-4-4	-3-5-3-3	-3-4-3-3	(2)
For a pipelined burst transfer immediately following a write:				
Page Hit Read	-12-4-4-4	-9-3-3-3	-9-3-3-3	(3)
Page Hit Write	-6-3-4-4	-5-3-3-3	-5-3-3-3	
Page Miss & Bank Miss Read	-15-4-4-4	-12-3-3-3	-12-3-3-3	(1,3)
Page Miss & Bank Hit Read	-17-4-4-4	-14-3-3-3	-13-3-3-3	(2,3)
Page Miss & Bank Miss Write	-6-6-4-4	-5-5-3-3	-5-5-3-3	(1)
Page Miss & Bank Hit Write	-6-8-4-4	-5-7-3-3	-5-6-3-3	(2)

See the notes for Table 2.

Table 2. General Case EDO DRAM Timing Summary

Transfer	60ns EDO Aggressive	50ns EDO Conservative	50ns EDO Aggressive	Note
Memory Timing Register 1	11	0C	2C	
Memory Timing Register 2	05	05	02	
Bridge Chipset Options 3	0C	0C	0C	
Initial Read Burst	10-3-3-3	10-3-3-3	10-2-2-2	(3)
Initial Write Burst	5-3-3-3	5-3-3-3	5-4-2-2	
For a pipelined burst transfer immediately following a read:				
Page Hit Read	-5-3-3-3	-5-3-3-3	-5-2-2-2	(3)
Page Hit Write	-3-3-3-3	-3-3-3-3	-3-2-2-2	
Page Miss & Bank Miss Read	-7-3-3-3	-7-3-3-3	-7-2-2-2	(1,3)
Page Miss & Bank Hit Read	-8-3-3-3	-7-3-3-3	-7-2-2-2	(2,3)
Page Miss & Bank Miss Write	-3-3-3-3	-3-3-3-3	-3-3-2-2	(1)
Page Miss & Bank Hit Write	-3-3-3-3	-3-3-3-3	-3-3-2-2	(2)
For a pipelined burst transfer immediately following a write:				
Page Hit Read	-9-3-3-3	-9-3-3-3	-7-2-2-2	(3)
Page Hit Write	-5-3-3-3	-5-3-3-3	-4-2-2-2	
Page Miss & Bank Miss Read	-11-3-3-3	-11-3-3-3	-10-2-2-2	(1,3)
Page Miss & Bank Hit Read	-12-3-3-3	-11-3-3-3	-10-2-2-2	(2,3)
Page Miss & Bank Miss Write	-5-4-3-3	-5-4-3-3	-4-5-2-2	(1)
Page Miss & Bank Hit Write	-5-5-3-3	-5-4-3-3	-4-5-2-2	(2)

1) The RAS# of the new bank is high and has been high (precharging) for the minimum RAS# high time. The bridge places the address on the address lines and asserts RAS#.
2) The access is a page miss, but within the same bank, so the RAS# line must be sent high for at least the minimum RAS# high (precharge) time. The bridge also places the new address on the address lines and asserts RAS#.
3) If asynchronous SRAMs are used with the internal L2 controller, an additional clock cycle is added to the fourth beat of any CPU to memory read burst that causes a cache miss. For example, following a read—a pipelined page hit, cache miss, burst read with EDO DRAM, requires –3–3–3–3 CPU clocks when the L2 uses burst SRAMs and –3–3–3–4 CPU clocks when the L2 uses asynchronous SRAMs. This extra beat is caused by delaying the final TA# by one CPU_CLK to allow the asynchronous SRAM sufficient data hold time for the fourth beat.

3 Can the 660 address and data buses be left tristated ?

Date 4/9/96

Description . . We have not seen any functional problems with the 660 which have been caused by allowing CPU_ADDR[0:31] and CPU_DATA[0:63] to float for an extended amount of time (several seconds).

However, the 660 is a CMOS device, so allowing the inputs to float allows the possibility that the input voltage will float to a level that causes both of the input transistors to conduct some current, thus increasing the power dissipation of these inputs. A more remote possibility is that these inputs will oscillate, which will also increase the power dissipation of the inputs without causing functional problems. As with all electrical devices, system level and handling

precautions should be taken to ensure that the 660 is not exposed to ESD events in excess of its published protection limits.

4 Is my DRAM fast enough to do 660 RMW cycles in ECC mode ?

Date 4/9/96

Description . . In ECC mode, the 660 can do a read–modify–write cycle to the DRAM if the CPU or a PCI bus-master initiates a memory write of less than 8 bytes.

As shown in Section A.7.5 of the 660UM, when the 660 does a RMW cycle, it does not use the RMW cycle capability that is built into some DRAMs. Instead, it does a read, modifies the data, and then writes back the data (as a pipelined page hit write). This allows RMW cycles with any DRAM that is fast enough to perform read cycles and write cycles. No recalculation of the CAS# pulse width is required.

5 How do interrupt acknowledge cycles work ?

Date 4/11/96

Description . . To perform an interrupt acknowledge operation, the CPU initiates a single-byte read to address BFFF FFF0. This causes the 660 to arbitrate for the PCI bus and then to initiate a single-byte PCI Interrupt Acknowledge transaction with PCI_C/BE[0]# active. PCI_C/BE[0]# is active regardless of the endian mode of the 660. The PCI Interrupt Acknowledge transaction that the 660 generates is similar to those generated by x86 to PCI bridges. The interrupt controller (eg SIO) then claims the transaction and supplies the single-byte interrupt vector on PCI byte lane 0. The 660 then returns the vector to the CPU on the correct byte lane.

There is no physical interrupt vector BCR in the bridge. Other PCI bus masters can initiate interrupt acknowledge transactions.

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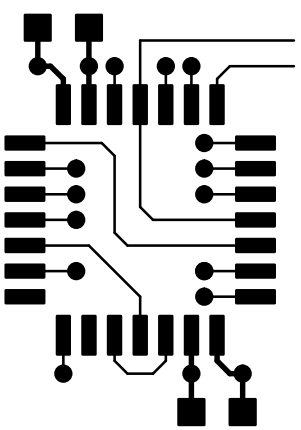
ftp://ftp.austin.ibm.com/pub/PPC_support



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