PowerPC™

IBM27-82660 Revision 2.1 Product Update

MPR660ESU-04

This document describes improvements to the IBM27-82660 Bridge from revision 1.0 to revision 2.0, and corrects an error in the revision 2.0 Product Update.

October 30, 1995

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Document Revision History

Errata Summary release 1.0 (April 19, 1995) [MPR660ESU-00]
Errata for the 1.0 revision of the chipset.

Errata Summary release 1.2 (April 19, 1995) [MPR660ESU-03]
Errata for IBM27–82664 revision 1.1 and IBM27–82663 revisions 1.0 and 2.0.

IBM27-82660 Revision 2.0 Product Update (June 5, 1995) [MPR660ESU-01]
Information on improvements to the chipset design from revision 1.0 to revision 2.0.

IBM27-82660 Revision 2.1 Product Update (October 30, 1995) [MPR660ESU-04]
Corrected information on improvements to the chipset design from revision 1.0 to revision 2.0.

Part Identification, IBM27-82660 Chipset

IBM27-82663 (663 Buffer)
Chipset Rev. 1.0 contains IBM27-82663 Rev. 1.0. The package is marked 94G0235.

Chipset Rev. 2.0 contains IBM27-82663 Rev. 2.0. The package is marked 94G0178.

IBM27-82664 (664 Controller)
Chipset Rev. 1.0 contains IBM27-82664 Rev. 1.0. The package is marked 94G0232.

Chipset Rev. 2.0 contains IBM27-82664 Rev. 1.1. The package is marked 94G0176.

IBM27-82660 Revision 2.1 Product Update

October 30, 1995

This document describes improvements to the IBM27-82660 Bridge from revision 1.0 to revision 2.0, and corrects an error in the revision 2.0 Product Update.

Revision 1.0 of the 660 Bridge is described by a combination of three documents:

- *The IBM 27-82660 PowerPC to PCI Bridge User's Manual*, MPR660UMU-01 (beta version)
- *A System Implementation Example for the IBM 82660 Chipset (Preliminary)* schematic set, attached to the User's Manual
- The *IBM27-82660 Revision 1.0 Errata Summary*, MPR660ESU-00, or the most current 1.x revision.

Between revisions 1.0 and 2.0 of the 660 Bridge, several changes were implemented:

1. All known revision 1.0 errata were designed out. All external logic workarounds that were required to fix revision 1.0 errata were eliminated.
2. Two signal connections were added to the chipset. DBG# was added to the 664 Controller. PCI_TRDY# was added to the 663 Buffer.
3. The entire pinout of the 663 Buffer was rearranged.
4. The example implementation of the 663 Buffer was changed to enhance signal to noise ratio.

Revision 2.0 of the 660 Bridge is also described by a combination of four documents:

1. *The IBM 27-82660 PowerPC to PCI Bridge User's Manual*, MPR660UMU-01 (beta version)
2. The *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set, attached to the User's Manual
3. This document, the *IBM27–82660 Revision 2.1 Product Update*
4. The most current version of the revision 2.x Errata Summary.

1 All Known Revision 1.0 Errata Designed Out

All external logic that was required as a workaround for the revision 1.0 chipset has been eliminated. Except as noted herein, all of the workarounds should be removed from the design, and the 660 Bridge incorporated in the design as shown in the *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set.

2 Signals Added to the Chipset

DBG# was added to the 664 Controller to support a 604 in fast L2 mode. This change is documented in the MPR660UMU-01 release of the 660 Bridge User's Manual, and is noted here for completeness. See the 660 User's Manual for more information.

PCI_TRDY# was connected to the 663 Buffer to improve performance.

3 663 Buffer Pinout Rearranged

The pinout of the 663 Buffer was rearranged to reduce ground bounce effects by distributing simultaneously switched signals more evenly around the perimeter of the device. Previously, signal groups that were logically grouped were also grouped together physically. Redistributing these I/O more evenly has the effect of more evenly distributing the instantaneous current drawn from the power pins. This more even distribution of the current draw also evens out the instantaneous voltage drop experienced by the device during simultaneous switching events.

Note that the previous version of this document (revision 2.0) incorrectly showed the MEM_CHECK[0:7] pins in reversed order.

3.1 New 663 Buffer Numeric Pin List

Pin	663 Signal Name	Pin	663 Signal Name	Pin	663 Signal Name
1	CPU_DATA[22]	50	PCI_AD[26]	99	CPU_DATA[49]
2	CPU_DATA[23]	51	PCI_AD[27]	100	MEM_DATA[45]
3	CPU_DPAR[2]	52	V_{DD}	101	MEM_DATA[46]
4	CPU_DATA[24]	53	GND	102	MEM_DATA[47]
5	MEM_DATA[24]	54	CPU_DATA[32]	103	MEM_CHECK[2]
6	MEM_DATA[25]	55	CPU_DATA[33]	104	CPU_DATA[50]
7	MEM_DATA[26]	56	CPU_DATA[34]	105	CPU_DATA[51]
8	V_{DD}	57	CPU_DATA[35]	106	CPU_DATA[52]
9	GND	58	MEM_DATA[32]	107	CPU_DATA[53]
10	PCI_AD[04]	59	MEM_DATA[33]	108	MEM_DATA[48]
11	PCI_AD[05]	60	MEM_DATA[34]	109	MEM_DATA[49]
12	PCI_AD[06]	61	V_{DD}	110	V_{DD}
13	PCI_AD[07]	62	PCI_AD[28]	111	MEM_DATA[50]
14	PCI_AD[08]	63	PCI_AD[29]	112	MEM_DATA[51]
15	PCI_AD[09]	64	PCI_AD[30]	113	MEM_DATA[52]
16	PCI_AD[10]	65	PCI_AD[31]	114	CPU_DATA[54]
17	PCI_AD[11]	66	GND	115	CPU_DATA[55]
18	PCI_AD[12]	67	CPU_DATA[36]	116	CPU_DPAR[6]
19	PCI_AD[13]	68	CPU_DATA[37]	117	CPU_DATA[56]
20	PCI_AD[14]	69	CPU_DATA[38]	118	MEM_DATA[53]
21	PCI_AD[15]	70	CPU_DATA[39]	119	MEM_DATA[54]
22	V_{DD}	71	GND	120	GND
23	GND	72	V_{DD}	121	MEM_DATA[55]
24	CPU_DATA[25]	73	MEM_DATA[35]	122	MEM_CHECK[1]
25	CPU_DATA[26]	74	MEM_DATA[36]	123	MEM_DATA[56]
26	CPU_DATA[27]	75	MEM_DATA[37]	124	CPU_DATA[57]
27	CPU_DATA[28]	76	MEM_DATA[38]	125	CPU_DATA[58]
28	MEM_DATA[27]	77	CPU_DPAR[4]	126	CPU_DATA[59]
29	MEM_DATA[28]	78	CPU_DATA[40]	127	CPU_DATA[60]
30	MEM_DATA[29]	79	CPU_DATA[41]	128	V_{DD}
31	CPU_DATA[29]	80	CPU_DATA[42]	129	GND
32	CPU_DATA[30]	81	MEM_DATA[39]	130	MEM_DATA[57]
33	CPU_DATA[31]	82	MEM_CHECK[3]	131	MEM_DATA[58]
34	CPU_DPAR[3]	83	MEM_DATA[40]	132	MEM_DATA[59]
35	MEM_DATA[30]	84	V_{DD}	133	MEM_DATA[60]
36	MEM_DATA[31]	85	GND	134	CPU_DATA[61]
37	MEM_CHECK[4]	86	CPU_DATA[43]	135	CPU_DATA[62]
38	V_{DD}	87	CPU_DATA[44]	136	CPU_DATA[63]
39	GND	88	CPU_DATA[45]	137	CPU_DPAR[7]
40	PCI_AD[16]	89	CPU_DATA[46]	138	MEM_DATA[61]
41	PCI_AD[17]	90	MEM_DATA[41]	139	MEM_DATA[62]
42	PCI_AD[18]	91	MEM_DATA[42]	140	MEM_DATA[63]
43	PCI_AD[19]	92	MEM_DATA[43]	141	MEM_CHECK[0]
44	PCI_AD[20]	93	MEM_DATA[44]	142	V_{DD}
45	PCI_AD[21]	94	CPU_DATA[47]	143	GND
46	PCI_AD[22]	95	CPU_DPAR[5]	144	PCI_AD_OE#
47	PCI_AD[23]	96	V_{DD}	145	MEM_DATA_OE#
48	PCI_AD[24]	97	GND	146	CPU_DATA_OE#
49	PCI_AD[25]	98	CPU_DATA[48]	147	MEM_RD_SMPL

New 663 Buffer Numeric Pin List (Continued)

Pin	663 Signal Name
148	CPU_RDL_OPEN
149	ECC_LE_SEL
150	MEM_WRL_OPEN
151	CRS_C2PWXS
152	MWS_P2MRXS
153	PCI_EXT_SEL
154	C2P_WRL_OPEN
155	TEST#
156	MIO_TEST
157	CPU_CLK
158	V_{DD}
159	GND
160	ROM_LOAD
161	MEM_BE[0]
162	MEM_BE[1]
163	MEM_BE[2]
164	MEM_BE[3]
165	PCI_OL_OPEN
166	AOS_RR_MMRS
167	PCI_IRDY#
168	PCI_TRDY#
169	PCI_OUT_SEL
170	DUAL_CTRL_REF
171	MEM_ERR#
172	V_{DD}
173	GND
174	CPU_PAR_ERR#
175	SBE#
176	CPU_DATA[00]
177	CPU_DATA[01]
178	CPU_DATA[02]

Pin	663 Signal Name
179	CPU_DATA[03]
180	MEM_DATA[00]
181	V_{DD}
182	MEM_DATA[01]
183	MEM_DATA[02]
184	MEM_DATA[03]
185	CPU_DATA[04]
186	CPU_DATA[05]
187	CPU_DATA[06]
188	CPU_DATA[07]
189	MEM_DATA[04]
190	MEM_DATA[05]
191	GND
192	V_{DD}
193	MEM_DATA[06]
194	MEM_DATA[07]
195	MEM_CHECK[7]
196	CPU_DPAR[0]
197	CPU_DATA[08]
198	CPU_DATA[09]
199	CPU_DATA[10]
200	MEM_DATA[08]
201	MEM_DATA[09]
202	MEM_DATA[10]
203	MEM_DATA[11]
204	V_{DD}
205	GND
206	MEM_DATA[12]
207	CPU_DATA[11]
208	CPU_DATA[12]
209	CPU_DATA[13]

Pin	663 Signal Name
210	CPU_DATA[14]
211	MEM_DATA[13]
212	MEM_DATA[14]
213	MEM_DATA[15]
214	MEM_CHECK[6]
215	MEM_DATA[16]
216	V_{DD}
217	GND
218	CPU_DATA[15]
219	CPU_DPAR[1]
220	CPU_DATA[16]
221	CPU_DATA[17]
222	MEM_DATA[17]
223	MEM_DATA[18]
224	MEM_DATA[19]
225	MEM_DATA[20]
226	CPU_DATA[18]
227	CPU_DATA[19]
228	CPU_DATA[20]
229	CPU_DATA[21]
230	V_{DD}
231	MEM_DATA[21]
232	MEM_DATA[22]
233	MEM_DATA[23]
234	MEM_CHECK[5]
235	GND
236	PCI_AD[00]
237	PCI_AD[01]
238	PCI_AD[02]
239	PCI_AD[03]
240	GND

3.2 New 663 Buffer Alphabetic Pin List

Pin	663 Signal Name
166	AOS_RR_MMRS
154	C2P_WRL_OPEN
157	CPU_CLK
176	CPU_DATA[00]
177	CPU_DATA[01]
178	CPU_DATA[02]
179	CPU_DATA[03]
185	CPU_DATA[04]
186	CPU_DATA[05]
187	CPU_DATA[06]
188	CPU_DATA[07]
197	CPU_DATA[08]
198	CPU_DATA[09]
199	CPU_DATA[10]
207	CPU_DATA[11]
208	CPU_DATA[12]
209	CPU_DATA[13]
210	CPU_DATA[14]
218	CPU_DATA[15]
220	CPU_DATA[16]
221	CPU_DATA[17]
226	CPU_DATA[18]
227	CPU_DATA[19]
228	CPU_DATA[20]
229	CPU_DATA[21]
1	CPU_DATA[22]
2	CPU_DATA[23]
4	CPU_DATA[24]
24	CPU_DATA[25]
25	CPU_DATA[26]
26	CPU_DATA[27]
27	CPU_DATA[28]
31	CPU_DATA[29]
32	CPU_DATA[30]
33	CPU_DATA[31]
54	CPU_DATA[32]
55	CPU_DATA[33]
56	CPU_DATA[34]
57	CPU_DATA[35]
67	CPU_DATA[36]
68	CPU_DATA[37]
69	CPU_DATA[38]
70	CPU_DATA[39]
78	CPU_DATA[40]
79	CPU_DATA[41]
80	CPU_DATA[42]
86	CPU_DATA[43]
87	CPU_DATA[44]

Pin	663 Signal Name
88	CPU_DATA[45]
89	CPU_DATA[46]
94	CPU_DATA[47]
98	CPU_DATA[48]
99	CPU_DATA[49]
104	CPU_DATA[50]
105	CPU_DATA[51]
106	CPU_DATA[52]
107	CPU_DATA[53]
114	CPU_DATA[54]
115	CPU_DATA[55]
117	CPU_DATA[56]
124	CPU_DATA[57]
125	CPU_DATA[58]
126	CPU_DATA[59]
127	CPU_DATA[60]
134	CPU_DATA[61]
135	CPU_DATA[62]
136	CPU_DATA[63]
146	CPU_DATA_OE#
196	CPU_DPAR[0]
219	CPU_DPAR[1]
3	CPU_DPAR[2]
34	CPU_DPAR[3]
77	CPU_DPAR[4]
95	CPU_DPAR[5]
116	CPU_DPAR[6]
137	CPU_DPAR[7]
174	CPU_PAR_ERR#
148	CPU_RDL_OPEN
151	CRS_C2PWXS
170	DUAL_CTRL_REF
149	ECC_LE_SEL
9	GND
23	GND
39	GND
53	GND
66	GND
71	GND
85	GND
97	GND
120	GND
129	GND
143	GND
159	GND
173	GND
191	GND
205	GND

Pin	663 Signal Name
217	GND
235	GND
240	GND
161	MEM_BE[0]
162	MEM_BE[1]
163	MEM_BE[2]
164	MEM_BE[3]
141	MEM_CHECK[0]
122	MEM_CHECK[1]
103	MEM_CHECK[2]
82	MEM_CHECK[3]
37	MEM_CHECK[4]
234	MEM_CHECK[5]
214	MEM_CHECK[6]
195	MEM_CHECK[7]
180	MEM_DATA[00]
182	MEM_DATA[01]
183	MEM_DATA[02]
184	MEM_DATA[03]
189	MEM_DATA[04]
190	MEM_DATA[05]
193	MEM_DATA[06]
194	MEM_DATA[07]
200	MEM_DATA[08]
201	MEM_DATA[09]
202	MEM_DATA[10]
203	MEM_DATA[11]
206	MEM_DATA[12]
211	MEM_DATA[13]
212	MEM_DATA[14]
213	MEM_DATA[15]
215	MEM_DATA[16]
222	MEM_DATA[17]
223	MEM_DATA[18]
224	MEM_DATA[19]
225	MEM_DATA[20]
231	MEM_DATA[21]
232	MEM_DATA[22]
233	MEM_DATA[23]
5	MEM_DATA[24]
6	MEM_DATA[25]
7	MEM_DATA[26]
28	MEM_DATA[27]
29	MEM_DATA[28]
30	MEM_DATA[29]
35	MEM_DATA[30]
36	MEM_DATA[31]
58	MEM_DATA[32]

New 663 Buffer Alphabetic Pin List (Continued)

Pin	663 Signal Name
59	MEM_DATA[33]
60	MEM_DATA[34]
73	MEM_DATA[35]
74	MEM_DATA[36]
75	MEM_DATA[37]
76	MEM_DATA[38]
81	MEM_DATA[39]
83	MEM_DATA[40]
90	MEM_DATA[41]
91	MEM_DATA[42]
92	MEM_DATA[43]
93	MEM_DATA[44]
100	MEM_DATA[45]
101	MEM_DATA[46]
102	MEM_DATA[47]
108	MEM_DATA[48]
109	MEM_DATA[49]
111	MEM_DATA[50]
112	MEM_DATA[51]
113	MEM_DATA[52]
118	MEM_DATA[53]
119	MEM_DATA[54]
121	MEM_DATA[55]
123	MEM_DATA[56]
130	MEM_DATA[57]
131	MEM_DATA[58]
132	MEM_DATA[59]
133	MEM_DATA[60]
138	MEM_DATA[61]
139	MEM_DATA[62]
140	MEM_DATA[63]
145	MEM_DATA_OE#

Pin	663 Signal Name
171	MEM_ERR#
147	MEM_RD_SMPL
150	MEM_WRL_OPEN
156	MIO_TEST
152	MWS_P2MRXS
236	PCI_AD[00]
237	PCI_AD[01]
238	PCI_AD[02]
239	PCI_AD[03]
10	PCI_AD[04]
11	PCI_AD[05]
12	PCI_AD[06]
13	PCI_AD[07]
14	PCI_AD[08]
15	PCI_AD[09]
16	PCI_AD[10]
17	PCI_AD[11]
18	PCI_AD[12]
19	PCI_AD[13]
20	PCI_AD[14]
21	PCI_AD[15]
40	PCI_AD[16]
41	PCI_AD[17]
42	PCI_AD[18]
43	PCI_AD[19]
44	PCI_AD[20]
45	PCI_AD[21]
46	PCI_AD[22]
47	PCI_AD[23]
48	PCI_AD[24]
49	PCI_AD[25]
50	PCI_AD[26]

Pin	663 Signal Name
51	PCI_AD[27]
62	PCI_AD[28]
63	PCI_AD[29]
64	PCI_AD[30]
65	PCI_AD[31]
144	PCI_AD_OE#
153	PCI_EXT_SEL
167	PCI_IRDY#
165	PCI_OL_OPEN
169	PCI_OUT_SEL
168	PCI_TRDY#
160	ROM_LOAD
175	SBE#
155	TEST#
8	V_{DD}
22	V_{DD}
38	V_{DD}
52	V_{DD}
61	V_{DD}
72	V_{DD}
84	V_{DD}
96	V_{DD}
110	V_{DD}
128	V_{DD}
142	V_{DD}
158	V_{DD}
172	V_{DD}
181	V_{DD}
192	V_{DD}
204	V_{DD}
216	V_{DD}
230	V_{DD}

4 Example Implementation Change

To improve output signal quality, 33Ω series resistors have been added to the 663 buffer connections to the CPU data bus lines CPU_DATA[0:63] and CPU_DPAR[0:8]. Each resister is placed between the 663 Buffer CPU_DATA[n] pin and all other CPU bus agent(s) attached to the CPU_DATA[n] net. In the case of the CPU_DPAR[n] nets, the resistor is placed between the 663 Buffer CPU_DPAR[n] pin and all other CPU bus agent(s) attached to the CPU_DPAR[n] net. For maximum benefit, place the series resistors as close to the 663 Buffer package as is feasible. These resistors and the new pinout of the 663 Buffer are shown on the *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set.

5 Additional Resources

The *IBM PowerPC 603/604 Reference Design* revision 2.1 and the *IBM PowerPC 604 SMP Reference Design* are now available to designers from your IBM technical representative. These designs feature the 660 Bridge, and include comprehensive and extensive documentation of system-related issues.

PowerPC

USA and Canada:
IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) PowerFax

Europe:
IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713–5757 (Français)
(33) 6713–5756 (Italiano)
Fax: (33) 6713–5750
(from Paris add 16)

Europe:
IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511–516–3444 (English)
(49) 511–516–3555 (Deutsche)
Fax: (49) 511–516–3888

Japan:
IBM
800, Ichimiyake
Yasu–cho, Yasu–gun
Shiga–ken, Japan 520–23
Tel: (81) 775–87–4745
Fax: (81) 775–87–4735

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