PowerPC™

IBM27-82660 Revision 2.0 Product Update

MPR660ESU-01

This document describes improvements to the IBM27-82660 Bridge from revision 1.0 to revision 2.0.

June 5, 1995

IBM®

Document Revision History

Errata Summary release 1.0 (April 19, 1995)
Errata for the 1.0 revision of the chipset.

IBM27-82660 Revision 2.0 Product Update (June 5, 1995)
Information on improvements to the chipset design from revision 1.0 to revision 2.0.

Part Identification, IBM27-82660 Chipset

IBM27-82663 (663 Buffer)
Chipset Rev. 1.0 contains IBM27-82663 Rev. 1.0. The package is marked 94G0235.

Chipset Rev. 2.0 contains IBM27-82663 Rev. 2.0. The package is marked 94G0178.

IBM27-82664 (664 Controller)
Chipset Rev. 1.0 contains IBM27-82664 Rev. 1.0. The package is marked 94G0232.

Chipset Rev. 2.0 contains IBM27-82664 Rev. 1.1. The package is marked 94G0176.

IBM27-82660 Revision 2.0 Product Update

June 5, 1995

This document describes improvements to the IBM27-82660 Bridge from revision 1.0 to revision 2.0.

Revision 1.0 of the 660 Bridge is described by a combination of three documents:

- *The IBM 27-82660 PowerPC to PCI Bridge User's Manual*, MPR660UMU-01 (beta version)
- *A System Implementation Example for the IBM 82660 Chipset (Preliminary)* schematic set, attached to the User's Manual
- The *IBM27-82660 Revision 1.0 Errata Summary*, MPR660ESU-00, or the most current 1.x revision.

Between revisions 1.0 and 2.0 of the 660 Bridge, several changes were implemented:

1. All known revision 1.0 errata were designed out. All external logic workarounds that were required to fix revision 1.0 errata were eliminated.
2. Two signal connections were added to the chipset. DBG# was added to the 664 Controller. PCI_TRDY# was added to the 663 Buffer.
3. The entire pinout of the 663 Buffer was rearranged.
4. The example implementation of the 663 Buffer was changed to enhance signal to noise ratio.

Revision 2.0 of the 660 Bridge is also described by a combination of three (or four) documents:

- *The IBM 27-82660 PowerPC to PCI Bridge User's Manual*, MPR660UMU-01 (beta version)
- The *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set, attached to the User's Manual
- This document, the *IBM27–82660 Revision 2.0 Product Update*
- The most current version of the revision 2.x Errata Summary.

1 All Known Revision 1.0 Errata Designed Out

All external logic that was required as a workaround for the revision 1.0 chipset has been eliminated. Except as noted herein, all of the workarounds should be removed from the design, and the 660 Bridge incorporated in the design as shown in the *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set.

2 Signals Added to the Chipset

DBG# was added to the 664 Controller to support a 604 in fast L2 mode. This change is documented in the MPR660UMU-01 release of the 660 Bridge User's Manual, and is noted here for completeness. See the 660 User's Manual for more information.

PCI_TRDY# was connected to the 663 Buffer to improve performance.

3 663 Buffer Pinout Rearranged

The pinout of the 663 Buffer was rearranged to reduce ground bounce effects by distributing simultaneously switched signals more evenly around the perimeter of the device. Previously, signal groups that were logically grouped were also grouped together physically. Redistributing these I/O more evenly has the effect of more evenly distributing the instantaneous current drawn from the power pins. This more even distribution of the current draw also evens out the instantaneous voltage drop experienced by the device during simultaneous switching events.

3.1 New 663 Buffer Numeric Pin List

Pin	663 Signal Name	Pin	663 Signal Name	Pin	663 Signal Name
1	CPU_DATA[22]	50	PCI_AD[26]	99	CPU_DATA[49]
2	CPU_DATA[23]	51	PCI_AD[27]	100	MEM_DATA[45]
3	CPU_DPAR[2]	52	V_{DD}	101	MEM_DATA[46]
4	CPU_DATA[24]	53	GND	102	MEM_DATA[47]
5	MEM_DATA[24]	54	CPU_DATA[32]	103	MEM_CHECK[5]
6	MEM_DATA[25]	55	CPU_DATA[33]	104	CPU_DATA[50]
7	MEM_DATA[26]	56	CPU_DATA[34]	105	CPU_DATA[51]
8	V_{DD}	57	CPU_DATA[35]	106	CPU_DATA[52]
9	GND	58	MEM_DATA[32]	107	CPU_DATA[53]
10	PCI_AD[04]	59	MEM_DATA[33]	108	MEM_DATA[48]
11	PCI_AD[05]	60	MEM_DATA[34]	109	MEM_DATA[49]
12	PCI_AD[06]	61	V_{DD}	110	V_{DD}
13	PCI_AD[07]	62	PCI_AD[28]	111	MEM_DATA[50]
14	PCI_AD[08]	63	PCI_AD[29]	112	MEM_DATA[51]
15	PCI_AD[09]	64	PCI_AD[30]	113	MEM_DATA[52]
16	PCI_AD[10]	65	PCI_AD[31]	114	CPU_DATA[54]
17	PCI_AD[11]	66	GND	115	CPU_DATA[55]
18	PCI_AD[12]	67	CPU_DATA[36]	116	CPU_DPAR[6]
19	PCI_AD[13]	68	CPU_DATA[37]	117	CPU_DATA[56]
20	PCI_AD[14]	69	CPU_DATA[38]	118	MEM_DATA[53]
21	PCI_AD[15]	70	CPU_DATA[39]	119	MEM_DATA[54]
22	V_{DD}	71	GND	120	GND
23	GND	72	V_{DD}	121	MEM_DATA[55]
24	CPU_DATA[25]	73	MEM_DATA[35]	122	MEM_CHECK[6]
25	CPU_DATA[26]	74	MEM_DATA[36]	123	MEM_DATA[56]
26	CPU_DATA[27]	75	MEM_DATA[37]	124	CPU_DATA[57]
27	CPU_DATA[28]	76	MEM_DATA[38]	125	CPU_DATA[58]
28	MEM_DATA[27]	77	CPU_DPAR[4]	126	CPU_DATA[59]
29	MEM_DATA[28]	78	CPU_DATA[40]	127	CPU_DATA[60]
30	MEM_DATA[29]	79	CPU_DATA[41]	128	V_{DD}
31	CPU_DATA[29]	80	CPU_DATA[42]	129	GND
32	CPU_DATA[30]	81	MEM_DATA[39]	130	MEM_DATA[57]
33	CPU_DATA[31]	82	MEM_CHECK[4]	131	MEM_DATA[58]
34	CPU_DPAR[3]	83	MEM_DATA[40]	132	MEM_DATA[59]
35	MEM_DATA[30]	84	V_{DD}	133	MEM_DATA[60]
36	MEM_DATA[31]	85	GND	134	CPU_DATA[61]
37	MEM_CHECK[3]	86	CPU_DATA[43]	135	CPU_DATA[62]
38	V_{DD}	87	CPU_DATA[44]	136	CPU_DATA[63]
39	GND	88	CPU_DATA[45]	137	CPU_DPAR[7]
40	PCI_AD[16]	89	CPU_DATA[46]	138	MEM_DATA[61]
41	PCI_AD[17]	90	MEM_DATA[41]	139	MEM_DATA[62]
42	PCI_AD[18]	91	MEM_DATA[42]	140	MEM_DATA[63]
43	PCI_AD[19]	92	MEM_DATA[43]	141	MEM_CHECK[7]
44	PCI_AD[20]	93	MEM_DATA[44]	142	V_{DD}
45	PCI_AD[21]	94	CPU_DATA[47]	143	GND
46	PCI_AD[22]	95	CPU_DPAR[5]	144	PCI_AD_OE#
47	PCI_AD[23]	96	V_{DD}	145	MEM_DATA_OE#
48	PCI_AD[24]	97	GND	146	CPU_DATA_OE#
49	PCI_AD[25]	98	CPU_DATA[48]	147	MEM_RD_SMPL

New 663 Buffer Numeric Pin List (Continued)

Pin	663 Signal Name
148	CPU_RDL_OPEN
149	ECC_LE_SEL
150	MEM_WRL_OPEN
151	CRS_C2PWXS
152	MWS_P2MRXS
153	PCI_EXT_SEL
154	C2P_WRL_OPEN
155	TEST#
156	MIO_TEST
157	CPU_CLK
158	V_{DD}
159	GND
160	ROM_LOAD
161	MEM_BE[0]
162	MEM_BE[1]
163	MEM_BE[2]
164	MEM_BE[3]
165	PCI_OL_OPEN
166	AOS_RR_MMRS
167	PCI_IRDY#
168	PCI_TRDY#
169	PCI_OUT_SEL
170	DUAL_CTRL_REF
171	MEM_ERR#
172	V_{DD}
173	GND
174	CPU_PAR_ERR#
175	SBE#
176	CPU_DATA[00]
177	CPU_DATA[01]
178	CPU_DATA[02]

Pin	663 Signal Name
179	CPU_DATA[03]
180	MEM_DATA[00]
181	V_{DD}
182	MEM_DATA[01]
183	MEM_DATA[02]
184	MEM_DATA[03]
185	CPU_DATA[04]
186	CPU_DATA[05]
187	CPU_DATA[06]
188	CPU_DATA[07]
189	MEM_DATA[04]
190	MEM_DATA[05]
191	GND
192	V_{DD}
193	MEM_DATA[06]
194	MEM_DATA[07]
195	MEM_CHECK[0]
196	CPU_DPAR[0]
197	CPU_DATA[08]
198	CPU_DATA[09]
199	CPU_DATA[10]
200	MEM_DATA[08]
201	MEM_DATA[09]
202	MEM_DATA[10]
203	MEM_DATA[11]
204	V_{DD}
205	GND
206	MEM_DATA[12]
207	CPU_DATA[11]
208	CPU_DATA[12]
209	CPU_DATA[13]

Pin	663 Signal Name
210	CPU_DATA[14]
211	MEM_DATA[13]
212	MEM_DATA[14]
213	MEM_DATA[15]
214	MEM_CHECK[1]
215	MEM_DATA[16]
216	V_{DD}
217	GND
218	CPU_DATA[15]
219	CPU_DPAR[1]
220	CPU_DATA[16]
221	CPU_DATA[17]
222	MEM_DATA[17]
223	MEM_DATA[18]
224	MEM_DATA[19]
225	MEM_DATA[20]
226	CPU_DATA[18]
227	CPU_DATA[19]
228	CPU_DATA[20]
229	CPU_DATA[21]
230	V_{DD}
231	MEM_DATA[21]
232	MEM_DATA[22]
233	MEM_DATA[23]
234	MEM_CHECK[2]
235	GND
236	PCI_AD[00]
237	PCI_AD[01]
238	PCI_AD[02]
239	PCI_AD[03]
240	GND

3.2 New 663 Buffer Alphabetic Pin List

Pin	663 Signal Name
166	AOS_RR_MMRS
154	C2P_WRL_OPEN
157	CPU_CLK
176	CPU_DATA[00]
177	CPU_DATA[01]
178	CPU_DATA[02]
179	CPU_DATA[03]
185	CPU_DATA[04]
186	CPU_DATA[05]
187	CPU_DATA[06]
188	CPU_DATA[07]
197	CPU_DATA[08]
198	CPU_DATA[09]
199	CPU_DATA[10]
207	CPU_DATA[11]
208	CPU_DATA[12]
209	CPU_DATA[13]
210	CPU_DATA[14]
218	CPU_DATA[15]
220	CPU_DATA[16]
221	CPU_DATA[17]
226	CPU_DATA[18]
227	CPU_DATA[19]
228	CPU_DATA[20]
229	CPU_DATA[21]
1	CPU_DATA[22]
2	CPU_DATA[23]
4	CPU_DATA[24]
24	CPU_DATA[25]
25	CPU_DATA[26]
26	CPU_DATA[27]
27	CPU_DATA[28]
31	CPU_DATA[29]
32	CPU_DATA[30]
33	CPU_DATA[31]
54	CPU_DATA[32]
55	CPU_DATA[33]
56	CPU_DATA[34]
57	CPU_DATA[35]
67	CPU_DATA[36]
68	CPU_DATA[37]
69	CPU_DATA[38]
70	CPU_DATA[39]
78	CPU_DATA[40]
79	CPU_DATA[41]
80	CPU_DATA[42]
86	CPU_DATA[43]
87	CPU_DATA[44]

Pin	663 Signal Name
88	CPU_DATA[45]
89	CPU_DATA[46]
94	CPU_DATA[47]
98	CPU_DATA[48]
99	CPU_DATA[49]
104	CPU_DATA[50]
105	CPU_DATA[51]
106	CPU_DATA[52]
107	CPU_DATA[53]
114	CPU_DATA[54]
115	CPU_DATA[55]
117	CPU_DATA[56]
124	CPU_DATA[57]
125	CPU_DATA[58]
126	CPU_DATA[59]
127	CPU_DATA[60]
134	CPU_DATA[61]
135	CPU_DATA[62]
136	CPU_DATA[63]
146	CPU_DATA_OE#
196	CPU_DPAR[0]
219	CPU_DPAR[1]
3	CPU_DPAR[2]
34	CPU_DPAR[3]
77	CPU_DPAR[4]
95	CPU_DPAR[5]
116	CPU_DPAR[6]
137	CPU_DPAR[7]
174	CPU_PAR_ERR#
148	CPU_RDL_OPEN
151	CRS_C2PWXS
170	DUAL_CTRL_REF
149	ECC_LE_SEL
9	GND
23	GND
39	GND
53	GND
66	GND
71	GND
85	GND
97	GND
120	GND
129	GND
143	GND
159	GND
173	GND
191	GND
205	GND

Pin	663 Signal Name
217	GND
235	GND
240	GND
161	MEM_BE[0]
162	MEM_BE[1]
163	MEM_BE[2]
164	MEM_BE[3]
195	MEM_CHECK[0]
214	MEM_CHECK[1]
234	MEM_CHECK[2]
37	MEM_CHECK[3]
82	MEM_CHECK[4]
103	MEM_CHECK[5]
122	MEM_CHECK[6]
141	MEM_CHECK[7]
180	MEM_DATA[00]
182	MEM_DATA[01]
183	MEM_DATA[02]
184	MEM_DATA[03]
189	MEM_DATA[04]
190	MEM_DATA[05]
193	MEM_DATA[06]
194	MEM_DATA[07]
200	MEM_DATA[08]
201	MEM_DATA[09]
202	MEM_DATA[10]
203	MEM_DATA[11]
206	MEM_DATA[12]
211	MEM_DATA[13]
212	MEM_DATA[14]
213	MEM_DATA[15]
215	MEM_DATA[16]
222	MEM_DATA[17]
223	MEM_DATA[18]
224	MEM_DATA[19]
225	MEM_DATA[20]
231	MEM_DATA[21]
232	MEM_DATA[22]
233	MEM_DATA[23]
5	MEM_DATA[24]
6	MEM_DATA[25]
7	MEM_DATA[26]
28	MEM_DATA[27]
29	MEM_DATA[28]
30	MEM_DATA[29]
35	MEM_DATA[30]
36	MEM_DATA[31]
58	MEM_DATA[32]

New 663 Buffer Alphabetic Pin List (Continued)

Pin	663 Signal Name	Pin	663 Signal Name	Pin	663 Signal Name
59	MEM_DATA[33]	171	MEM_ERR#	51	PCI_AD[27]
60	MEM_DATA[34]	147	MEM_RD_SMPL	62	PCI_AD[28]
73	MEM_DATA[35]	150	MEM_WRL_OPEN	63	PCI_AD[29]
74	MEM_DATA[36]	156	MIO_TEST	64	PCI_AD[30]
75	MEM_DATA[37]	152	MWS_P2MRXS	65	PCI_AD[31]
76	MEM_DATA[38]	236	PCI_AD[00]	144	PCI_AD_OE#
81	MEM_DATA[39]	237	PCI_AD[01]	153	PCI_EXT_SEL
83	MEM_DATA[40]	238	PCI_AD[02]	167	PCI_IRDY#
90	MEM_DATA[41]	239	PCI_AD[03]	165	PCI_OL_OPEN
91	MEM_DATA[42]	10	PCI_AD[04]	169	PCI_OUT_SEL
92	MEM_DATA[43]	11	PCI_AD[05]	168	PCI_TRDY#
93	MEM_DATA[44]	12	PCI_AD[06]	160	ROM_LOAD
100	MEM_DATA[45]	13	PCI_AD[07]	175	SBE#
101	MEM_DATA[46]	14	PCI_AD[08]	155	TEST#
102	MEM_DATA[47]	15	PCI_AD[09]	8	V_{DD}
108	MEM_DATA[48]	16	PCI_AD[10]	22	V_{DD}
109	MEM_DATA[49]	17	PCI_AD[11]	38	V_{DD}
111	MEM_DATA[50]	18	PCI_AD[12]	52	V_{DD}
112	MEM_DATA[51]	19	PCI_AD[13]	61	V_{DD}
113	MEM_DATA[52]	20	PCI_AD[14]	72	V_{DD}
118	MEM_DATA[53]	21	PCI_AD[15]	84	V_{DD}
119	MEM_DATA[54]	40	PCI_AD[16]	96	V_{DD}
121	MEM_DATA[55]	41	PCI_AD[17]	110	V_{DD}
123	MEM_DATA[56]	42	PCI_AD[18]	128	V_{DD}
130	MEM_DATA[57]	43	PCI_AD[19]	142	V_{DD}
131	MEM_DATA[58]	44	PCI_AD[20]	158	V_{DD}
132	MEM_DATA[59]	45	PCI_AD[21]	172	V_{DD}
133	MEM_DATA[60]	46	PCI_AD[22]	181	V_{DD}
138	MEM_DATA[61]	47	PCI_AD[23]	192	V_{DD}
139	MEM_DATA[62]	48	PCI_AD[24]	204	V_{DD}
140	MEM_DATA[63]	49	PCI_AD[25]	216	V_{DD}
145	MEM_DATA_OE#	50	PCI_AD[26]	230	V_{DD}

4 Example Implementation Change

To improve output signal quality, 33Ω series resistors have been added to the 663 buffer connections to the CPU data bus lines CPU_DATA[0:63] and CPU_DPAR[0:8]. Each resister is placed between the 663 Buffer CPU_DATA[n] pin and all other CPU bus agent(s) attached to the CPU_DATA[n] net. In the case of the CPU_DPAR[n] nets, the resistor is placed between the 663 Buffer CPU_DPAR[n] pin and and all other CPU bus agent(s) attached to the CPU_DPAR[n] net. For maximum benefit, place the series resistors as close to the 663 Buffer package as is feasible. These resistors and the new pinout of the 663 Buffer are shown on the *IBM27-82660 Example Implementation For MPR660UMU–02* schematic set.

PowerPC

USA and Canada:
IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) PowerFax

Europe:
IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713–5757 (Français)
(33) 6713–5756 (Italiano)
Fax: (33) 6713–5750
(from Paris add 16)

Europe:
IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511–516–3444 (English)
(49) 511–516–3555 (Deutsche)
Fax: (49) 511–516–3888

Japan:
IBM
800, Ichimiyake
Yasu–cho, Yasu–gun
Shiga–ken, Japan 520–23
Tel: (81) 775–87–4745
Fax: (81) 775–87–4735

Document Number: MPR660ESU–01

IBM27-82660

EXAMPLE IMPLEMENTATION FOR MPR660UMU-02

PRELIMINARY

IBM	
	SIZE B / REVISION / DRWNG PART NUMBER
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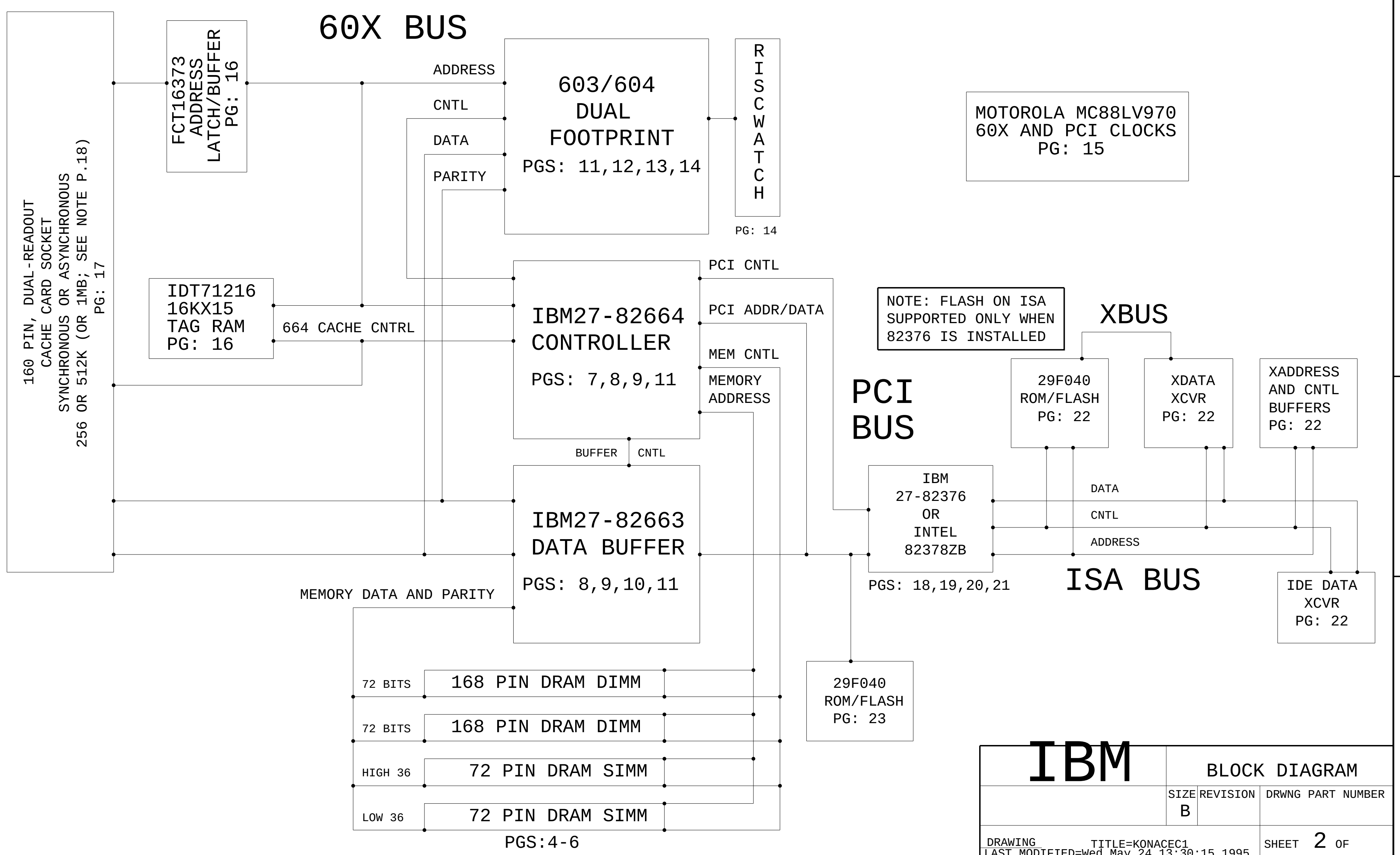


IBM	BLOCK DIAGRAM		
	SIZE B	REVISION	DRWNG PART NUMBER
DRAWING TITLE=KONACEC1 LAST_MODIFIED=Wed May 24 13:30:15 1995			SHEET 2 OF

CONFIGURATION NOTES

SYSTEM CLOCK CONFIGURATION OPTIONS

MOTO LV970 CONFIG SETTINGS:

J9: LEGAL SETTINGS FOR REFERENCE DESIGN MARKED WITH (*)
MPC601_CLKS = 0; VCO_SEL SET TO 0

LEGAL	PCI DIV1	PCI DIV0	BCLK DIV1	BCLK DIV0	2X_PCLK,PCLK_EN BCLK_EN	ALL OTHER BCLK(X)	PCI_CLK(X)
*	0	0	0	0	FOUT	FOUT	FOUT
	0	0	0	1	FOUT	FOUT/2	FOUT/2
	0	0	1	0	FOUT	FOUT/3	FOUT/3
	0	0	1	1	FOUT	FOUT/4	FOUT/4
*	0	1	0	0	FOUT	FOUT	FOUT/2
	0	1	0	1	FOUT	FOUT/2	FOUT/4
	0	1	1	0	FOUT	FOUT/3	FOUT/6
	0	1	1	1	FOUT	FOUT/4	FOUT/8
*	1	0	0	0	FOUT	FOUT	FOUT/3
	1	0	0	1	FOUT	FOUT/2	FOUT/6
	1	0	1	0	FOUT	FOUT/3	FOUT/9
	1	0	1	1	FOUT	FOUT/4	FOUT/12
*	1	1	0	0	FOUT	FOUT	FOUT
	1	1	0	1	FOUT	FOUT/2	FOUT
	1	1	1	0	FOUT	FOUT/3	FOUT
	1	1	1	1	FOUT	FOUT/4	FOUT

VCO_SEL PIN (PIN 52):

FOUT = 8 X FIN IF VCO_SEL=1
FOUT = 4 X FIN IF VCO_SEL=0
FVCO = 32 X FIN; 300MHZ <= FVCO <= 1000MHZ
IT IS REQUIRED THAT 10MHZ <= FIN <= 25 MHZ

FIN IS DEFINED BY Y1 CRYSTAL. ALTERNATELY, THE PLL CAN BE BYPASSED AND A REFERENCE FREQUENCY (TTL_CLK) IS TRANSFERRED TO THE OUTPUTS.

603/604 PLL CONFIG

J10: USABLE PLLCFG SETTINGS

PLL CFG0	PLL CFG1	PLL CFG2	PLL CFG3	604 PCLK:BCLK RATIO	604 VCO DIV	603 PCLK:BCLK RATIO	603 VCO DIV
0	0	0	0	1:1	/2	1:1	/2
0	0	0	1	1:1	/4	1:1	/4
0	0	1	0	1:1	/8	1:1	/8
0	0	1	1				
0	1	0	0	2:1	/2	2:1	/2
0	1	0	1	2:1	/4	2:1	/4
0	1	1	0				
0	1	1	1				
1	0	0	0	3:1	/2	3:1	/2
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0	3:2	/2	4:1	/2
1	1	0	1	3:2	/4		
1	1	1	0				
1	1	1	1				

SET PLLCFG SUCH THAT FVCO / DIV = BCLK X RATIO
AND 100<=FVCO<=200 FOR 603, 112.5<=FVCO,=225 FOR 604

PCI TO ISA BRIDGE CONFIGURATION OPTIONS

THIS REFERENCE IMPLEMENTATION ILLUSTRATES THE USAGE OF ONE OF TWO PCI/ISA BRIDGE CHIPS, THE IBM27-82376 OR THE INTEL SIO 82378ZB.

THESE TWO CHIPS SHARE 171 PINS WITH IDENTICAL FUNCTION AND LOCATION. THERE ARE AN ADDITIONAL 19 PINS THAT HAVE SLIGHTLY DIFFERENT FUNCTION OR DEFINITION AND 18 PINS THAT HAVE COMPLETELY UNIQUE FUNCTIONS.

THE READER SHOULD REFERENCE PAGES 18-21 FOR NOTES REGARDING THE CONNECTION OF THESE DEVICES.

60X PROCESSOR OPERATING MODES

THE 604 PROCESSOR HAS TWO DRIVER MODE CONFIGURATION PINS THAT CAN BE CONFIGURED TO ALLOW THE USER TO CHOOSE THE DRIVE STRENGTH FOR A SUBSET OF THE 60X BUS CONTROL PINS. THESE DRIVER MODE PINS (DRVMOD<1:0>) ARE SET BY PULL UP/DOWN RESISTORS ON KONA.

THE DRVMOD PINS SHOULD BE SET ACCORDING TO THE TABLE SHOWN BELOW.

DRVMOD<0> = 0, R110 = 1K, R137 = NOPOP
= 1, R110 = NOPOP, R137 = 10K
DRVMOD<1> = 0, R109 = 1K, R128 = NOPOP
= 1, R109 = NOPOP, R128 = 10K

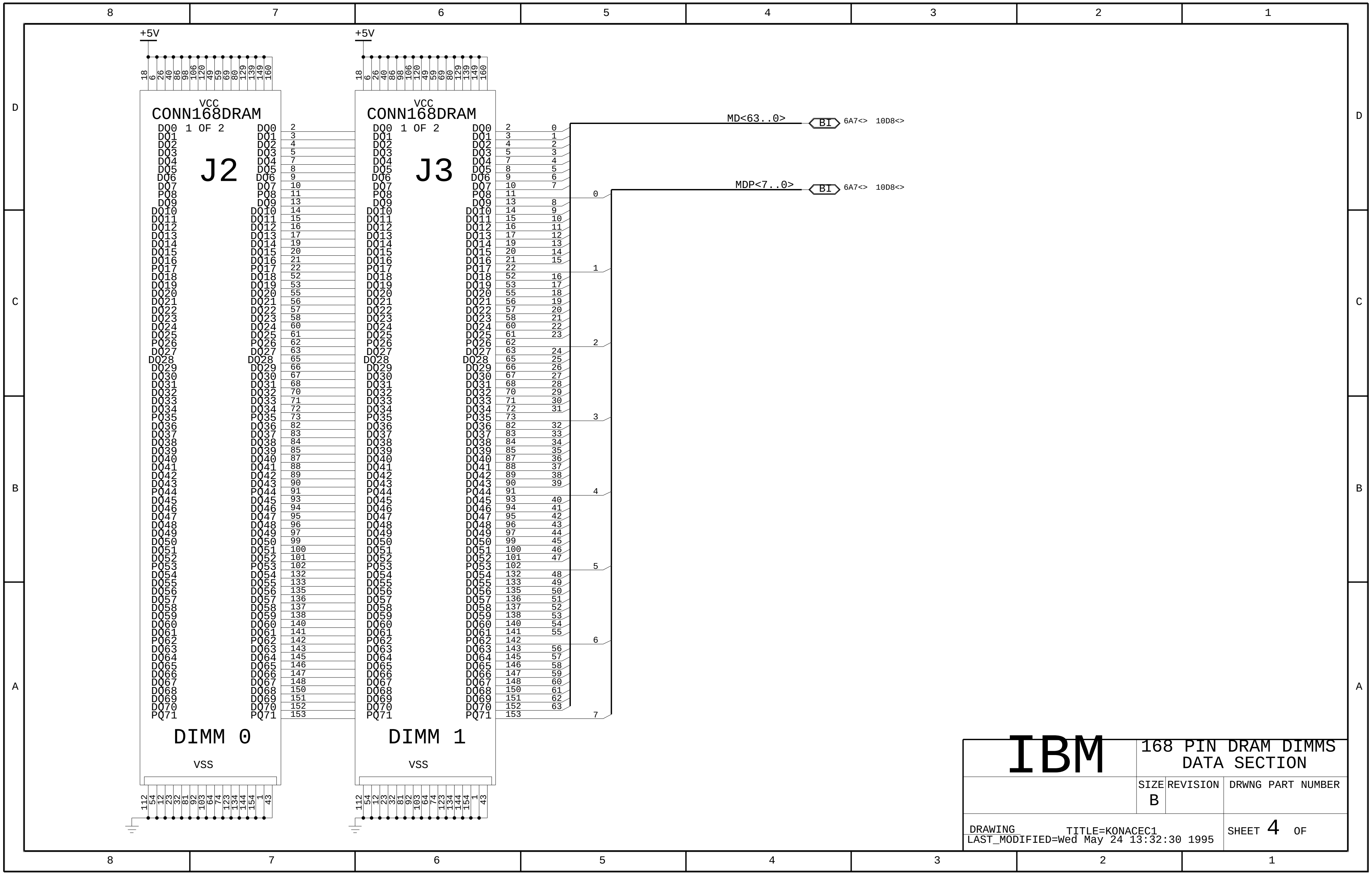
MODE	DRVMOD<0>	DRVMOD<1>
DISABLED	0	0
NORMAL	0	1
STRONG	1	0
HERCULEAN	1	1

664 CONTROLLER OPERATING MODES

THE 664 SYSTEM CONTROLLER HAS TWO HARDWARE STRAPPING OPTIONS THAT MUST BE CONFIGURED USING JUMPERS AT J6.

J6.B1 IS CONNECTED TO MWS_P2MRXS. THIS PIN SHOULD BE PULLED UP IF THE SYSTEM PROCESSOR IS A 603 RUNNING 1:1 CLOCKING MODE. OTHERWISE THIS PIN SHOULD BE PULLED DOWN.

J6.B2 IS CONNECTED TO CRS_C2PWXS. THIS PIN SHOULD BE PULLED UP IF THE SYSTEM IPL ROM IS LOCATED BEHIND THE PCI I/O BRIDGE. OTHERWISE IT SHOULD BE PULLED DOWN TO INDICATE THAT THE SYSTEM IPL ROM IS CONNECTED DIRECTLY TO THE 664 ROM INTERFACE.



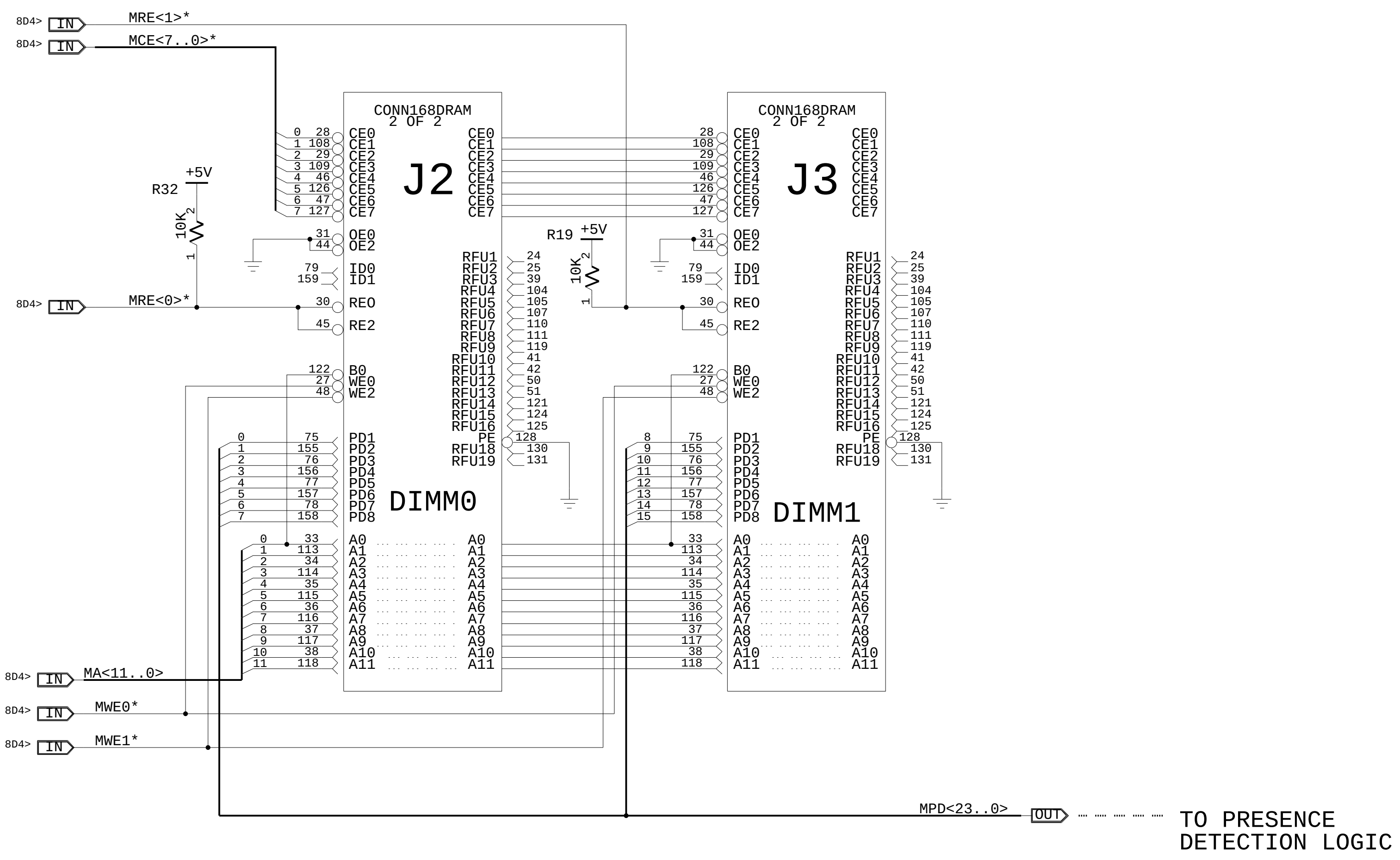
IBM

168 PIN DRAM DIMMS
DATA SECTION

SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:30 1995

SHEET 4 OF



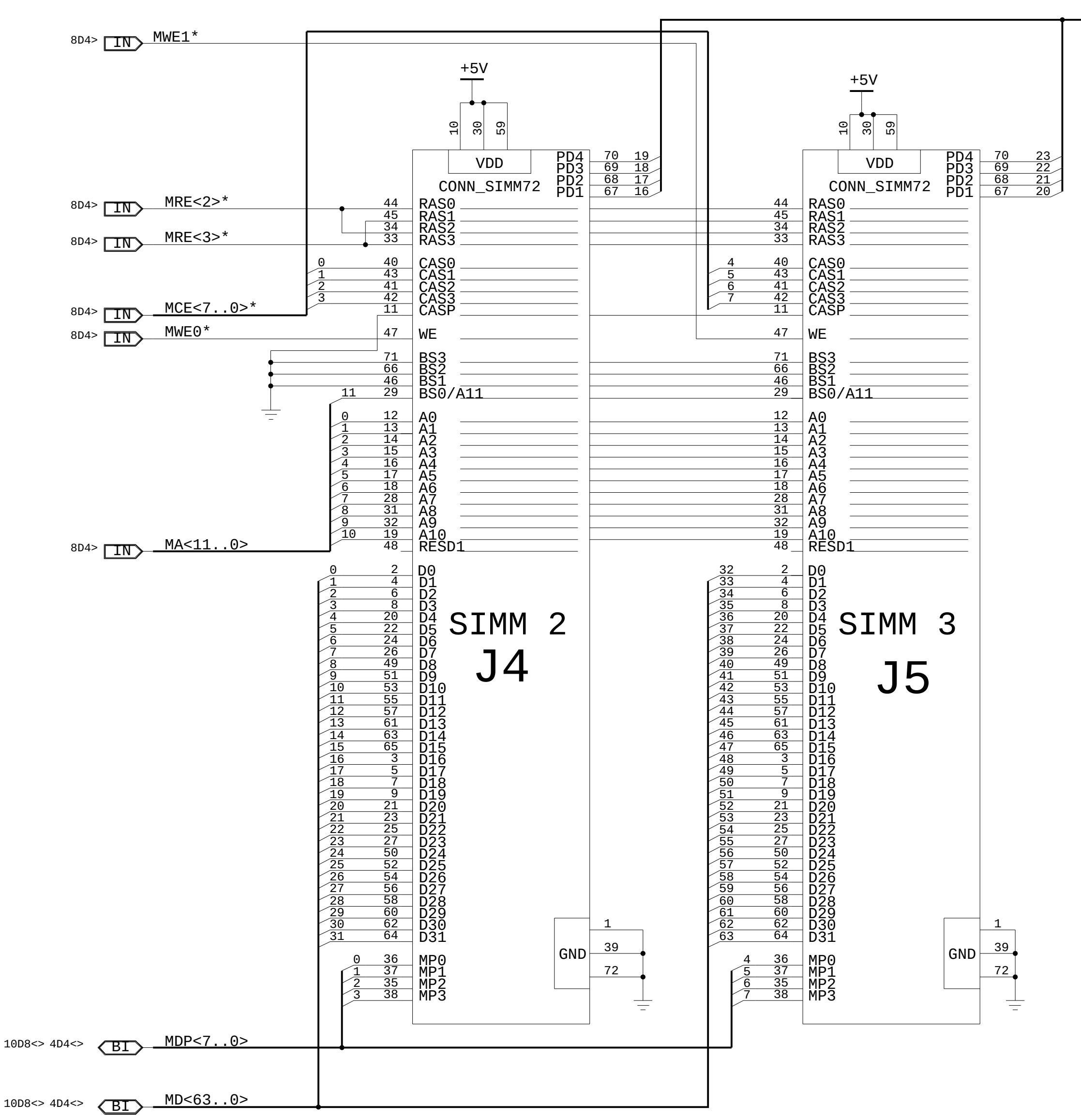
IBM

168 PIN DRAM DIMMS
CONTROL SECTION

SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:32 1995

SHEET 5 OF



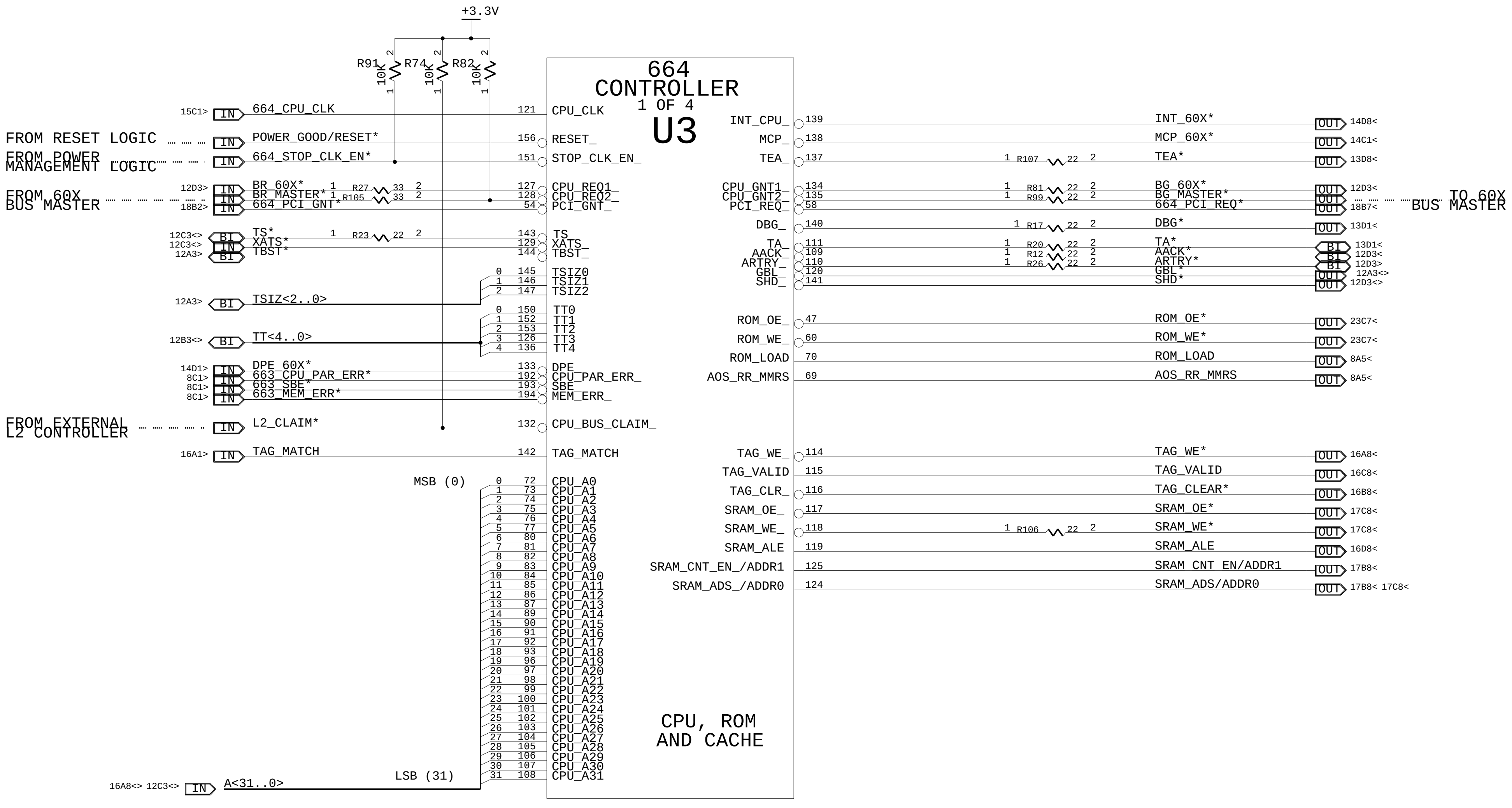
BUFFERING MA,WE,RAS, AND CAS

DESIGNERS SHOULD CONSIDER BUFFERING THE 82664 MEMORY DRIVERS (MA,WE,RAS,CAS) WHEN THE LOAD ON AN INDIVIDUAL DRIVER APPROACHES 350-400PF.

BUFFERING WILL MOST LIKELY NOT BE NECESSARY FOR DESIGNS USING 1-8 168 PIN X72 DUAL-SIDED IN-LINE MEMORY MODULES.

SOME BUFFERING MAY BE NECESSARY FOR DESIGNS USING MORE THAN TWO 72 PIN X36 SINGLE-SIDED IN-LINE MEMORY MODULES.

IBM	72 PIN DRAM DIMMS		
	SIZE B	REVISION	DRWNG PART NUMBER
DRAWING TITLE=KONACEC1 LAST_MODIFIED=Wed May 24 13:32:35 1995			SHEET 6 OF



PHYSICAL DESIGN NOTE:

ALL SERIES RESISTORS MUST BE PLACED AS CLOSE TO 664 AS POSSIBLE.

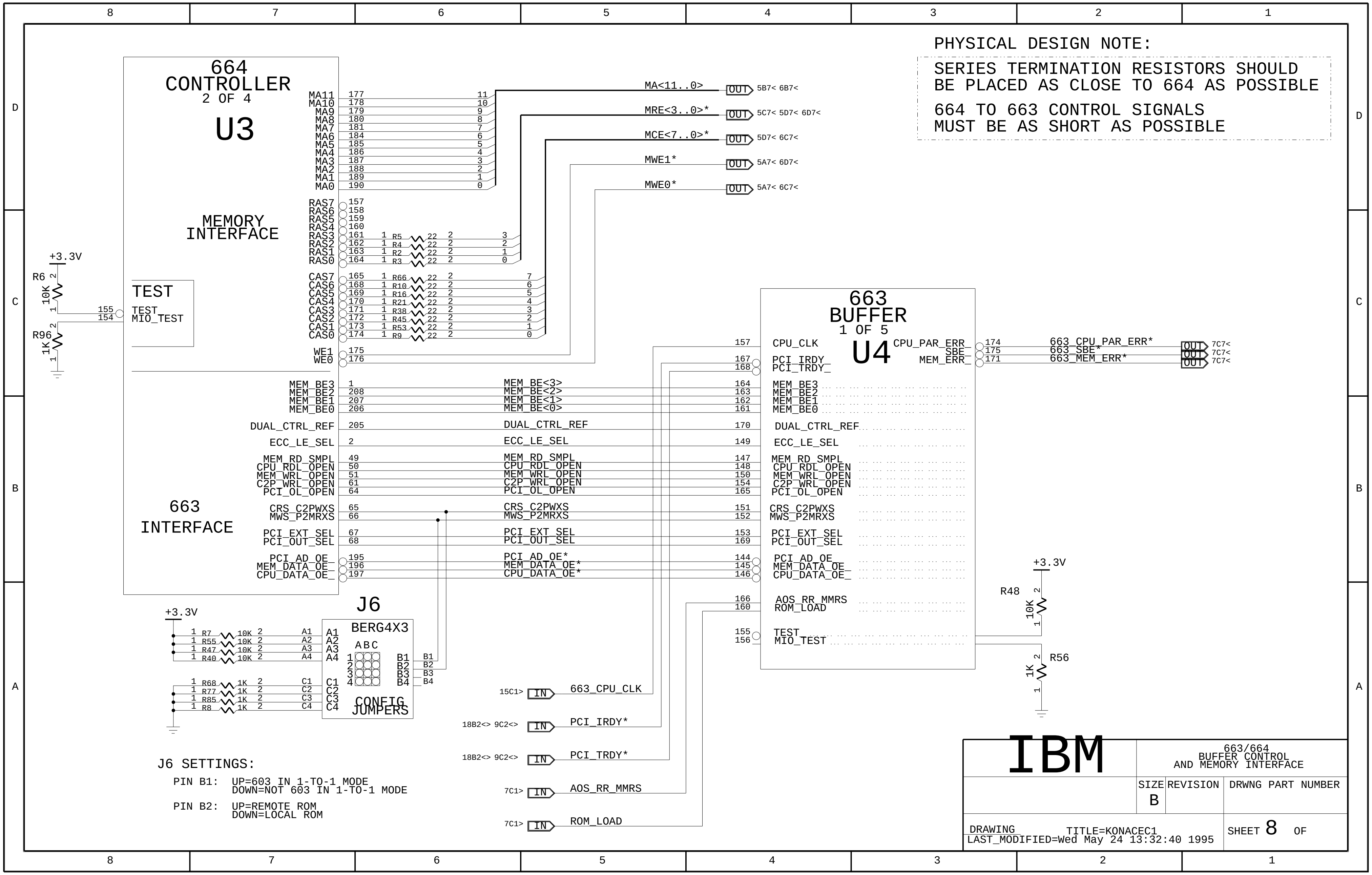
IBM

664 CONTROLLER
CENTRAL CONTROL PORTION

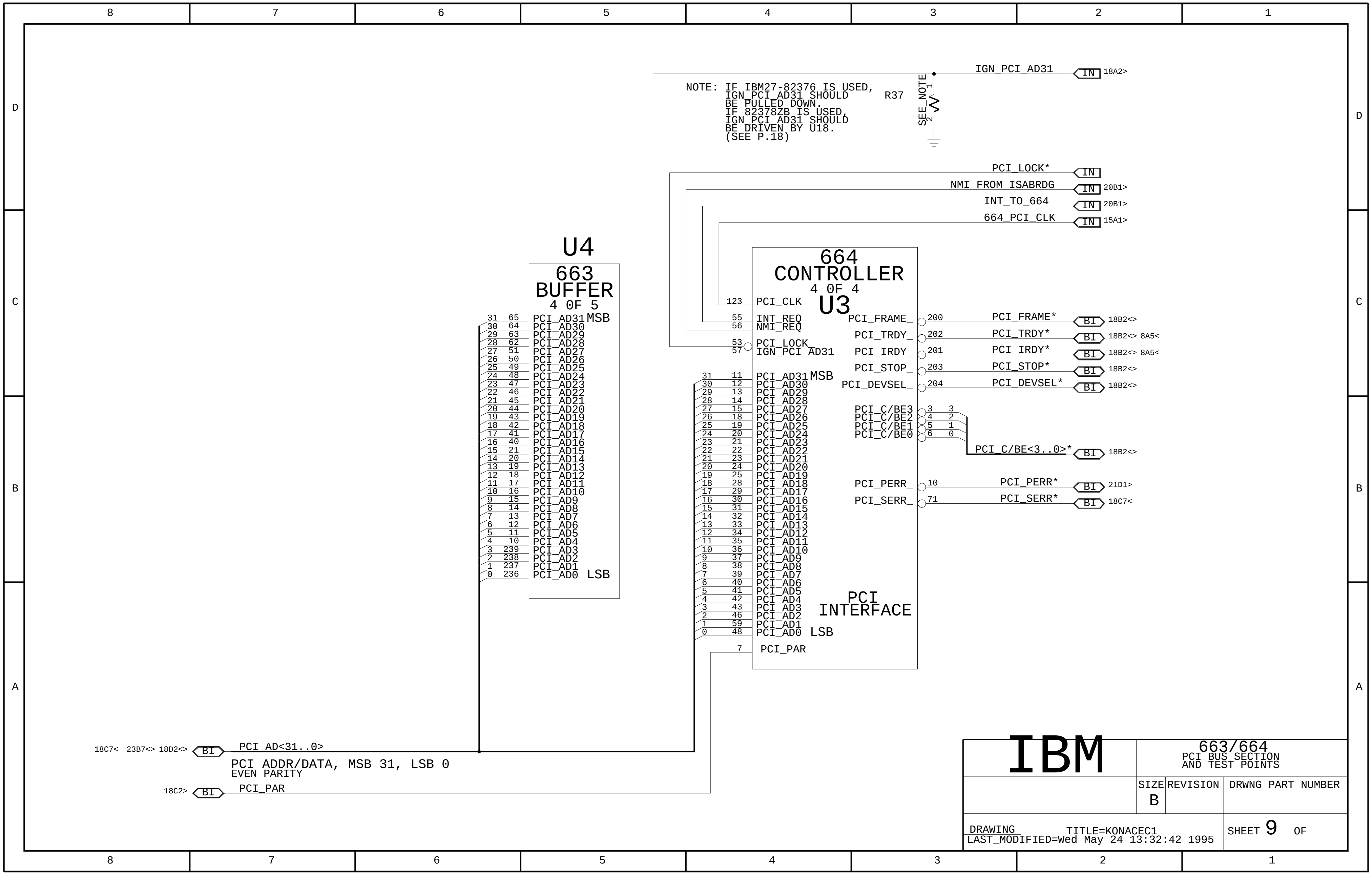
SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:38 1995

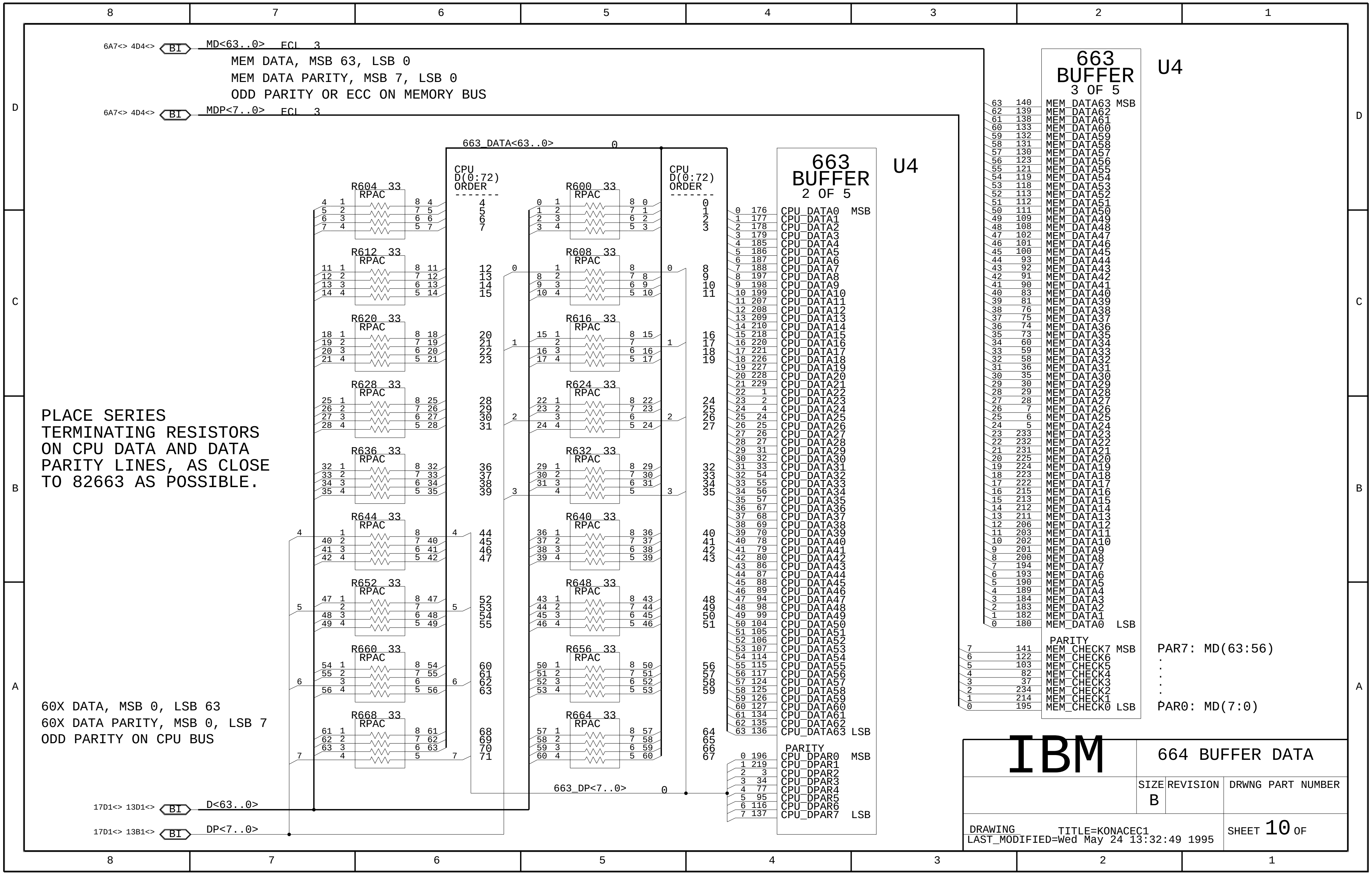
SHEET 7 OF



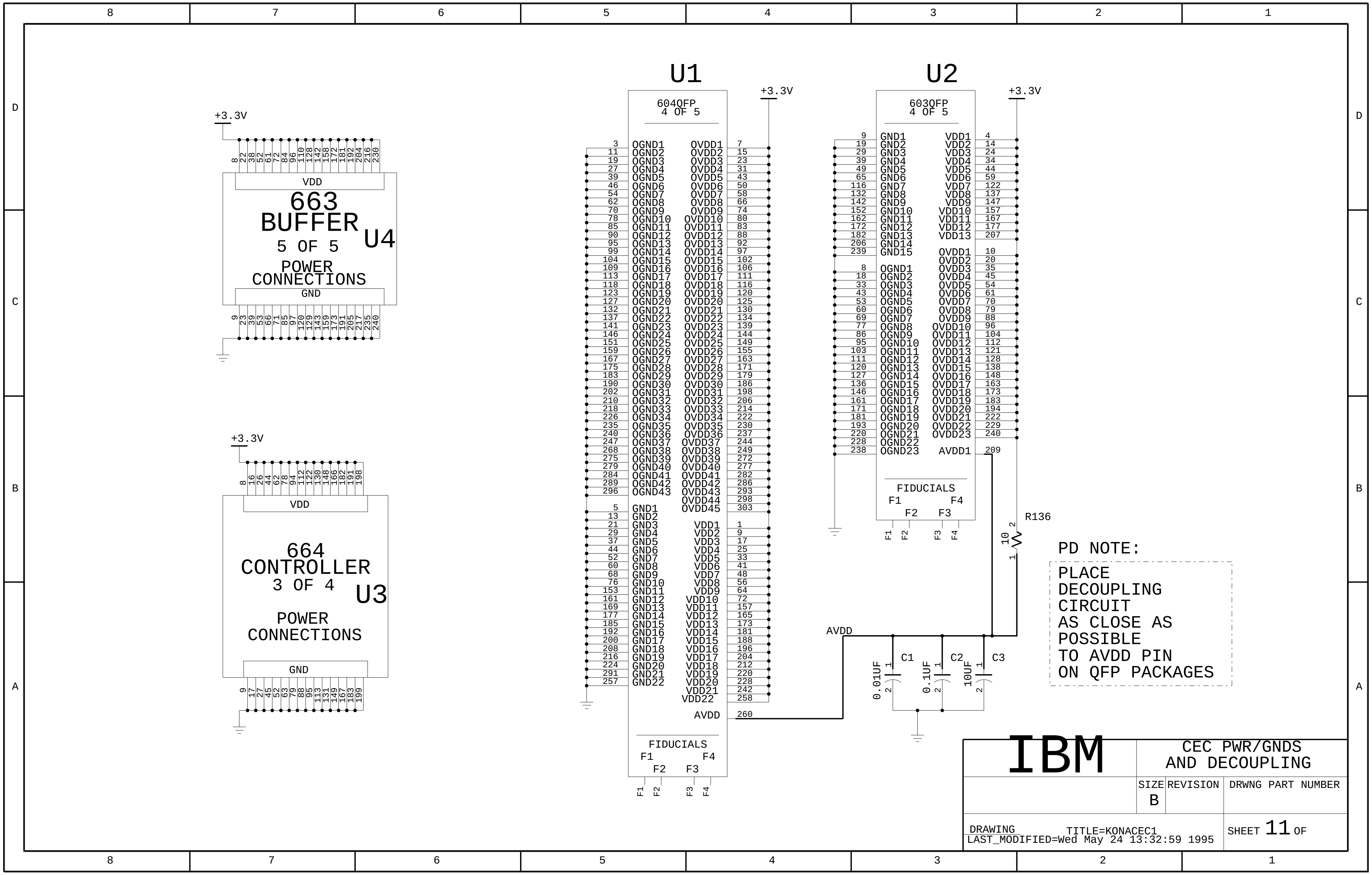
PHYSICAL DESIGN NOTE:
SERIES TERMINATION RESISTORS SHOULD BE PLACED AS CLOSE TO 664 AS POSSIBLE
664 TO 663 CONTROL SIGNALS MUST BE AS SHORT AS POSSIBLE
664 CONTROLLER 2 OF 4
U3
MEMORY INTERFACE
663 INTERFACE
TEST
TEST
MIO_TEST
MA11 MA10 MA9 MA8 MA7 MA6 MA5 MA4 MA3 MA2 MA1 MA0
RAS7 RAS6 RAS5 RAS4 RAS3 RAS2 RAS1 RAS0
CAS7 CAS6 CAS5 CAS4 CAS3 CAS2 CAS1 CAS0
WE1 WE0
MA<11..0>
MRE<3..0>*
MCE<7..0>*
MWE1*
MWE0*
OUT
5B7< 6B7<
5C7< 5D7< 6D7<
5D7< 6C7<
5A7< 6D7<
5A7< 6C7<
MEM_BE3 MEM_BE2 MEM_BE1 MEM_BE0
MEM_BE<3> MEM_BE<2> MEM_BE<1> MEM_BE<0>
DUAL_CTRL_REF
ECC_LE_SEL
MEM_RD_SMPL
CPU_RDL_OPEN
MEM_WRL_OPEN
C2P_WRL_OPEN
PCI_OL_OPEN
CRS_C2PWXS
MWS_P2MRXS
PCI_EXT_SEL
PCI_OUT_SEL
PCI_AD_OE_
MEM_DATA_OE_
CPU_DATA_OE_
PCI_AD_OE*
MEM_DATA_OE*
CPU_DATA_OE*
663 BUFFER 1 OF 5
U4
CPU_CLK
PCI_IRDY_
PCI_TRDY_
CPU_PAR_ERR_
SBE_
MEM_ERR_
663_CPU_PAR_ERR*
663_SBE*
663_MEM_ERR*
7C7<
AOS_RR_MMRS
ROM_LOAD
+3.3V
R6 10K
R96 1K
R48 10K
R56 1K
J6
BERG4X3
A B C
CONFIG JUMPERS
R7 R55 R47 R40 10K
R68 R77 R85 R8 1K
R5 R4 R2 R3 22
R66 R10 R16 R21 R38 R45 R53 R9 22
IN
663_CPU_CLK 15C1>
PCI_IRDY* 18B2<> 9C2<>
PCI_TRDY* 18B2<> 9C2<>
AOS_RR_MMRS 7C1>
ROM_LOAD 7C1>
J6 SETTINGS:
PIN B1: UP=603 IN 1-TO-1 MODE
DOWN=NOT 603 IN 1-TO-1 MODE
PIN B2: UP=REMOTE ROM
DOWN=LOCAL ROM
IBM
663/664 BUFFER CONTROL AND MEMORY INTERFACE
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:40 1995
SHEET 8 OF

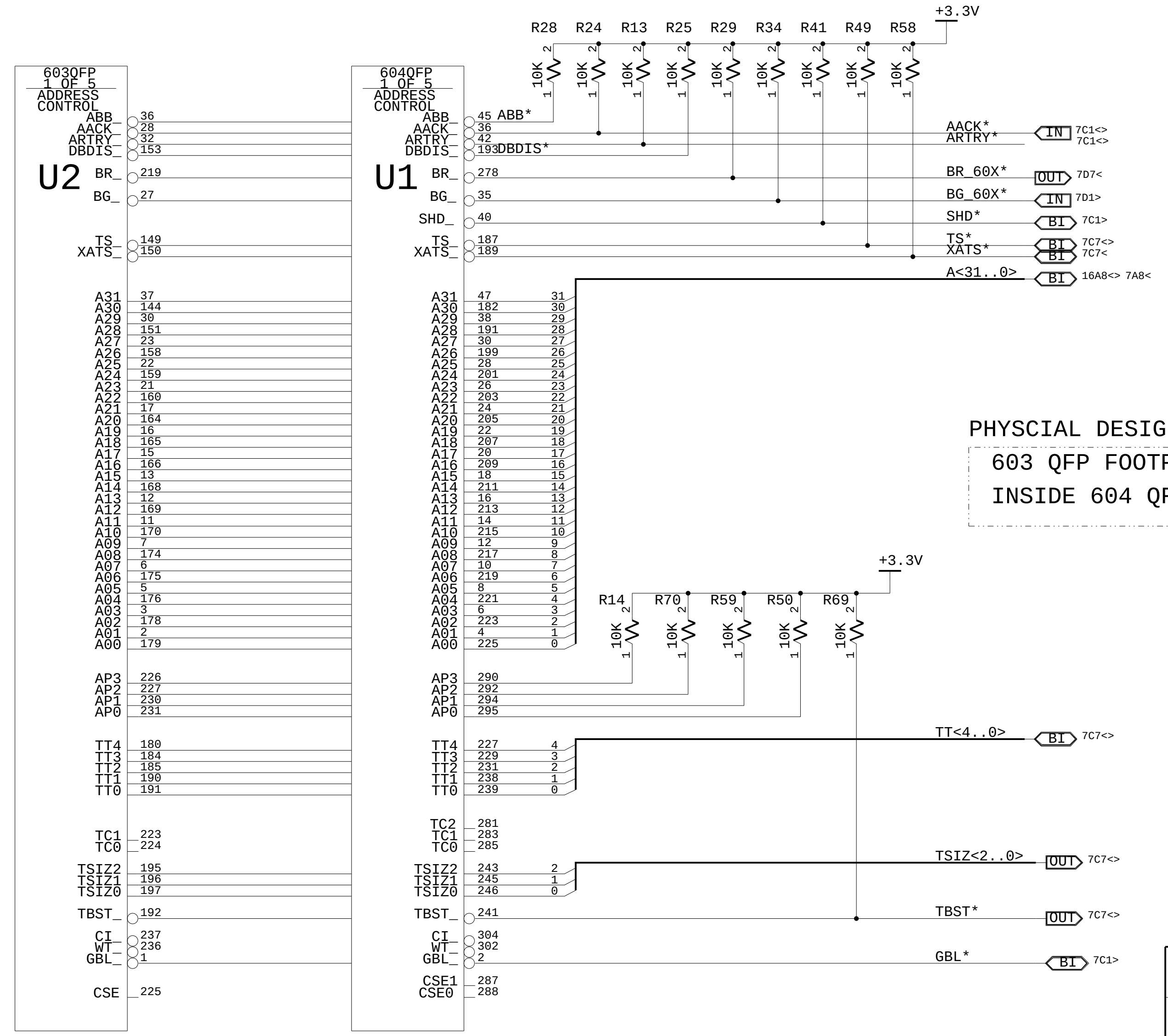


NOTE: IF IBM27-82376 IS USED,
IGN_PCI_AD31 SHOULD
BE PULLED DOWN.
IF 82378ZB IS USED,
IGN_PCI_AD31 SHOULD
BE DRIVEN BY U18.
(SEE P.18)
R37
SEE_NOTE
IGN_PCI_AD31
IN 18A2>
PCI_LOCK*
IN
NMI_FROM_ISABRDG
IN 20B1>
INT_TO_664
IN 20B1>
664_PCI_CLK
IN 15A1>
U4
663
BUFFER
4 OF 5
PCI_AD31 MSB
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0 LSB
664
CONTROLLER
4 OF 4
U3
PCI_CLK
INT_REQ
NMI_REQ
PCI_LOCK_
IGN_PCI_AD31
PCI_AD31 MSB
PCI_AD0 LSB
PCI
INTERFACE
PCI_PAR
PCI_FRAME_
PCI_TRDY_
PCI_IRDY_
PCI_STOP_
PCI_DEVSEL_
PCI_C/BE3
PCI_C/BE2
PCI_C/BE1
PCI_C/BE0
PCI_PERR_
PCI_SERR_
PCI_FRAME*
BI 18B2<>
PCI_TRDY*
BI 18B2<> 8A5<
PCI_IRDY*
BI 18B2<> 8A5<
PCI_STOP*
BI 18B2<>
PCI_DEVSEL*
BI 18B2<>
PCI_C/BE<3..0>*
BI 18B2<>
PCI_PERR*
BI 21D1>
PCI_SERR*
BI 18C7<
18C7< 23B7<> 18D2<>
BI
PCI_AD<31..0>
PCI ADDR/DATA, MSB 31, LSB 0
EVEN PARITY
18C2>
BI
PCI_PAR
IBM
663/664
PCI BUS SECTION
AND TEST POINTS
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:42 1995
SHEET 9 OF



6A7<> 4D4<> BI MD<63..0> ECL 3
MEM DATA, MSB 63, LSB 0
MEM DATA PARITY, MSB 7, LSB 0
ODD PARITY OR ECC ON MEMORY BUS
6A7<> 4D4<> BI MDP<7..0> ECL 3
663_DATA<63..0>
CPU D(0:72) ORDER
R604 33 RPAC
R612 33 RPAC
R620 33 RPAC
R628 33 RPAC
R636 33 RPAC
R644 33 RPAC
R652 33 RPAC
R660 33 RPAC
R668 33 RPAC
R600 33 RPAC
R608 33 RPAC
R616 33 RPAC
R624 33 RPAC
R632 33 RPAC
R640 33 RPAC
R648 33 RPAC
R656 33 RPAC
R664 33 RPAC
663 BUFFER 2 OF 5 U4
CPU_DATA0 MSB
CPU_DATA63 LSB
PARITY
CPU_DPAR0 MSB
CPU_DPAR7 LSB
663 BUFFER 3 OF 5 U4
MEM_DATA63 MSB
MEM_DATA0 LSB
PARITY
MEM_CHECK7 MSB
MEM_CHECK0 LSB
PAR7: MD(63:56)
PAR0: MD(7:0)
PLACE SERIES TERMINATING RESISTORS ON CPU DATA AND DATA PARITY LINES, AS CLOSE TO 82663 AS POSSIBLE.
60X DATA, MSB 0, LSB 63
60X DATA PARITY, MSB 0, LSB 7
ODD PARITY ON CPU BUS
663_DP<7..0>
17D1<> 13D1<> BI D<63..0>
17D1<> 13B1<> BI DP<7..0>
IBM
664 BUFFER DATA
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:49 1995
SHEET 10 OF


U1
604QFP
4 OF 5
U2
603QFP
4 OF 5
+3.3V
663
BUFFER
5 OF 5
U4
POWER
CONNECTIONS
VDD
GND
664
CONTROLLER
3 OF 4
U3
POWER
CONNECTIONS
FIDUCIALS
F1 F2 F3 F4
AVDD
AVDD1
R136
10
C1
C2
C3
0.01UF
0.1UF
10UF
PD NOTE:
PLACE
DECOUPLING
CIRCUIT
AS CLOSE AS
POSSIBLE
TO AVDD PIN
ON QFP PACKAGES
IBM
CEC PWR/GNDS
AND DECOUPLING
SIZE
B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:32:59 1995
SHEET 11 OF



PHYSCIAL DESIGN NOTE:

603 QFP FOOTPRINT CAN BE PLACED INSIDE 604 QFP FOOTPRINT

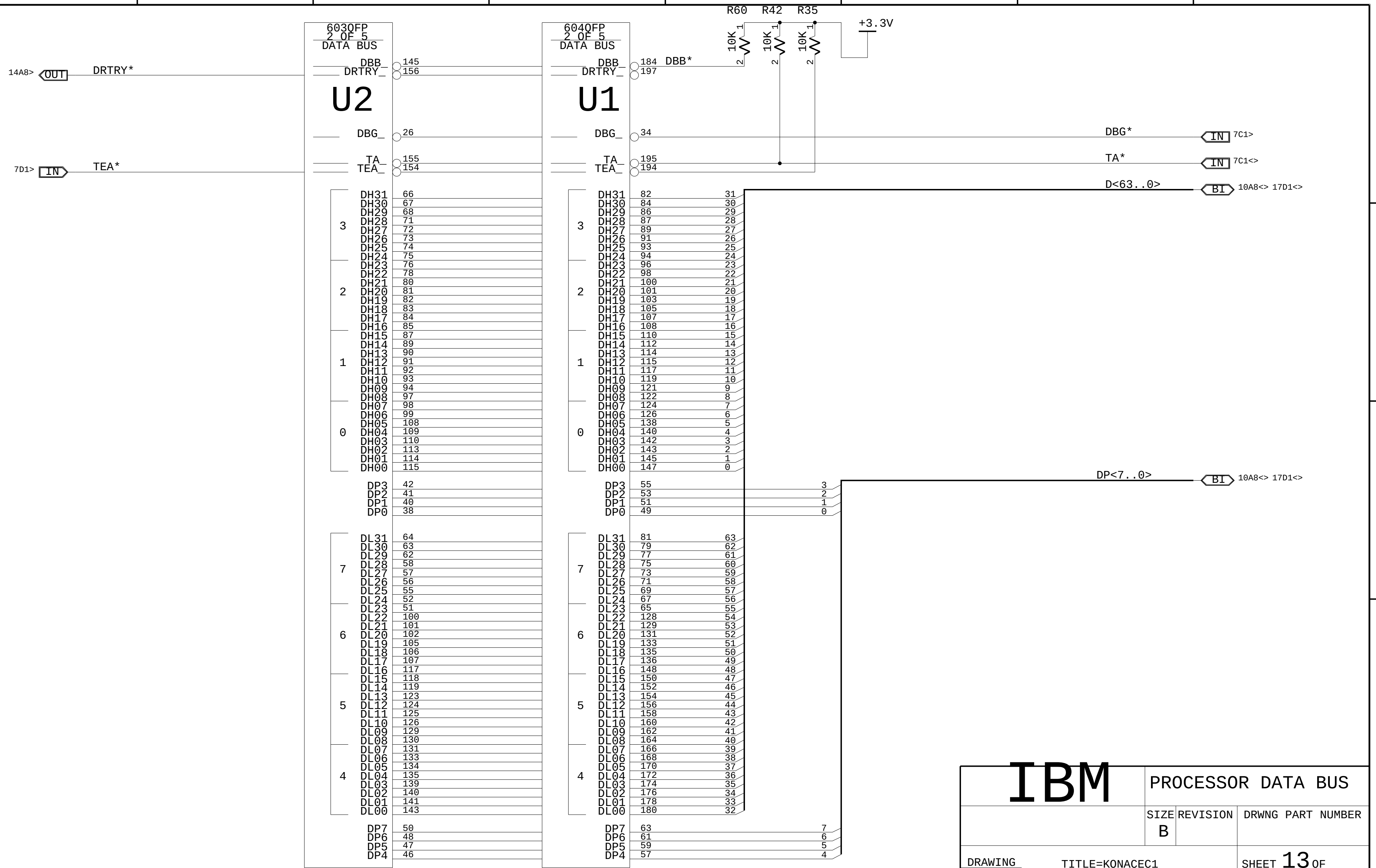
IBM

PROCESSOR DATA BUS

SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:03 1995

SHEET 12 OF



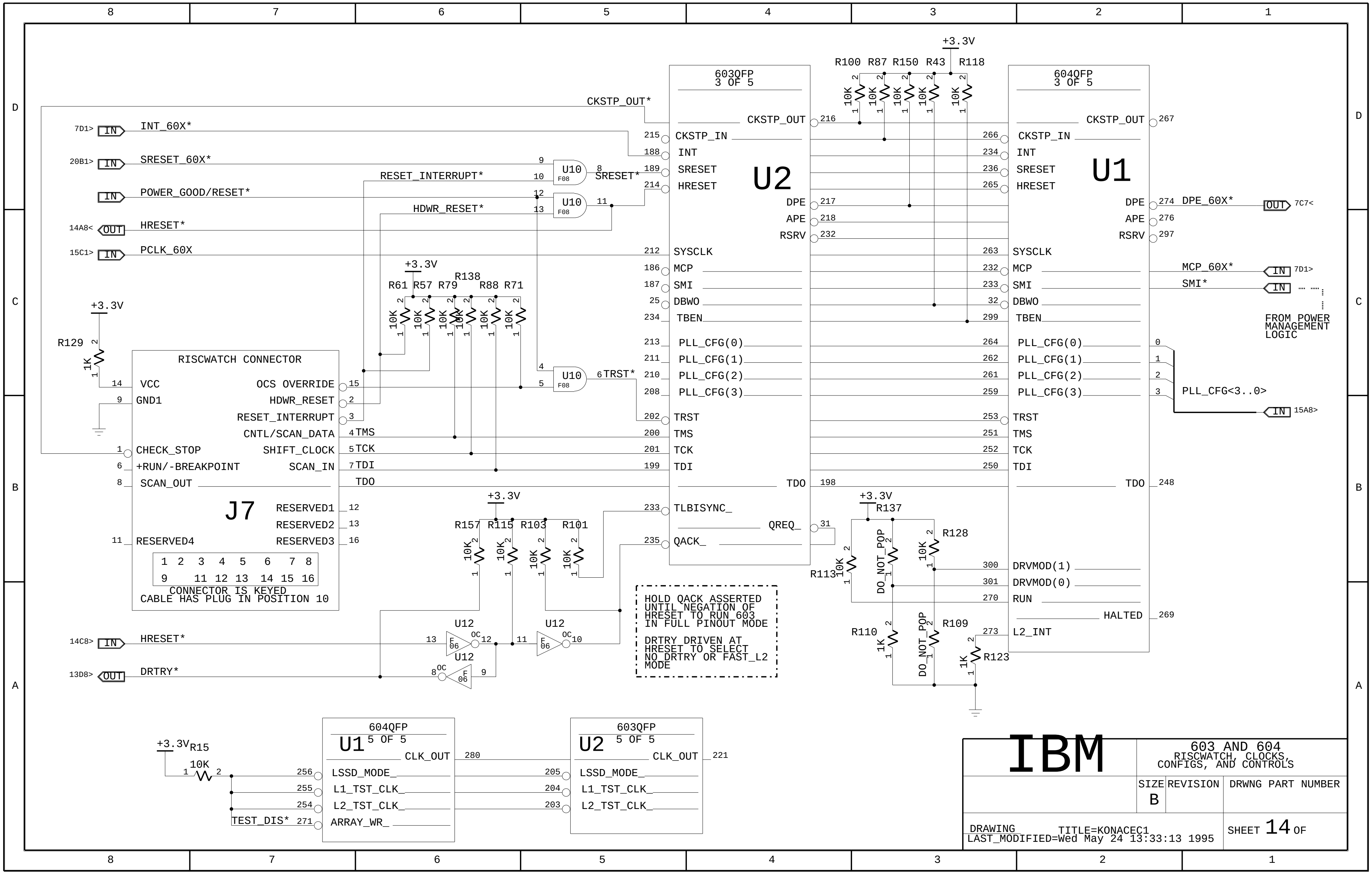
IBM

PROCESSOR DATA BUS

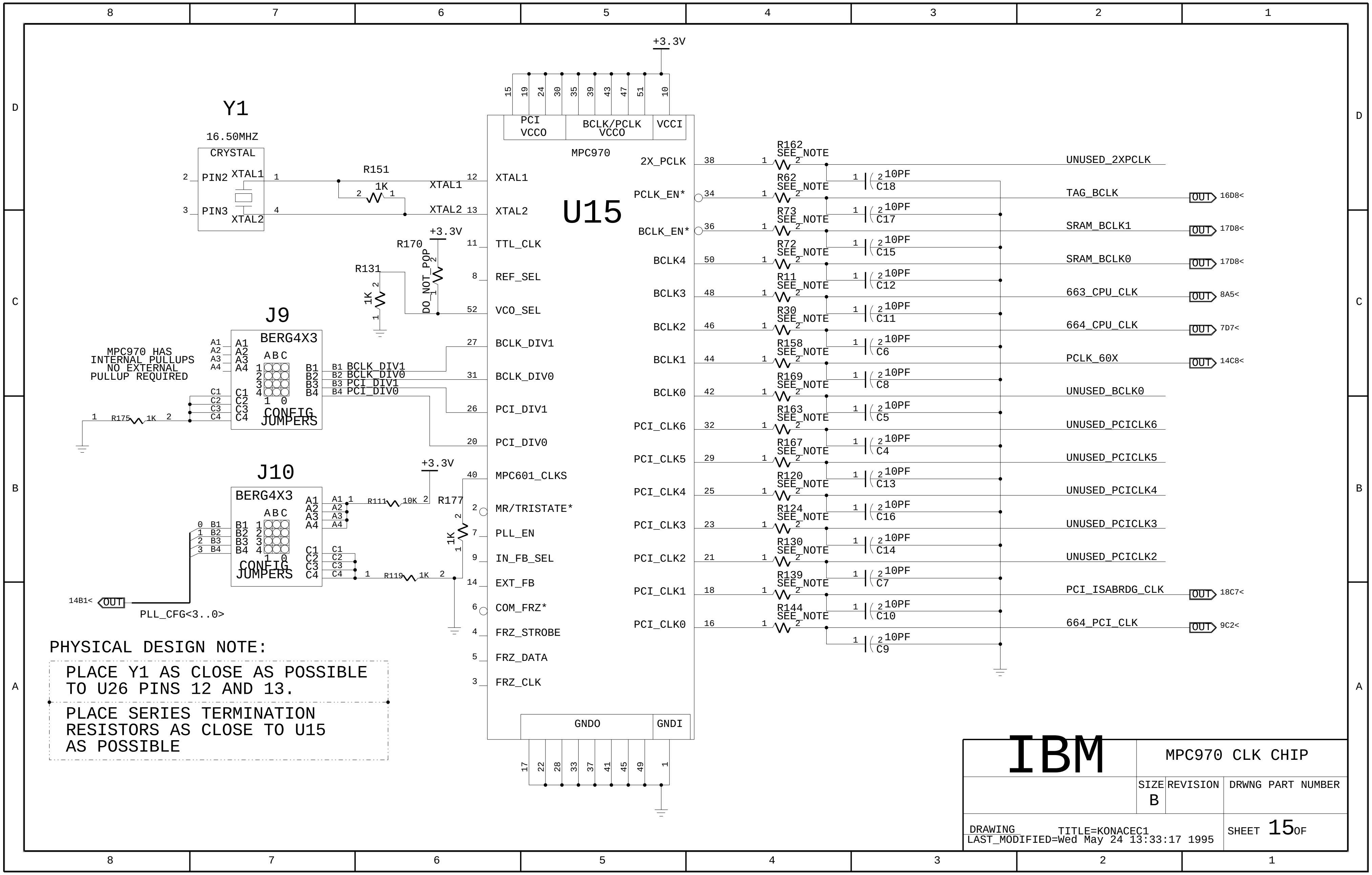
SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:08 1995

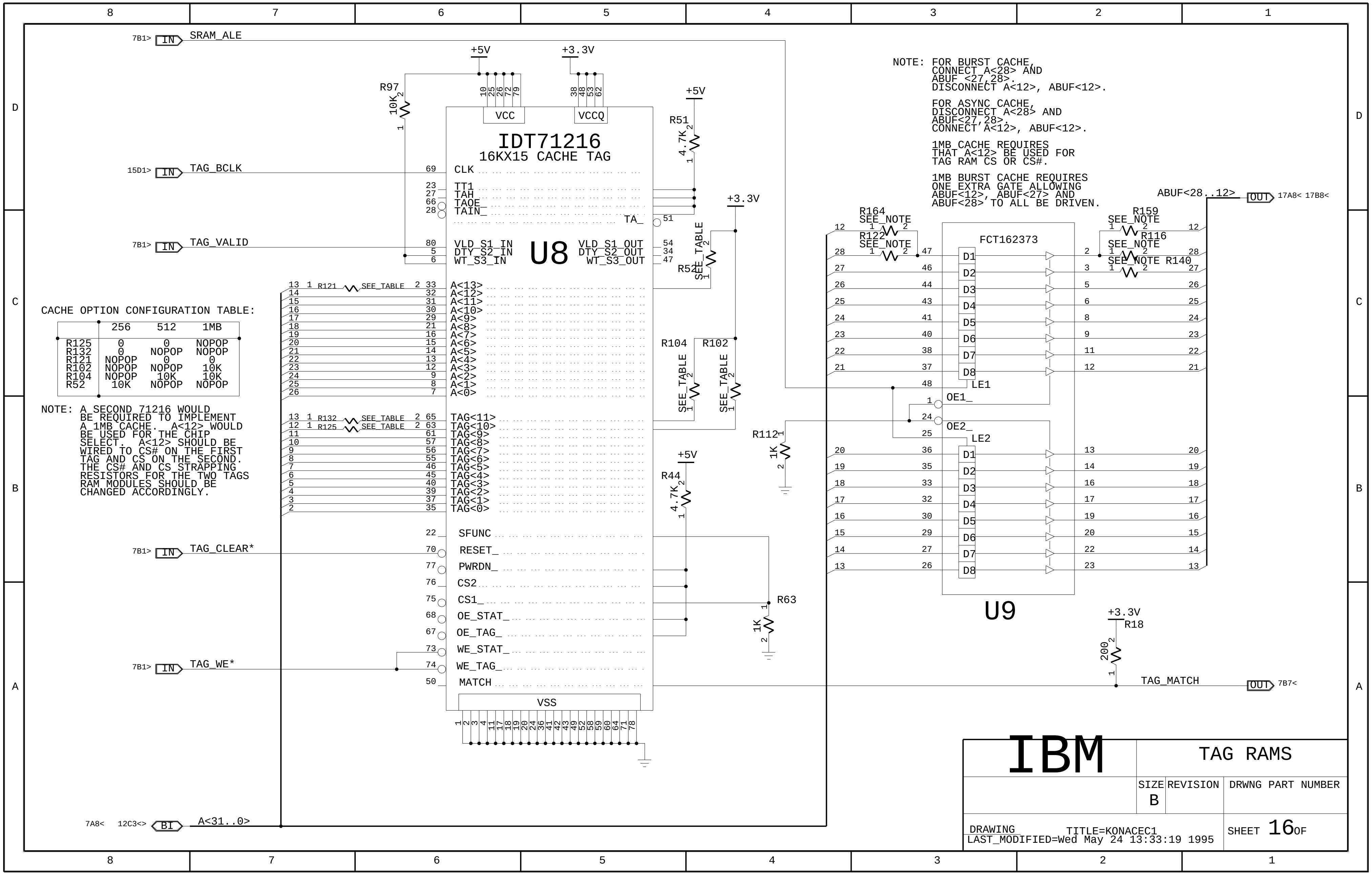
SHEET 13 OF



603QFP 3 OF 5
U2
CKSTP_OUT
CKSTP_IN
INT
SRESET
HRESET
DPE
APE
RSRV
SYSCLK
MCP
SMI
DBWO
TBEN
PLL_CFG(0)
PLL_CFG(1)
PLL_CFG(2)
PLL_CFG(3)
TRST
TMS
TCK
TDI
TDO
TLBISYNC_
QREQ_
QACK_
604QFP 3 OF 5
U1
DRVMOD(1)
DRVMOD(0)
RUN
HALTED
L2_INT
CKSTP_OUT*
INT_60X*
SRESET_60X*
RESET_INTERRUPT*
POWER_GOOD/RESET*
HDWR_RESET*
HRESET*
PCLK_60X
SRESET*
TRST*
U10
F08
DPE_60X*
MCP_60X*
SMI*
FROM POWER MANAGEMENT LOGIC
PLL_CFG<3..0>
+3.3V
R100 R87 R150 R43 R118
R61 R57 R79 R138 R88 R71
R129
1K
10K
RISCWATCH CONNECTOR
VCC
GND1
OCS OVERRIDE
HDWR_RESET
RESET_INTERRUPT
CNTL/SCAN_DATA
CHECK_STOP
SHIFT_CLOCK
+RUN/-BREAKPOINT
SCAN_IN
SCAN_OUT
J7
RESERVED1
RESERVED2
RESERVED3
RESERVED4
TMS
TCK
TDI
TDO
1 2 3 4 5 6 7 8
9 11 12 13 14 15 16
CONNECTOR IS KEYED
CABLE HAS PLUG IN POSITION 10
R157 R115 R103 R101
R137
R128
R113
DO_NOT_POP
R110
R109
R123
U12
DRTRY*
HOLD QACK ASSERTED UNTIL NEGATION OF HRESET TO RUN 603 IN FULL PINOUT MODE
DRTRY DRIVEN AT HRESET TO SELECT NO DRTRY OR FAST_L2 MODE
604QFP 5 OF 5
U1
CLK_OUT
LSSD_MODE_
L1_TST_CLK_
L2_TST_CLK_
ARRAY_WR_
TEST_DIS*
R15
603QFP 5 OF 5
U2
IBM
603 AND 604
RISCWATCH, CLOCKS, CONFIGS, AND CONTROLS
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:13 1995
SHEET 14 OF



+3.3V
Y1
16.50MHZ
CRYSTAL
PIN2 XTAL1
PIN3 XTAL2
R151
1K
XTAL1
XTAL2
U15
MPC970
PCI VCCO
BCLK/PCLK VCCO
VCCI
R170
DO_NOT_POP
R131
1K
J9
BERG4X3
MPC970 HAS INTERNAL PULLUPS NO EXTERNAL PULLUP REQUIRED
CONFIG JUMPERS
R175 1K
BCLK_DIV1
BCLK_DIV0
PCI_DIV1
PCI_DIV0
J10
BERG4X3
CONFIG JUMPERS
R111 10K
R177
R119 1K
PLL_CFG<3..0>
14B1< OUT
XTAL1
XTAL2
TTL_CLK
REF_SEL
VCO_SEL
BCLK_DIV1
BCLK_DIV0
PCI_DIV1
PCI_DIV0
MPC601_CLKS
MR/TRISTATE*
PLL_EN
IN_FB_SEL
EXT_FB
COM_FRZ*
FRZ_STROBE
FRZ_DATA
FRZ_CLK
GNDO
GNDI
2X_PCLK
PCLK_EN*
BCLK_EN*
BCLK4
BCLK3
BCLK2
BCLK1
BCLK0
PCI_CLK6
PCI_CLK5
PCI_CLK4
PCI_CLK3
PCI_CLK2
PCI_CLK1
PCI_CLK0
R162 SEE_NOTE
R62 SEE_NOTE
R73 SEE_NOTE
R72 SEE_NOTE
R11 SEE_NOTE
R30 SEE_NOTE
R158 SEE_NOTE
R169 SEE_NOTE
R163 SEE_NOTE
R167 SEE_NOTE
R120 SEE_NOTE
R124 SEE_NOTE
R130 SEE_NOTE
R139 SEE_NOTE
R144 SEE_NOTE
10PF C18
10PF C17
10PF C15
10PF C12
10PF C11
10PF C6
10PF C8
10PF C5
10PF C4
10PF C13
10PF C16
10PF C14
10PF C7
10PF C10
10PF C9
UNUSED_2XPCLK
TAG_BCLK OUT 16D8<
SRAM_BCLK1 OUT 17D8<
SRAM_BCLK0 OUT 17D8<
663_CPU_CLK OUT 8A5<
664_CPU_CLK OUT 7D7<
PCLK_60X OUT 14C8<
UNUSED_BCLK0
UNUSED_PCICLK6
UNUSED_PCICLK5
UNUSED_PCICLK4
UNUSED_PCICLK3
UNUSED_PCICLK2
PCI_ISABRDG_CLK OUT 18C7<
664_PCI_CLK OUT 9C2<
PHYSICAL DESIGN NOTE:
PLACE Y1 AS CLOSE AS POSSIBLE TO U26 PINS 12 AND 13.
PLACE SERIES TERMINATION RESISTORS AS CLOSE TO U15 AS POSSIBLE
IBM
MPC970 CLK CHIP
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:17 1995
SHEET 15 OF



NOTE: FOR BURST CACHE,
CONNECT A<28> AND
ABUF <27,28>.
DISCONNECT A<12>, ABUF<12>.

FOR ASYNC CACHE,
DISCONNECT A<28> AND
ABUF<27,28>.
CONNECT A<12>, ABUF<12>.

1MB CACHE REQUIRES
THAT A<12> BE USED FOR
TAG RAM CS OR CS#.

1MB BURST CACHE REQUIRES
ONE EXTRA GATE ALLOWING
ABUF<12>, ABUF<27> AND
ABUF<28> TO ALL BE DRIVEN.

CACHE OPTION CONFIGURATION TABLE:

	256	512	1MB
R125	0	0	NOPOP
R132	0	NOPOP	NOPOP
R121	NOPOP	0	0
R102	NOPOP	NOPOP	10K
R104	NOPOP	10K	10K
R52	10K	NOPOP	NOPOP

NOTE: A SECOND 71216 WOULD BE REQUIRED TO IMPLEMENT A 1MB CACHE. A<12> WOULD BE USED FOR THE CHIP SELECT. A<12> SHOULD BE WIRED TO CS# ON THE FIRST TAG AND CS ON THE SECOND. THE CS# AND CS STRAPPING RESISTORS FOR THE TWO TAGS RAM MODULES SHOULD BE CHANGED ACCORDINGLY.

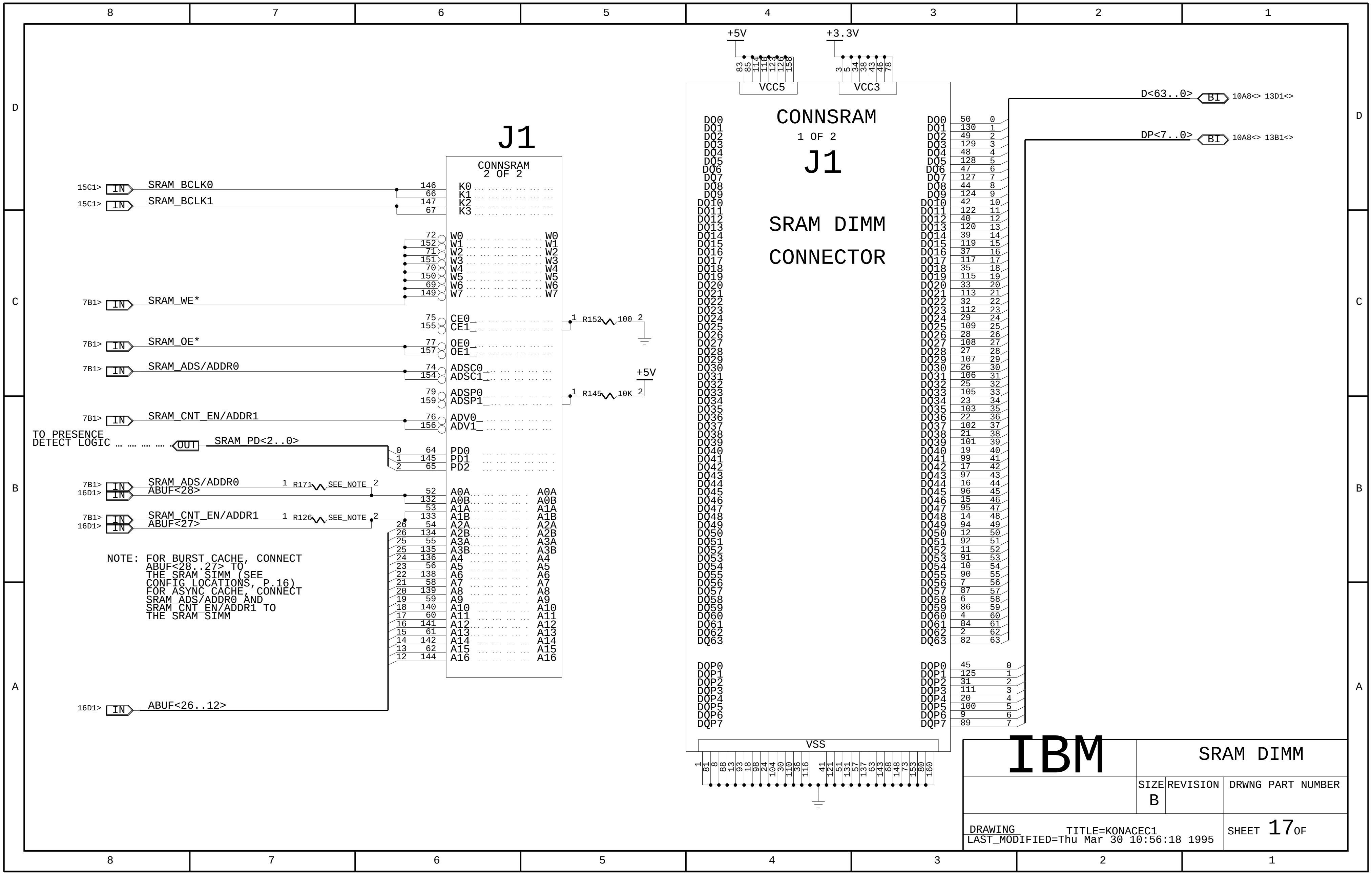
IBM

TAG RAMS

SIZE B REVISION DRWNG PART NUMBER

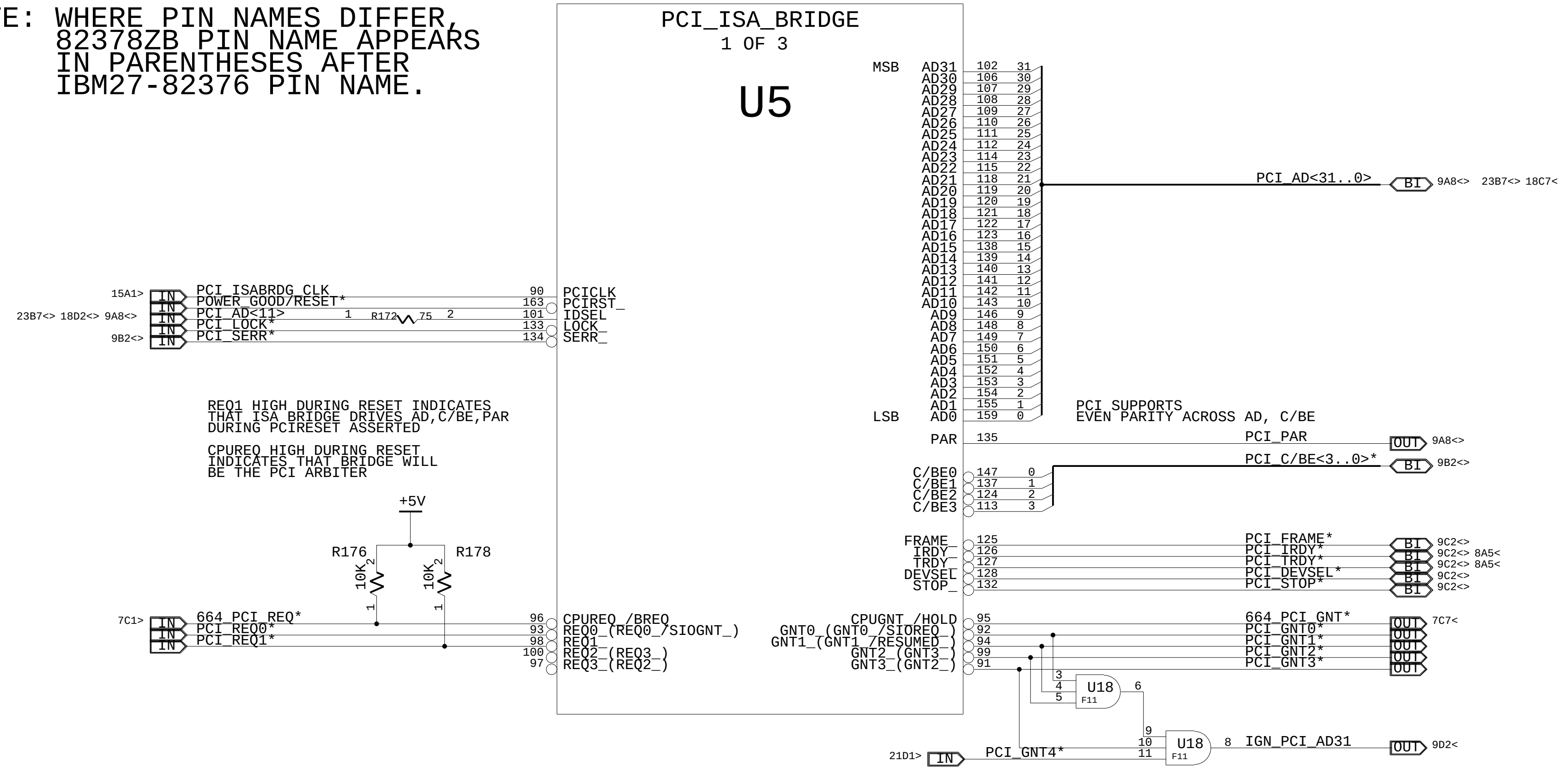
DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:19 1995

SHEET 16 OF



J1
CONNSRAM
2 OF 2
CONNSRAM
1 OF 2
J1
SRAM DIMM
CONNECTOR
+5V
+3.3V
VCC5
VCC3
VSS
SRAM_BCLK0
SRAM_BCLK1
SRAM_WE*
SRAM_OE*
SRAM_ADS/ADDR0
SRAM_CNT_EN/ADDR1
TO PRESENCE
DETECT LOGIC
SRAM_PD<2..0>
ABUF<28>
ABUF<27>
ABUF<26..12>
R171 SEE NOTE
R126 SEE NOTE
R152 100
R145 10K
D<63..0>
DP<7..0>
10A8<> 13D1<>
10A8<> 13B1<>
NOTE: FOR BURST CACHE, CONNECT
ABUF<28..27> TO
THE SRAM SIMM (SEE
CONFIG LOCATIONS, P.16)
FOR ASYNC CACHE, CONNECT
SRAM_ADS/ADDR0 AND
SRAM_CNT_EN/ADDR1 TO
THE SRAM SIMM
IBM
SRAM DIMM
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Thu Mar 30 10:56:18 1995
SHEET 17 OF

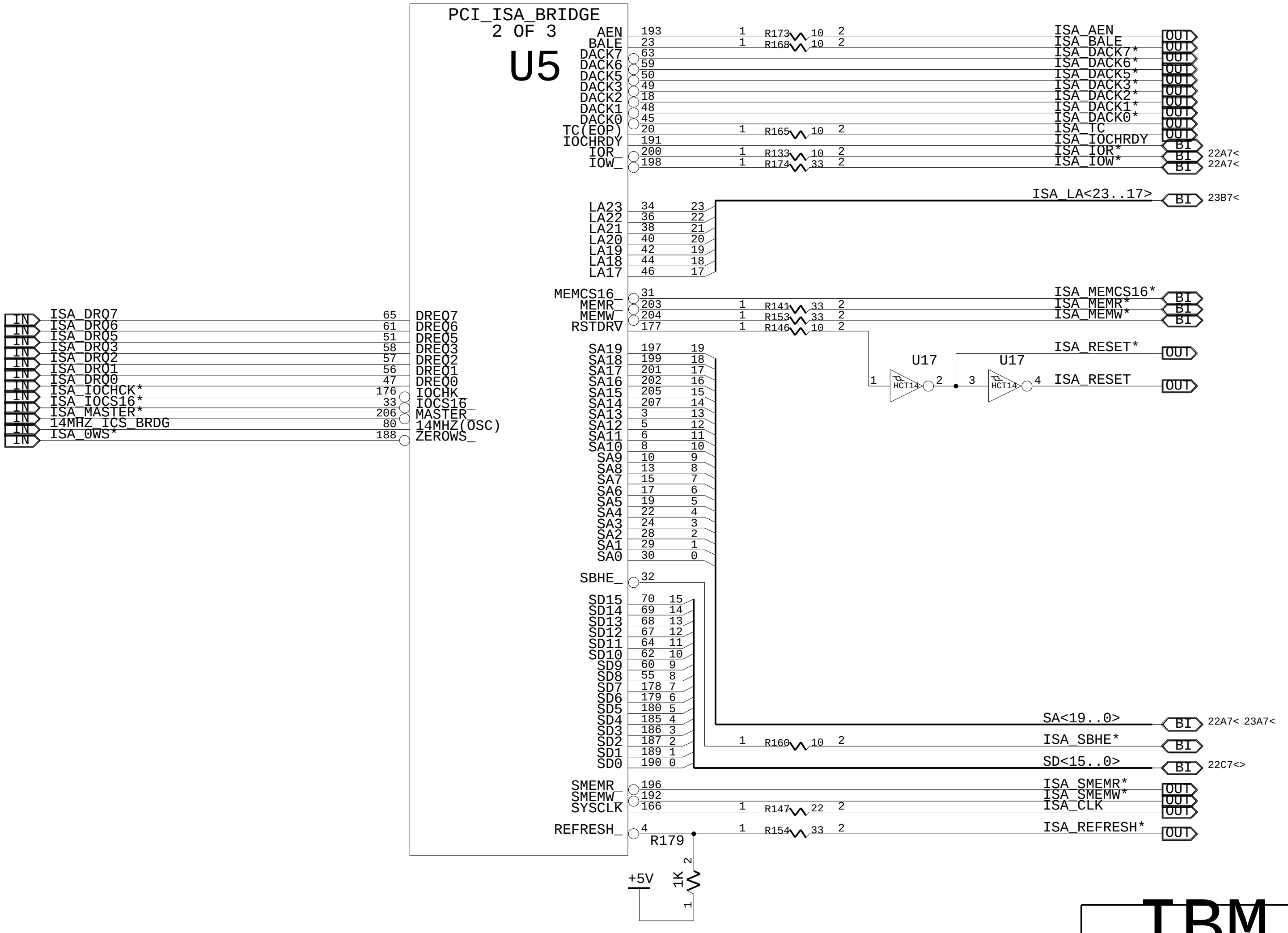
NOTE: WHERE PIN NAMES DIFFER,
82378ZB PIN NAME APPEARS
IN PARENTHESES AFTER
IBM27-82376 PIN NAME.



NOTE: CASCADING 'AND' GATES NECESSARY ONLY
IF 82378ZB IS INSTALLED. IGN_PCI_AD31
INDICATES TO 664 THAT THE PCI/ISA BRIDGE
IS THE PCI MASTER AND THAT THE BRIDGE
MAY BE RUNNING A CYCLE FOR AN ISA
MASTER.

THE USER SHOULD TAKE INTO CONSIDERATION
THE TIMING CONSTRAINTS OF THE 664
IGN_PCI_AD31 INPUT IN DESIGNING THIS
CASCADE CIRCUIT.

IBM	IBM27-82376, 82378ZB COMMON PINS-PCI PORTION		
	SIZE B	REVISION	DRWNG PART NUMBER
DRAWING TITLE=KONACEC1 LAST_MODIFIED=Thu Mar 30 10:56:59 1995			SHEET 18 OF



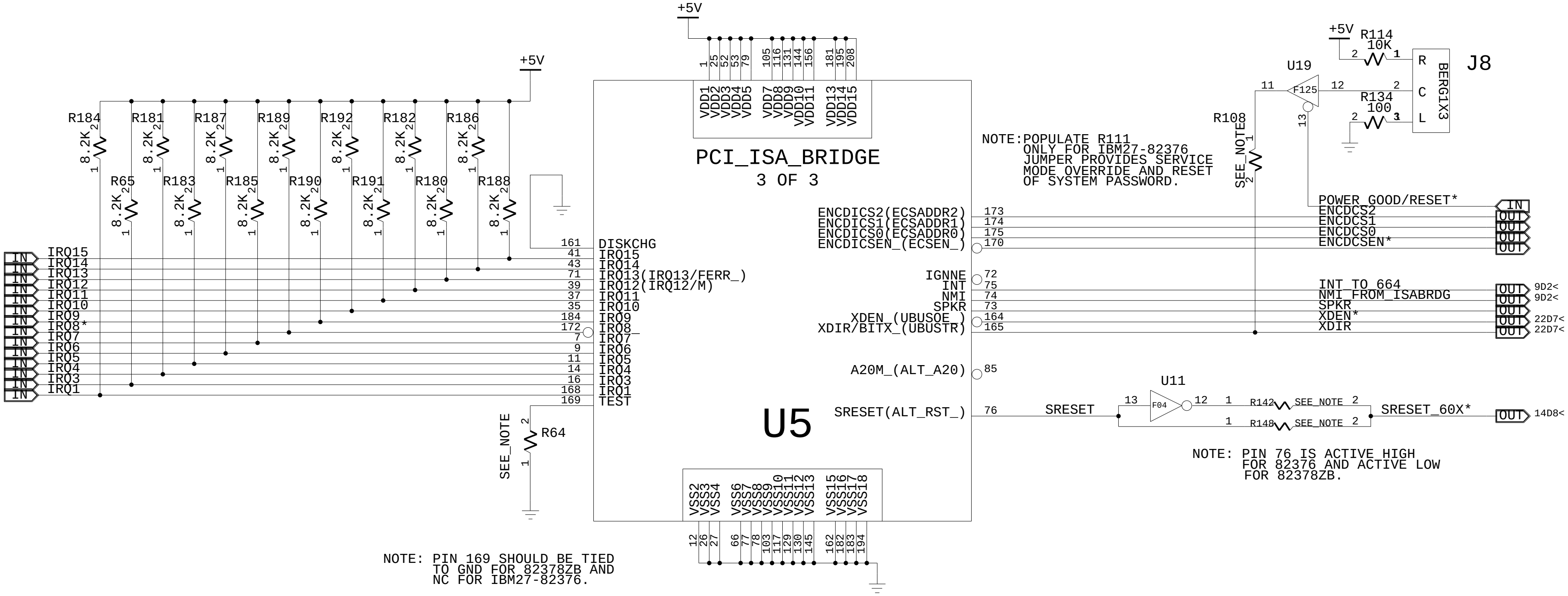
IBM

IBM27-82376, 82378ZB
COMMON PINS-ISA PORTION

SIZE	REVISION	DRWNG PART NUMBER
B		

DRAWING
TITLE=KONACEC1
LAST_MODIFIED=Thu Mar 30 10:57:13 1995

SHEET 19 OF



IBM

IBM27-82376, 82378ZB
COMMON PINS

SIZE	REVISION	DRWNG PART NUMBER
B		

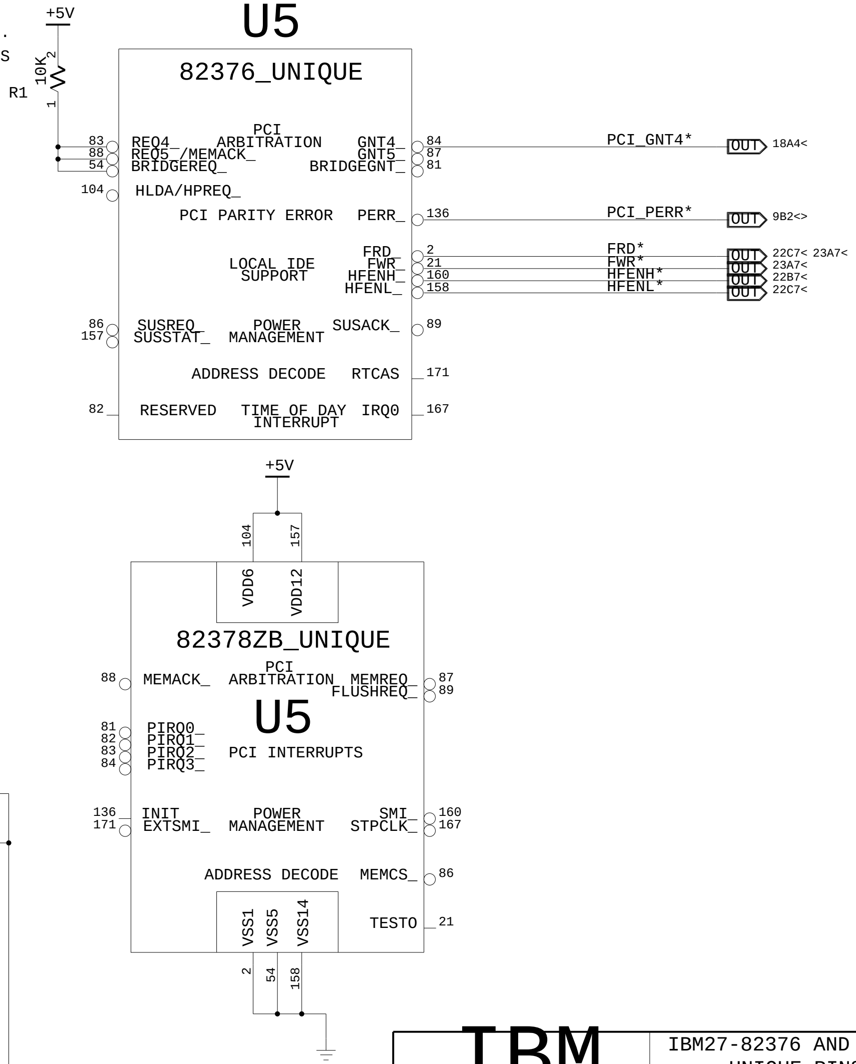
DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:01 1995

SHEET 20 OF

IBM27-82376/82378ZB COMMON PINS WITH SPECIAL CONSIDERATIONS

PIN #	82378ZB		IBM27-82376	
42	LA19	(I/O)	LA19/ROMSEC	(O)
44	LA18	(I/O)	LA18/ROMBANK	(O)
46	LA17	(I/O)	LA17	(O)
76	ALT_RST_	(O)	SRESET	(O)
85	ALT_A20_	(O)	A20M_	(O)
91	GNT2_	(O)	GNT3_	(O)
92	GNT0_/SIOREQ_	(O)	GNT0_	(O)
93	REQ0_/SIOGNT_	(I)	REQ0_	(I)
94	GNT1_/RESUME_	(O)	GNT1_	(O)
95	CPUGNT_	(O)	CPUGNT_/HOLD	(O)
96	CPUREQ_	(I)	CPUREQ_/BREQ	(I)
97	REQ2_	(I)	REQ3_	(I)
99	GNT3_	(O)	GNT2_	(O)
100	REQ3_	(I)	REQ2_	(I)
134	SERR_	(I)	SERR_	(I/O)
135	PAR	(O)	PAR	(I/O)
165	UBUSTR	(O)	XDIR/BITX_	(I/O)
169	TEST (GND)	(I)	TEST(NC)	(I)
176	IOCHK_	(I)	IOCHK_	(I/O)

NOTE: REQUEST PINS HAVE WEAK INTERNAL PULL UPS. THE USER MAY WISH TO PLACE EXTERNAL PULL UPS ON THESE PINS.



IBM27-82376/82378ZB UNIQUE PINOUT

PIN #	82378ZB	IBM27-82376	PIN #	82378ZB	IBM27-82376
2	VSS	FRD_	88	MEMACK_	REQ5_/MEMACK_
21	TESTO	FWR_	89	FLUSHREQ_	SUSACK_
54	VSS	BRIDGE_REQ_	104	VDD	HLDA/HPREQ_
81	PIRQ0_	BRIDGE_GNT_	136	INIT	PERR_
82	PIRQ1_	RESERVED	157	VDD	SUSSTAT_
83	PIRQ2_	REQ4_	158	VSS	HFENL_
84	PIRQ3_	GNT4_	160	SMI_	HFENH_
86	MEMCS_	SUSREQ_	167	STPCLK_	IRQ0
87	MEMREQ_	GNT5_/MEMREQ_	171	EXTSMI_	RTCAS

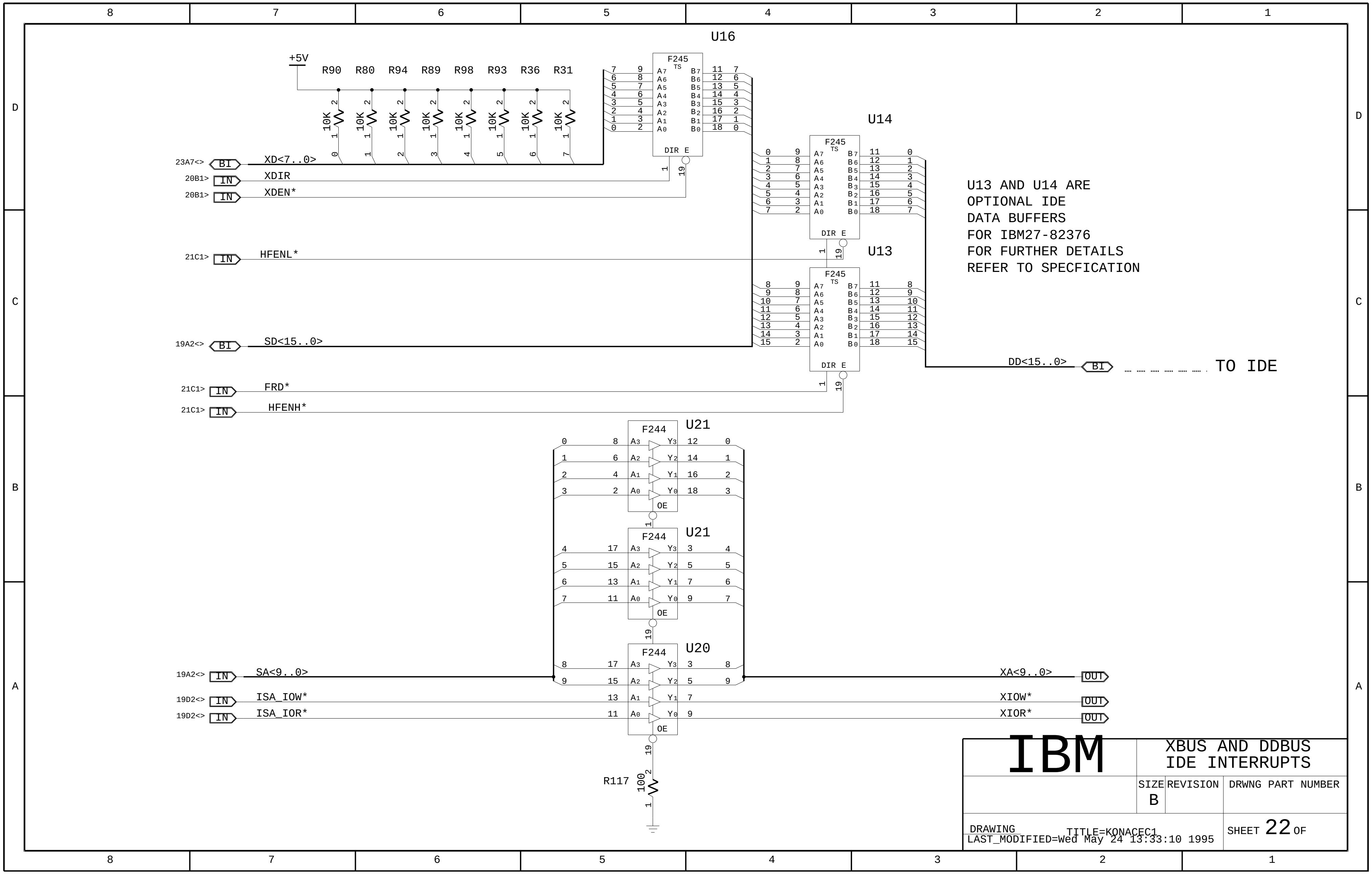
IBM

IBM27-82376 AND 82378ZB UNIQUE PINS

SIZE B | REVISION | DRWNG PART NUMBER

DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:05 1995

SHEET 21 OF


U16
F245
+5V
R90 R80 R94 R89 R98 R93 R36 R31
10K
23A7<> BI XD<7..0>
20B1> IN XDIR
20B1> IN XDEN*
U14
F245
U13 AND U14 ARE
OPTIONAL IDE
DATA BUFFERS
FOR IBM27-82376
FOR FURTHER DETAILS
REFER TO SPECFICATION
21C1> IN HFENL*
U13
F245
19A2<> BI SD<15..0>
DD<15..0> BI TO IDE
21C1> IN FRD*
21C1> IN HFENH*
U21
F244
U21
F244
U20
F244
19A2<> IN SA<9..0>
19D2<> IN ISA_IOW*
19D2<> IN ISA_IOR*
XA<9..0> OUT
XIOW* OUT
XIOR* OUT
R117
100
IBM
XBUS AND DDBUS
IDE INTERRUPTS
SIZE B
REVISION
DRWNG PART NUMBER
DRAWING TITLE=KONACEC1
LAST_MODIFIED=Wed May 24 13:33:10 1995
SHEET 22 OF

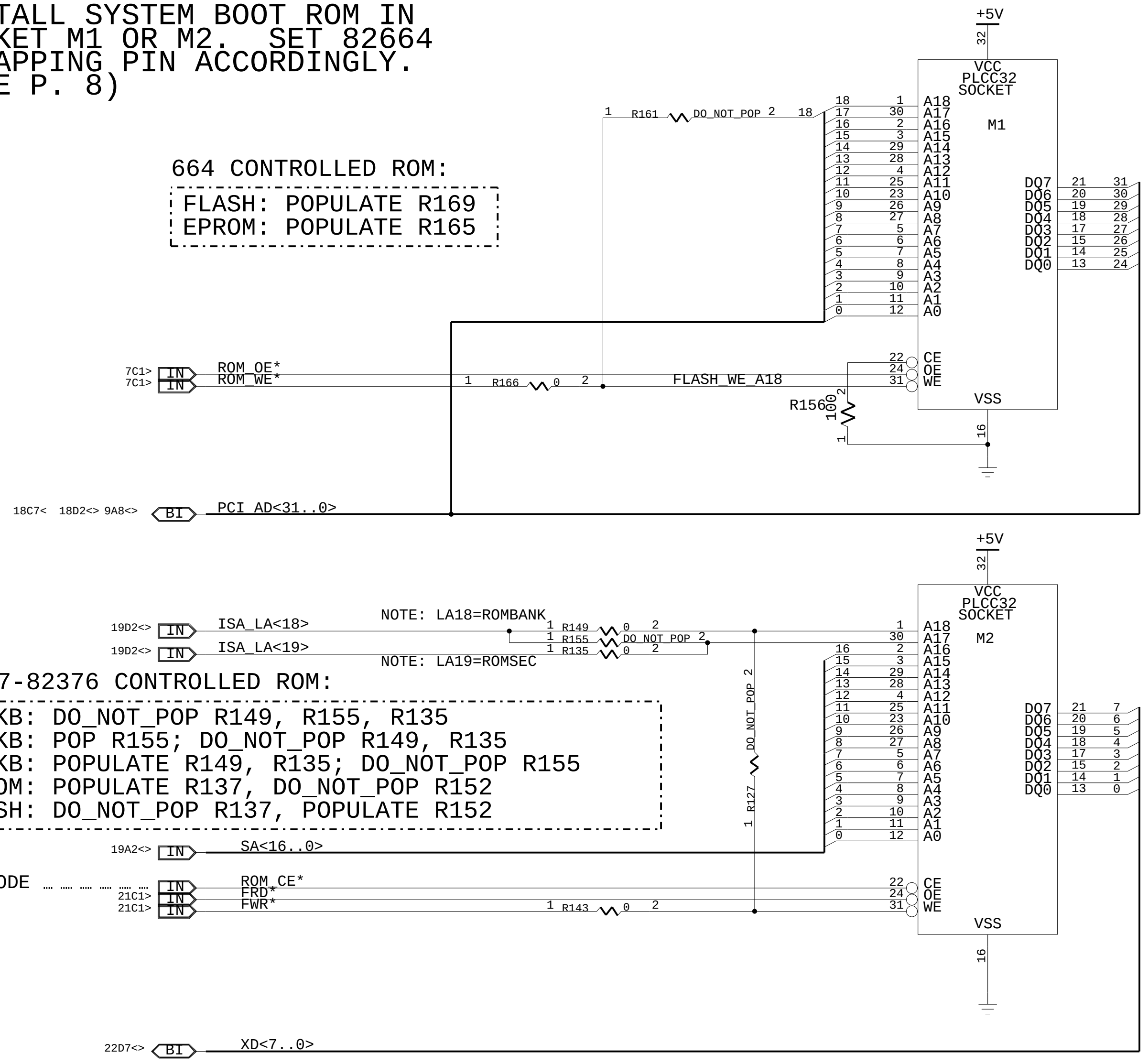
INSTALL SYSTEM BOOT ROM IN
SOCKET M1 OR M2. SET 82664
STRAPPING PIN ACCORDINGLY.
(SEE P. 8)

664 CONTROLLED ROM:

FLASH: POPULATE R169
EPROM: POPULATE R165

IBM27-82376 CONTROLLED ROM:

128KB: DO_NOT_POP R149, R155, R135
256KB: POP R155; DO_NOT_POP R149, R135
512KB: POPULATE R149, R135; DO_NOT_POP R155
EPROM: POPULATE R137, DO_NOT_POP R152
FLASH: DO_NOT_POP R137, POPULATE R152



NOTE: 664 HAS A LOCAL ROM INTERFACE THAT ALLOWS THE SYSTEM TO ACCESS A BOOT ROM WIRED TO PCI_AD<31..0>. SEE P.8 FOR THE PROPER SETTING OF JUMPER J6 TO CONFIGURE 664 FOR LOCAL ROM ACCESSES.

NOTE: 664 CAN ACCESS A BOOT ROM LOCATED ON ISA (OR SOME OTHER TERTIARY BUS) PROVIDED THAT THE PCI BRIDGE WILL DECODE ROM CYCLES TO THE UPPER 2MB OF THE 4GB ADDRESS SPACE. IBM27-82376 WILL DECODE ROM CYCLES IN THIS ADDRESS RANGE. SEE P.8 FOR THE PROPER SETTING OF JUMPER J6 TO CONFIGURE 664 FOR REMOTE ROM ACCESSES.

IBM	664 LOCAL BOOT ROM IBM27-82376 ISA BOOT ROM		
	SIZE B	REVISION	DRWNG PART NUMBER
DRAWING TITLE=KONACEC1 LAST_MODIFIED=Wed May 24 13:33:15 1995			SHEET 23 OF

```
*** Signal Cross-Reference ***
   --- for the entire design --

14MHZ_ICS_BRDG  19C8<
663_CPU_CLK     15C1> 8A5<
663_CPU_PAR_ERR * 8C1> 7C7<
663_DATA <63..0> 10D6
663_DP <7..0>   10A5
663_MEM_ERR *   8C1> 7C7<
663_SBE *       8C1> 7C7<
664_CPU_CLK     15C1> 7D7<
664_PCI_CLK     15A1> 9C2<
664_PCI_GNT *   18B2> 7C7<
664_PCI_REQ *   7C1> 18B7<
664_STOP_CLK_EN * 7D7<
A <31..0>       12C3<> 16A8<> 7A8<
AACK *          7C1<> 12D3<
ABB *           12D6
ABUF <28..12>   16D1> 17A8< 17B8<
AOS_RR_MMRS     7C1> 8A5<
ARTRY *         7C1<> 12D3>
AVDD            11A4
BCLK_DIV0       15C7
BCLK_DIV1       15C7
BG_60X *        7D1> 12D3<
BG_MASTER *     7D1>
BR_60X *        12D3> 7D7<
BR_MASTER *     7D7<
C2P_WRL_OPEN    8B6
CKSTP_OUT *     14D5
CPU_DATA_OE *   8B6
CPU_RDL_OPEN    8B6
CRS_C2PWXS      8B6
D <63..0>       10A8<> 13D1<> 17D1<>
DBB *           13D5
DBDIS *         12D6
DBG *           7C1> 13D1<
DD <15..0>      22C2<>
DP <7..0>       10A8<> 13B1<> 17D1<>
DPE_60X *       14D1> 7C7<
DRTRY *         13D8> 14A8>
DUAL_CTRL_REF   8B6
ECC_LE_SEL      8B6
ENCDCS0         20C1>
ENCDCS1         20C1>
ENCDCS2         20C1>
ENCDCSEN *      20C1>
FLASH_WE_A18    23C5
FRD *           21C1> 22C7< 23A7<
FWR *           21C1> 23A7<
GBL *           7C1> 12A3<>
HDWR_RESET *    14C6
HFENH *         21C1> 22B7<
HFENL *         21C1> 22C7<
HRESET *        14C8> 14A8<
IGN_PCI_AD31    18A2> 9D2<
INT_60X *       7D1> 14D8<
INT_TO_664      20B1> 9D2<
IRQ1            20B8<
IRQ3            20B8<
IRQ4            20B8<
IRQ5            20B8<
IRQ6            20B8<
IRQ7            20B8<
IRQ8 *          20B8<
IRQ9            20B8<

IRQ10           20B8<
IRQ11           20B8<
IRQ12           20B8<
IRQ13           20B8<
IRQ14           20C8<
IRQ15           20C8<
ISA_0WS *       19C8<
ISA_AEN         19D2>
ISA_BALE        19D2>
ISA_CLK         19A2>
ISA_DACK0 *     19D2>
ISA_DACK1 *     19D2>
ISA_DACK2 *     19D2>
ISA_DACK3 *     19D2>
ISA_DACK5 *     19D2>
ISA_DACK6 *     19D2>
ISA_DACK7 *     19D2>
ISA_DRQ0        19C8<
ISA_DRQ1        19C8<
ISA_DRQ2        19C8<
ISA_DRQ3        19C8<
ISA_DRQ5        19C8<
ISA_DRQ6        19C8<
ISA_DRQ7        19C8<
ISA_IOCHCK *    19C8<
ISA_IOCHRDY     19D2<>
ISA_IOCS16 *    19C8<
ISA_IOR *       19D2<> 22A7<
ISA_IOW *       19D2<> 22A7<
ISA_LA <23..17> 19D2<> 23B7<
ISA_MASTER *    19C8<
ISA_MEMCS16 *   19C2<>
ISA_MEMR *      19C2<>
ISA_MEMW *      19C2<>
ISA_REFRESH *   19A2>
ISA_RESET       19C2>
ISA_RESET *     19C2>
ISA_SBHE *      19A2<>
ISA_SMEMR *     19A2>
ISA_SMEMW *     19A2>
ISA_TC          19D2>
L2_CLAIM *      7B7<
MA <11..0>      8D4> 5B7< 6B7<
MCE <7..0> *    8D4> 5D7< 6C7<
MCP_60X *       7D1> 14C1<
MD <63..0>      4D4<> 6A7<> 10D8<>
MDP <7..0>      4D4<> 6A7<> 10D8<>
MEM_BE <3..0>   8B6 8C6
MEM_DATA_OE *   8B6
MEM_RD_SMPL     8B6
MEM_WRL_OPEN    8B6
MPD <23..0>     5A2> 6D2>
MRE <3..0> *    8D4> 5C7< 5D7< 6D7<
MWE0 *          8D4> 5A7< 6C7<
MWE1 *          8D4> 5A7< 6D7<
MWS_P2MRXS      8B6
NMI_FROM_ISABRDG 20B1> 9D2<
PCI_AD <31..0>  9A8<> 18D2<> 23B7<> 18C7<
PCI_AD_OE *     8B6
PCI_C/BE <3..0> * 9B2<> 18B2<>
PCI_DEVSEL *    9C2<> 18B2<>
PCI_DIV0        15B7
PCI_DIV1        15C7
PCI_EXT_SEL     8B6
PCI_FRAME *     9C2<> 18B2<>
PCI_GNT0 *      18B2>

PCI_GNT1 *      18B2>
PCI_GNT2 *      18B2>
PCI_GNT3 *      18B2>
PCI_GNT4 *      21D1> 18A4<
PCI_IRDY *      9C2<> 18B2<> 8A5<
PCI_ISABRDG_CLK 15A1> 18C7<
PCI_LOCK *      9D2< 18C7<
PCI_OL_OPEN     8B6
PCI_OUT_SEL     8B6
PCI_PAR         9A8<> 18C2>
PCI_PERR *      9B2<> 21D1>
PCI_REQ0 *      18B7<
PCI_REQ1 *      18B7<
PCI_SERR *      9B2<> 18C7<
PCI_STOP *      9C2<> 18B2<>
PCI_TRDY *      9C2<> 18B2<> 8A5<
PCLK_60X        15C1> 14C8<
PLL_CFG <3..0>  15A8> 14B1<
POWER_GOOD/RESET * 7D7< 14D8< 18C7< 20C1<
RESET_INTERRUPT * 14D6
ROM_CE *        23A7<
ROM_LOAD        7C1> 8A5<
ROM_OE *        7C1> 23C7<
ROM_WE *        7C1> 23C7<
SA <19..0>      19A2<> 22A7< 23A7<
SD <15..0>      19A2<> 22C7<>
SHD *           7C1> 12D3<>
SMI *           14C1<
SPKR            20B1>
SRAM_ADS/ADDR0  7B1> 17B8< 17C8<
SRAM_ALE        7B1> 16D8<
SRAM_BCLK0      15C1> 17D8<
SRAM_BCLK1      15C1> 17D8<
SRAM_CNT_EN/ADDR1 7B1> 17B8<
SRAM_OE *       7B1> 17C8<
SRAM_PD <2..0>  17B8>
SRAM_WE *       7B1> 17C8<
SRESET          20B3
SRESET *        14D5
SRESET_60X *    20B1> 14D8<
TA *            7C1<> 13D1<
TAG_BCLK        15D1> 16D8<
TAG_CLEAR *     7B1> 16B8<
TAG_MATCH       16A1> 7B7<
TAG_VALID       7B1> 16C8<
TAG_WE *        7B1> 16A8<
TBST *          7C7<> 12A3>
TCK             14B7
TDI             14B7
TDO             14B7
TEA *           7D1> 13D8<
TEST_DIS *      14A7
TMS             14B7
TRST *          14C5
TS *            7C7<> 12C3<>
TSIZ <2..0>     7C7<> 12A3>
TT <4..0>       7C7<> 12B3<>
UNUSED_2XPCLK   15D2>
UNUSED_BCLK0    15B2>
UNUSED_PCICLK2  15B2>
UNUSED_PCICLK3  15B2>
UNUSED_PCICLK4  15B2>
UNUSED_PCICLK5  15B2>
UNUSED_PCICLK6  15B2>
XA <9..0>       22A2>
XATS *          12C3<> 7C7<

XD <7..0>       22D7<> 23A7<>
XDEN *          20B1> 22D7<
XDIR            20B1> 22D7<
XIOR *          22A2>
XIOW *          22A2>
XTAL1           15D6
XTAL2           15C6
```

IBM

SIZE	REVISION	DRWNG PART NUMBER
B		
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