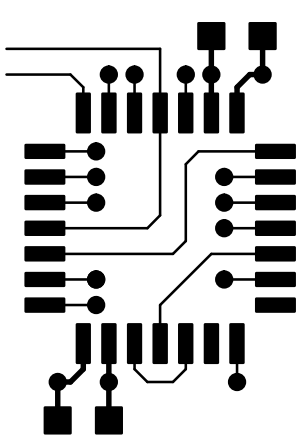
PowerPC™

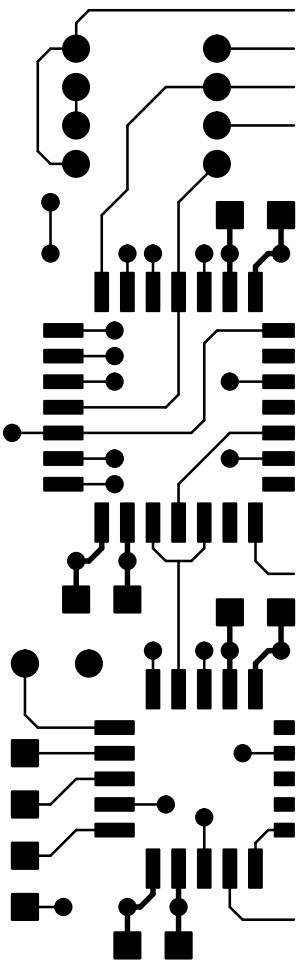
IBM27-82660 PowerPC™ to PCI Bus Bridge, Memory and L2 Controller

Product Brief

This document introduces the IBM27-82660 PowerPC to PCI Bus Bridge, Memory and L2 Controller.

MPR660PBU-00
July 7, 1995





IBM®

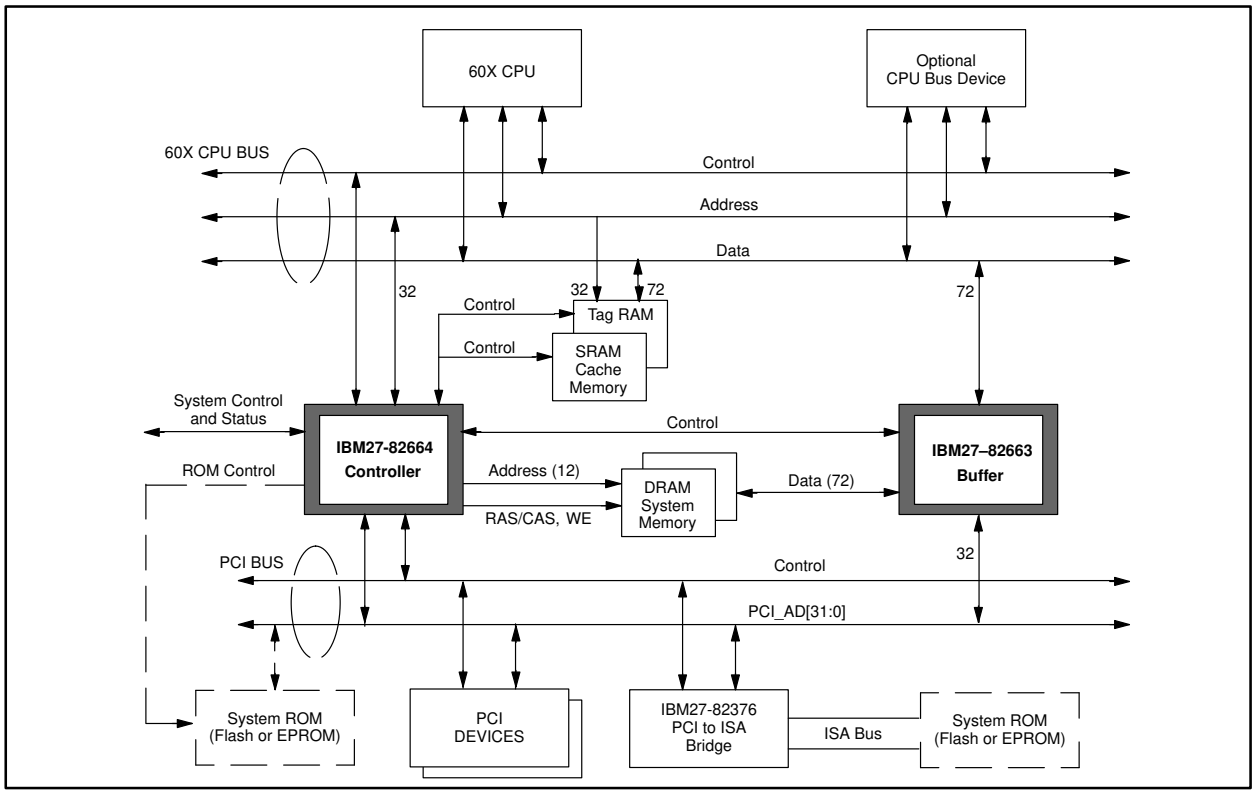


Figure 1. IBM 660 Bridge Chip Set in a Typical System Configuration

The IBM27-82660 PCI Bridge chip set (the 660 Bridge) provides an interface that can connect a PowerPC 60X CPU to high-performance peripheral component interconnect (PCI) devices such as graphics, LAN, and SCSI controllers. The 660 Bridge chip set provides the necessary control and communications logic to connect a PowerPC 60X CPU to PCI-compliant devices through the PCI bus.

The 660 Bridge chip set is comprised of the IBM27-82663 data buffer (the 663 Buffer) and the IBM27-82664 PCI and memory controller (the 664 Controller). The 660 Bridge supports the PowerPC 601, PowerPC 603, and PowerPC 604 microprocessor chips. Within this document, these three microprocessor chips are referred to generically as the 60X CPU. The 660 Bridge memory controller supports both system memory (DRAM) and level 2 (L2) cache memory. The L2 cache controller supports write-through, look-aside, direct-mapped protocols for either burst or asynchronous SRAM.

Figure 1 shows the interconnection of the 660 Bridge and the associated devices that make up a functional system. The 660 Bridge connects to the 60X CPU bus and the PCI bus. The 660 Bridge manages all communication between the 60X CPU and PCI devices. The 660 Bridge also manages system memory (DRAM), L2 cache, and ROM operations. Figure 2, on page 7, shows the various I/O signal groups.

1 The 663 Buffer

The 663 Buffer chip provides the data bus path between the 60X CPU data bus, the memory data bus, and the PCI bus. This chip also contains logic for error detection and correction, data path crossovers, and endian mode swapping. The 663 Buffer contains latches on each data bus path to improve bandwidth.

2 The 664 Controller

The 664 Controller chip contains the address bus and control logic that interfaces a PowerPC 60X processor with a PCI bus. It also contains a level 2 cache controller, a DRAM memory controller, and control logic for system central resources as required by a PowerPC reference platform compliant system.

3 Summary of 660 Bridge Features

This section summarizes the features of the 660 Bridge—including microprocessor support, the memory controller, the PowerPC CPU bus, the PCI expansion bus, the L2 cache controller, the system ROM controller, the bridge control register set, and the interrupt and exception handler.

- Complies with the PowerPC Reference Platform specification, version 1.0
- Complies with the PCI Revision 2.0 specification.

3.1 Packaging and Technology

- Designed in IBM YASU 3.3 to 3.6V CMOS4LP logic which allows I/Os that are compatible with 3.3V and 5.0V logic
- 208-pin (664 Controller) and 240-pin (663 Buffer) low-cost plastic wire-bond flatpacks
- Operates from 3.0V to 3.78V, allowing either 3.3V or 3.6V power sources.

3.2 Microprocessor Support

- Supports PowerPC 601, 603, and 604 microprocessors
- Supports 60X CPU bus speeds up to 66Mhz. Internally, the processor can run at faster frequencies
- Directly supports two 60X CPU bus masters
- Supports Little-endian and big-endian operating modes
  - Implements a byte swapper for little-endian mode
  - Support for low-order address translation (unmunging) in little-endian mode
- 64 bit wide 60X CPU data bus and 32 bit wide CPU address bus
- Utilizes address bus pipelining
- Dual bus structure between 60X CPU bus and PCI bus
- Data path latches enhance effective bandwidth
- Supports all clock modes for 60X CPUs (internal CPU clock to CPU bus)
- The MCP# signal on the 603 and 604 is supported for error reporting
- For reduced read latency, the no-DRTRY# mode of the 604 is supported
- The 603 no-DRTRY# mode is also supported except when the 603 is in 1:1 mode
- The 601 is always in DRTRY# mode
- Error reporting is by means of MCP# on the 603 and 604
- Error reporting is by means of TEA# and INT_CPU# on the 601
- The 604 store multiple 8-byte transfer is supported to the PCI bus
- Low-power mode is implemented through external clock stopping logic.

3.3 PCI Expansion Bus

- PCI bus frequency up to 33 MHz—PCI bus runs synchronously to the 60X CPU bus at one-third, one-half, or the same frequency
- 32-bit multiplexed PCI address and data path
- Support for I/O bus bridge (ISA, EISA, MicroChannel™)
- PCI to DRAM access—with L1 and L2 cache snooping
- Support for memory mapping of 60X address space into PCI transactions
  - PCI I/O reads and writes
  - PCI memory reads and writes
  - PCI configuration reads and writes
  - PCI interrupt acknowledge reads
- Supports ISA bus master access to system memory with ISA bridge on the PCI bus
- Supports contiguous ISA I/O and non-contiguous ISA I/O mappings (non-contiguous I/O so operating systems can memory-protect 32-byte blocks of ISA I/O space)
- Uses external PCI arbiter (usually from the I/O bridge chip)
- Support for PCI resource locking of system memory
- Supports type 0 and type 1 PCI configuration cycles.

3.4 Memory Controller

- Supports memory operations for the PowerPC Architecture™
- Data bus path 72 bits wide—64 data bits and eight bits of optional ECC or parity data
- Supports Eight SIMM sockets, with empty SIMM sockets allowed at any position
- Eight RAS# outputs, eight CAS# outputs, and two write-enable outputs
- Supports industry-standard 8-byte (168-pin) SIMMs of 8M, 16M, 32M, 64M, and 128M that can be individually installed for a minimum of 8M and a maximum of 1G
- Supports industry-standard 4-byte (72-pin) SIMMs of 4M, 8M, 16M, 32M, and 64M that must be installed in pairs for a minimum of 8M and a maximum of 512M
- Programmable memory timings enable optimization of DRAM timings for a large variety of 60X CPU bus frequencies, DRAM speeds, and system topologies
- Mixed use of different size SIMMs, including mixed 4-byte and 8-byte SIMMs
- Support for parity, ECC, or neither
  - Generates ECC or even parity, eight bits for eight bytes, on all memory writes
  - Checks ECC or parity eight-bytes wide on all memory reads
  - Detects and corrects all single-bit errors in ECC mode
  - Detects all two-bit errors in ECC mode
- Page-mode access—fast page-mode is supported
- Support for extended-data-out (EDO) DRAM (hyper-page mode) for higher bandwidth memory performance
- Provides row-address and column-address multiplexing for SIMMs requiring:
  - 10 row by 10 column
  - 11 row by 10 column
  - 12 row by 10 column and 11 row by 11 column (supported simultaneously)
  - 12 row by 11 column
  - 12 row by 12 column
- Non-interleaved memory access operation
- Programmable DRAM refresh timer with low-power mode
- Memory refresh address counter
- Burst-mode memory address generation logic
  - 32-byte CPU bursts to and from memory
  - Variable length PCI burst to and from memory
- Little-endian and big-endian modes
- Supports ISA master to DRAM access

If 70ns DRAM is used in a system with the 60X CPU bus at 66MHz (CPU clock period 15ns), the minimum access times when the CPU accesses system memory are as follows:

- Pipelined burst read: 4-4-4-4 CPU clocks—16 CPU clocks for 32 bytes of data
- Pipelined burst write: 5-4-4-4 CPU clocks—17 CPU clocks for 32 bytes of data

If 70ns EDO DRAM is used in a system with the 60X CPU bus at 66MHz (CPU clock period 15ns), the minimum access times when the CPU accesses system memory are as follows:

- Pipelined burst Read: 3-3-3-3 CPU clocks—12 CPU clocks for 32 bytes of data
- Pipelined burst Write: 4-3-3-3 CPU clocks—13 CPU clocks for 32 bytes of data

Other minimum memory timings are as follows:

- Pipelined L2 cache read at 66MHz with synchronous SRAM:
  3-1-1-1 -2-1-1-1- 2-1-1-1 ... 2-1-1-1
- Pipelined L2 cache read at 66MHz with asynchronous SRAM:
  3-2-2-2 -3-2-2-2 -3-2-2-2 ... -3-2-2-2
  - PCI to memory read at 66MHx CPU and 33MHz PCI
    5-1-1-1 -1-1-1-1 6-1-1-1 -1-1-1-1 6-1-1-1 -1-1-1-1 ... 6-1-1-1 -1-1-1-1
  - PCI to memory write at 66MHx CPU and 33MHz PCI
    5-1-1-1 -1-1-1-1 3-1-1-1 -1-1-1-1 3-1-1-1 -1-1-1-1 ... 3-1-1-1 -1-1-1-1.

3.5 L2 Cache Controller

- Controls external burst-mode or asynchronous SRAMs for cached data
- Controls external tag RAMs for tag information
- Look-aside, direct-mapped, and write-through protocols
- Supports all cache sizes
- Externally determined Cache size
- Responds to snoop cycles for PCI reads and writes of system memory
- Option to check parity of data stored in L2 on read cycles
- L2 cache controller can be disabled if external L2 cache is used.

3.6 System ROM Controller

- Supports ROM attached to PCI_AD bus or I/O bus such as the IBM27-82376 ISA-attached ROM (I/O bridge must support ROM addresses FFF0 0000h to FFFF FFFFh)
- Supports 8-bit ROM, flash ROM, or EPROM
  - Provides 8-bit to 64-bit conversion on reads
  - 21-bit address support for up to 2M addressable ROM
- Flash ROM write cycles generated for in-system flash ROM writes
- Flash ROM write lock-out support
- Single-beat (one-byte to eight-byte) read cycle
- Single-beat (one-byte) write cycle
- Pseudo burst-mode (32-byte) read cycle.

3.7 The Bridge Control Register Set

- Implemented PCI register model
- Includes 650 Bridge-compatible registers
- Configuration through register 0CF8h and 0CFCh configuration method
- All chip set options (except two) are configured in the register set.
  - The 603 in 1:1 mode is a strapping option.
  - Direct-attach or remote ROM is a strapping option.

3.8 Interrupt and Exception Handler

- Non-maskable error reporting by means of TEA# or MCP#
- Supports error address and control capture registers
- Reports the following types of errors:
  - Memory parity or ECC error
  - CPU illegal transfer
  - PCI bus parity error
  - CPU data bus parity error
  - PCI cycle abort
  - L2 cache parity error
  - Write to locked flash ROM
  - Memory access out of range
- Drives CPU data lines to all one-bits on out-of-range memory reads
- PCI configuration read cycles return all one-bits when no device responds.

4 Improvements Over 650 Bridge

- Includes L2 cache controller that supports synchronous and asynchronous SRAMs
- System performance improvements:
  - Programmable memory controller optimizes to memory speed and topology
  - Support for high-bandwidth memory technology (extended-data-out DRAM)
  - Up to 1G addressable DRAM
  - Utilizes 60X CPU bus address pipelining
  - Dual bus structure between 60X CPU bus and PCI bus
  - Data path latches provide bandwidth improvements
- ECC memory support
- Supports IBM27-82376 PCI/ISA bridge chip
- ROM can be attached to an ISA bus controller or to the PCI bus
- Improved clocking modes:
  - Supports 603 in 1-to-1 mode (60X internal clock vs. 60X CPU bus)
  - Support for PCI at one-third of 60X CPU bus frequency added
- The 604 store multiple 8-byte transfer is supported to the PCI bus
- Low-cost packaging—a 208-pin and a 240-pin plastic quad flatpack
- Uses an external PCI bus arbiter
- Provides basic multi-processor support
- Supports type 1 PCI configuration cycles in addition to type 0
- Implements Low-power mode
- Implements Expanded error control and reporting
- Provides a DRAM refresh timer
- Implements PCI-compatible configuration register set.

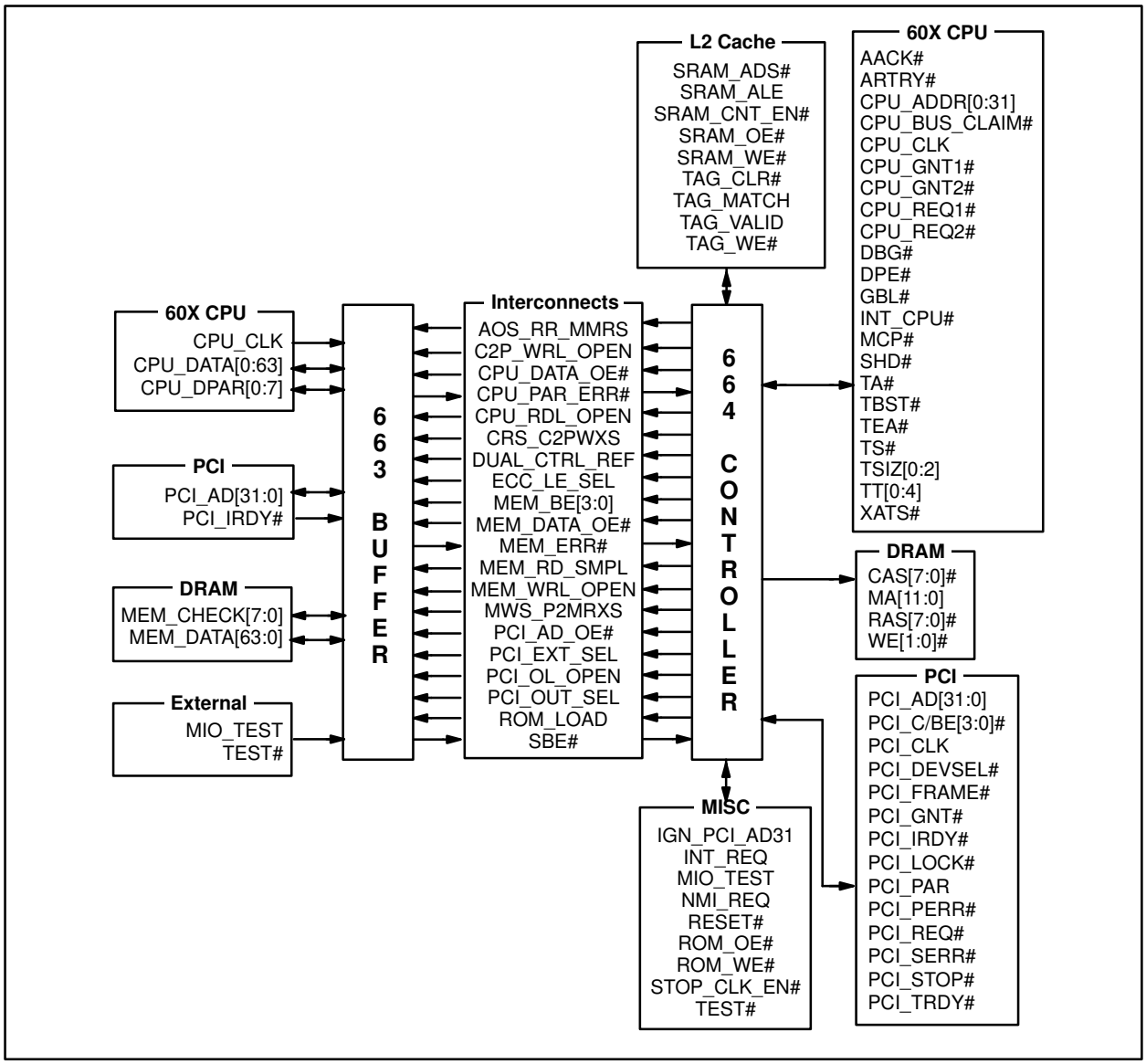


Figure 2. 660 Bridge Pin Connections

PowerPC

© International Business Machines Corporation, 1995. Printed in the United States of America 7/95. All Rights reserved.

IBM Microelectronics, PowerPC, PowerPC 601, PowerPC 603, PowerPC 604, RiscWatch, and AIX are trademarks of the IBM corporation. IBM and the IBM logo are registered trademarks of the IBM corporation. Other company names and product identifiers are trademarks of the respective companies.

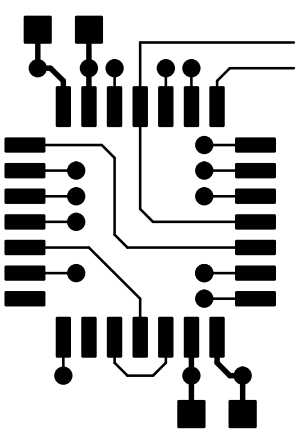
This document contains information which is subject to change by IBM without notice. IBM assumes no responsibility or liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. The products described in this document are not intended for use in implantation or other direct life-support applications where malfunction may result in physical harm or injury to persons. NO WARRANTIES OF ANY KIND, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE OFFERED IN THIS DOCUMENT.

USA and Canada:
IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC
Fax: (800) PowerFax

Japan:
IBM
800, Ichimiyake
Yasu–cho, Yasu–gun
Shiga–ken, Japan 520–23
Tel: (81) 775–87–4745
Fax: (81) 775–87–4735

Europe:
IBM
La Pompignane BP 1021
34006 Montpellier, France
Tel: (33) 6713–5757 (Français)
(33) 6713–5756 (Italiano)
Fax: (33) 6713–5750
(from Paris add 16)

Europe:
IBM
Informations Systeme GmbH
Laatzener Str. 1
30539 Hannover, Germany
Tel: (49) 511–516–3444 (English)
(49) 511–516–3555 (Deutsche)
Fax: (49) 511–516–3888



Document Number: MPR660PBU-00