Elevate your hybrid cloud with IBM z15

Jonathan Bradbury STSM Lead ISA Architect IBM Z



Co-Created with Clients

342 Clients

Sponsor User Program
IBM Z Design Council
GM Advisory Council
Cross section of user groups
(geos, industries, size)

102 Enterprises

CISO **IT Director Application Architects** Infrastructure Architects **IM/Data Architects Security Architects Z** Administrator Z SME **Z Junior System Programmer Security Administrators Application developers Line of Business Executive Cloud Architect Facilities Managers** IT Operators

15 User Personas

3x more engagement with user personas over z14, started at concept across z/OS and Linux on z, Cross-team alignment from OM, design, marketing, development, sales enablement

467
Interaction
Hours

Elevate your hybrid cloud with IBM z15









Service Level Excellence

Industry's highest level of business uptime to meet SLA and regulatory compliance

Data Protection & Privacy

Industry-first solution to protect sensitive data across your multicloud

Mission Critical Cloud

Integrate seamlessly into hybrid multicloud, blockchain and Al

Standardized & Flexible for the Cloud Data Center

Modular, scalable and proven cloud-ready infrastructure

Ready for cloud data center

Designed to align with data center trends, to optimize cost, density and flexibility

- Modular and Scalable 1-4 19" frames depending on capacity requirements
- A z15 single system performance enables reduced overall system power consumption by 40% versus the equivalent x86 configuration
- Both raised and non-raised floors as well as top and bottom exit I/O and power



Purpose built for mission-critical applications

Processor

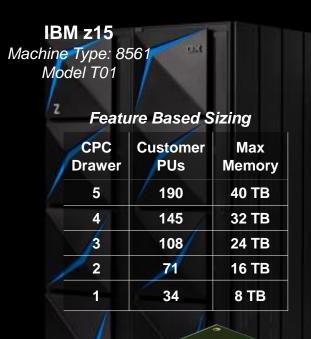
- Up to 190 client configurable cores
- 14% Single Thread Performance Improvement
- 25% maximum system capacity growth over z14
- New on-chip acceleration of compression for faster processing and more efficient storage of data
- More investments in pause-less garbage collection, 30+ new instructions codesigned and exploited by Java, and vector enhancements for analytics applications

Memory

40 TB Max Per System - RAIM Memory design

To the Data

- Significant scalability improvements up to 20% more I/O channels and 50% more logical Coupling Facility connections over z14
- Faster SSL/TLS handshake performance on z15 with Crypto Express7S compared to z14 with Crypto Express6S



15.6 miles of wires, 9.2B transistors and 26.2B wiring connections

z15 I/O Features

FICON Express16SA

zHyperLink Express1.1

OSA Express7S

25GbE & 10GbE RoCE Express2.1

Crypto Express7S

Coupling Express LR

Integrated Coupling Adapter (ICA) SR1.1

LinuxOne only: NVMe carrier & FCP Express32S





No InfiniBand Coupling Links

No zEDC card

Carry Forward:

FICON Express16S & 8S; OSA-Express6S & 5S; 25GbE & 10GbE RoCE Express2; zHyperLink Express; Crypto Express6S & 5S; Coupling Express LR; Integrated Coupling Adapter (ICA) SR

Manage huge growth of data with Pervasive Compression

Reduce data sizes by and improve workload execution time

Get started with compression now

- 6x Compression ratio for storage savings, reduced bandwidth, faster transfer times
- BSAM/QSAM compression saves space, elapsed time, and CPU.
- Compression for file transfer: Compress data with zlib 42x faster with Integrated Accelerator for zEDC compared to using software compression.

Do more without limits

- Integrated Accelerator provides better reliability and eliminates complex planning and setup
- Standard on IBM z15 replacement for zEDC Express adapter
- Full Linux virtualization 100% access for all LPARS and virtual machines
- · No change to applications is required

Optimized Security and Compliance

- Combine Pervasive Encryption with Integrated Acceleration for zEDC and get optimized and secure infrastructure
- Save CPU and cost by combining compression with Pervasive Encryption

Pervasive Encryption

Up to 17x more compression throughput than a max configured z14

Service Level Excellence

Industry's highest level of business uptime to meet SLA and regulatory compliance



IBM Z – Service Level Excellence

In today's Digital Age of "always on" interconnected networks, businesses demand near-flawless and uninterrupted connectivity to conduct business operations. This Digital Age is marked by dramatic increases in



EXTERNAL RISKS

Natural disasters and cyber threats are on the rise

> 1,500

Natural disasters in the last 5 years (EMDAT)

\$3.86 Million

Avg cost of a single data breach to companies worldwide.

(Ponemon Institute)

COSTS

The average hourly costs of downtime are immense

81% of large enterprises lose \$300,000+ per hour ...

... and **33%** lose **\$1,000,000+** per hour. (ITIC)

CUSTOMER DEMANDS

"Customers are very unforgiving if firms come up short on delivering a great experience, regardless of the nature of disruption or outage." (Forrester)

COMPLIANCE REQUIREMENTS

81% of corporations require a minimum of **99.99% uptime**

IBM Z – Transformational resilience

IBM Z is at the forefront to surpass industry availability requirements, maximizing uptime, and empowering your IT system to rapidly and autonomically recover from any disruption.

- Better throughput, less stutter
- Higher overall server hardware reliability
- Faster recovery when failures occur
- Reduce I/O latency to storage
- Concurrent maintenance improvements
- React faster to workload fluctuations
- Improved workload scaling
- Parallel Sysplex coupling technology for data sharing and workload balancing

IBM Z is in a class of its own:
83% of respondents said their
firms achieved five and six
nines –99.999% and 99.9999%
– or greater uptime.
(ITIC

IBM System Recovery Boost Unleash your capacity to maximize your availability

Diminish the impact of any event, planned or unplanned, so you can achieve service level excellence with **zero increase in IBM software licensing costs**.

Recover workloads substantially faster than on prior Z machines by unleashing additional processing capacity during a fixed-period performance increase on an LPAR-by-LPAR basis.

With System Recovery Boost, you can achieve up to:

2.0x Faster

Return to pre-shutdown service levels

2.0x Faster

Processing of transactional backlog

2.5x Faster

Processing of batch backlog

2.5x Faster

GDPS automated startup, shutdown, site switches, etc.

Performance for the System Recovery Boost period

Processor Capacity Boost using zIIPs

Provides parallelism and a boost in processor capacity for processing any kind of work during the Boost.

Speed Boost

Sub-capacity machines gain a boost in processor speed by running the central processors at full-capacity speed during the Boost.

GDPS Reconfiguration

Increases the speed at which GDPS drives hardware actions, along with the speed of the underlying hardware services

System Recovery Boost Turbo - Unlock additional "dark cores" for extra zIIP processor capacity

Cryptographic acceleration with z15 hardware

Cryptographic acceleration with Crypto Express7S:

- Improved SSL/TLS handshake performance on z15 with Crypto Express7S compared to z14 with Crypto Express6S
- Updates to Common Cryptographic Architecture (CCA) for security modules that enhance remote ATM key loading, offer new protections for banking payments, and extended compliance support to stay up to date on industry standards

Cryptographic coprocessor on every core with CP Assist for Cryptographic Function (CPACF):

- Enhanced with elliptic curve cryptographic (ECC) algorithms that can help reduce CPU consumption for applications like Blockchain
- Enable an EP11 secure key to be converted to a protected key that can be used by CPACF

Designed for EAL5+

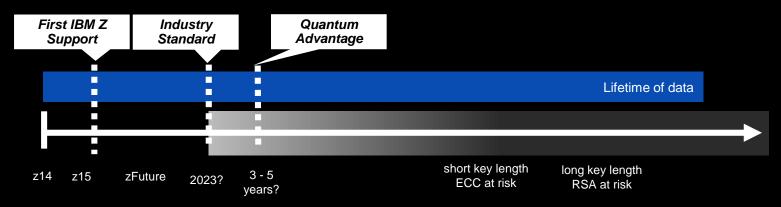


IBM Z investments in Quantum Safe Cryptography

Initial z15 Capability

- Initially delivered via Quantum safe digital signatures for z/OS SMF records
- · Agility in algorithms to update as standards evolve
- Acceleration coming in HSM for essential primitives for Quantum Safe cryptography

Timeline of Quantum Advantage vs. Data Lifecycle



Accelerate application development and solve business problems with the most advanced and fit-for-purpose compilers

Compilers enable modernization and increases performance of critical business applications

Java enables delivery of rich, scalable and robust applications with speed and agility

- Using COBOL 6.3 on average 58% reduction in CPU usage over applications compiled with COBOL v4.2 on z15
- Automatic Binary Optimizer v3.2 reduces CPU usage by up to 57% for compute intense apps built originally on COBOL 4.2
- Up to 22% reduction in CPU usage on z15 over the same set of key numerically intensive doubleprecision floating-point applications built with z/OS v2.3 XL C/C++ on z14

- Up to 20% throughput improvements in general Java workloads
- Takes advantage of new Integrated Accelerator for zEDC for up to 15x improvement over software and up to 2x faster elapsed times over zEDC Express
- Pause-less garbage collection: reducing pause times by up to 3x better throughput for constrained Service Level Agreements

End to end solution for data in flight protection

Future *IBM Fibre Channel Endpoint Security* to allow FICON® or FCP Links from the z15 to the next generation of the IBM DS8900F storage family to be encrypted and protected



Statement of Direction in Announce – To be delivered post GA

Challenges

- Corporate directive to encrypt all data in-flight.
- Ensure the integrity and confidentiality of data that is inflight is protected.

Client Value

- Knowledge that all data flowing within and across datacenters are traveling between trusted entities
- Be able to provide auditable data verifying that customer data is only being accessed by trusted IBM Z and storage devices
- Supports all IBM Z operating systems
- Reduces and eliminates insider threats of unauthorized access to data in flight



Protection of data that must be shared

New **z/OS** Data Privacy for Diagnostics is a z/OS capability exclusive to z15 with the ability to control access to data shared with business partners and eco-systems

Challenges

- Protection from accidentally sharing sensitive data when sending diagnostic information to vendors
- Concern for organizations who must comply with GDPR laws and/or other data privacy laws or company mandates

Client Value

- Sensitive data tagging APIs combined with machine learning (ML) to detect, tag and redact all tagged data from diagnostic dumps
- MVP is working with 1st set of exploiters (Db2, IMS and some DFSMS[™] components) to provide the infrastructure to tag sensitive data in z/OS
- Tagging does not impact dump times
- Supported on IBM z15 running z/OS 2.3 or 2.4

IBM z15 operating system support

z/OS

- z/OS 2.4 with PTFs
- z/OS 2.3 with PTFs
- z/OS 2.2 with PTFs

z/VSE

- z/VSE 6.2

z/TPF

z/TPF 1.1

z/VM

- z/VM 7.1 compatibility and exploitation support
- z/VM 6.4 compatibility support
- Data compression and sort optimization, new adapter support



Linux on Z

- Red Hat RHEL 8.0
- Red Hat RHEL 7.7
- Red Hat RHEL 6.10
- SUSE SLES 15.1
- SUSE SLES 12.4
- Ubuntu 18.04 LTS
- Ubuntu 16.04 LTS

KVM running on **Z**

KVM hypervisor for IBM Z is offered with the following Linux distributions:

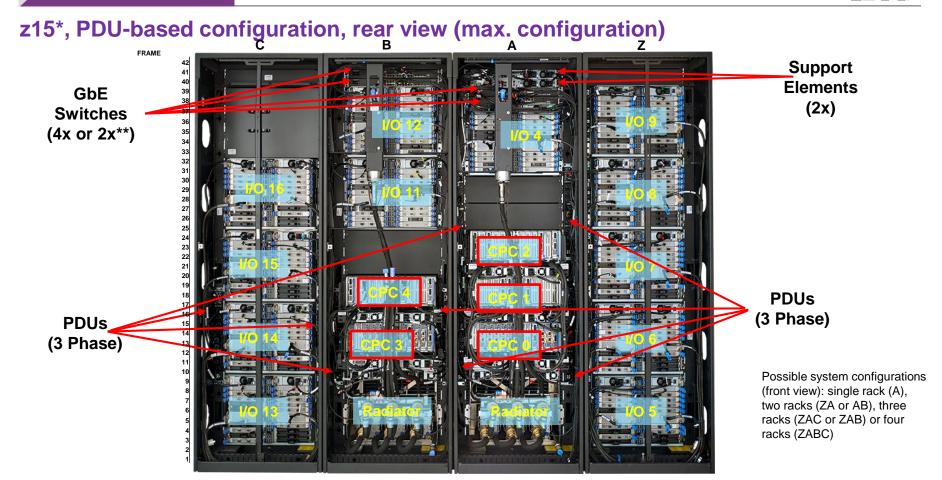
- Red Hat RHEL 8.0
- SUSE SLES 15.1
- SUSE SLES 12.4
- Ubuntu 18.04 LTS
- Ubuntu 16.04 LTS

NOTE: IBM and the Linux distribution partners plan to support the listed Linux distributions on z15. For IBM tested and Partner certified Linux environments see: ibm.com/il-infrastructure/z/os/linux-tested-platforms

IBM cannot legally discuss z15 exploitation prior to GA from distributors.

IBM is working with the open source community and the Linux distribution partners to get new z15 functionality supported with Linux for Z and KVM.

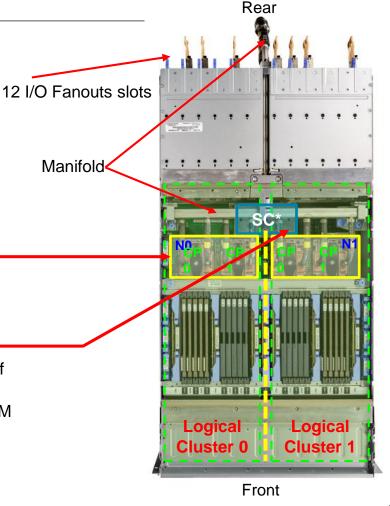
CEC Details



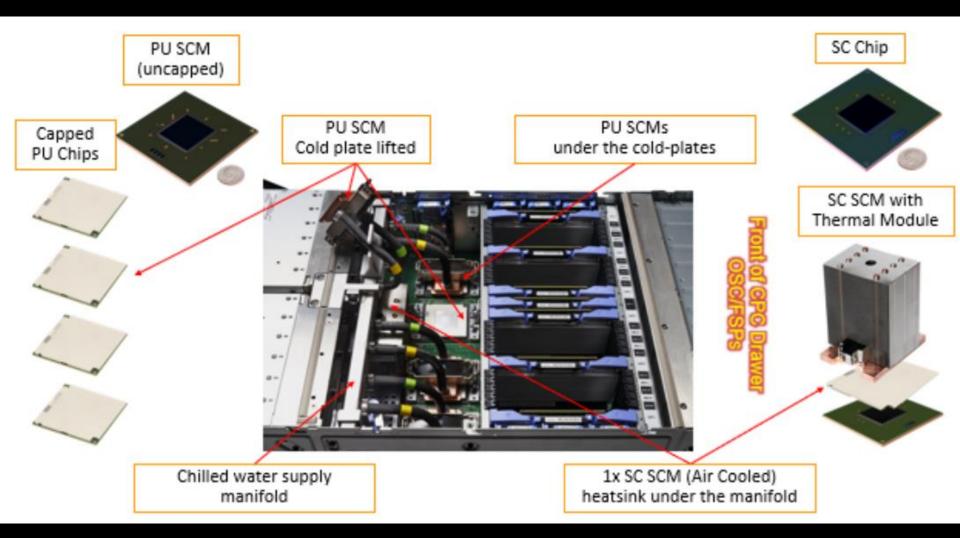
IBM Z

z15 Processor Drawer (Top View)

- Each PU SCM:
 - 14nm
 - Four PU SCMs
 - One Memory Controller per PU Chip
 - Five DDR4 DIMM slots per Memory Controller
 - 20 DIMMs total per drawer
- Each drawer:
 - Two logical PU clusters (0 and 1)
 - Four PU Chips per CPC Drawer:
 - 41 active PUs per drawer Max34, Max71, Max108 and Max145
 - 43 active PUs per drawer Max190
 - One SC Chip (960 MB L4 cache)
 - DIMM slots: 20 DIMMs to support up to 8 TB of addressable memory (10 TB RAIM)
 - Water cooling for PU SCMs, air cooled SC SCM
 - Two Flexible Support Processors/ OSC Cards
 - 12 fanout slots for PCle+ I/O drawer or PCle coupling fanouts (ICA SR).



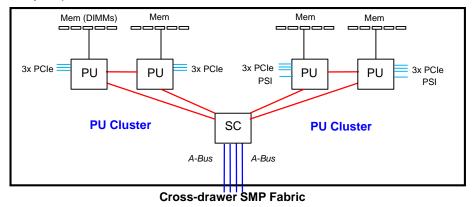
Manifold



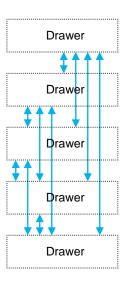


z15 On-Drawer and System Topology

Fully Populated Drawer



- PU Chip: 12 SMT2 cores per PU chip, core frequency @ 5.2 GHz, SC with 960MB L4 per Drawer
- Cores count: 24 cores per cluster, 48 cores in a drawer, 240 way 5-drawer system (with all core chips active*, actual design has max. 215 active cores)
- Fabric: Multi-layer (X and A) peer-peer fabric protocol
- Memory: DDR4 DIMMs, 5 DIMM's (RAIM) per CP, Support up to 40TB (512GB DIMMs) in a 5-drawer system
- PCIe: 3x PCIe x16 Gen4* per CP, 12 PCIe ports are pinned out from drawer



5 Drawer System Fully Interconnected

IBM Z – Processor Roadmap

45 nm

z196 9/2010

Top Tier Single Thread
Performance, System Capacity
Accelerator Integration
Out of Order Execution
Water Cooling
PCIe I/O Fabric
RAIM

Enhanced Energy Management

32 nm

zEC12 8/2012



Enhanced Throughput Improved out-of-order Transactional Memory Dynamic Optimization

Leadership Single Thread,

2 GB page support
Step Function in System
Capacity

22 nm

z13 1/2015



Leadership System Capacity and Performance

Modularity & Scalability

Dynamic SMT
Supports two instruction

threads SIMD

PCIe attached accelerators
Business Analytics Optimized

14 nm

z14 7/2017



Pervasive encryption

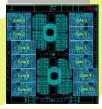
Low latency I/O for acceleration of transaction processing for DB2 on z/OS

Pause-less garbage collection for enterprise scale JAVA applications

New SIMD instructions

Optimized pipeline and enhanced SMT Virtual Flash Memory 14 nm

z15 9/2019



Focus on power efficiency and new on-chip architectures

Improved and enlarged caches

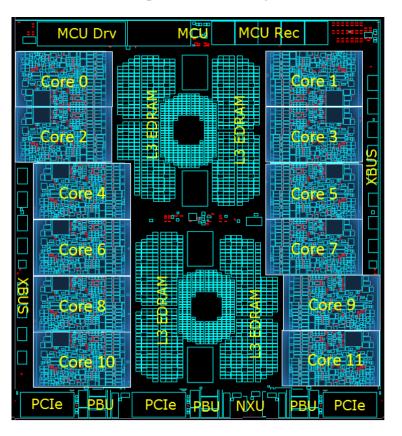
Optimized Out-of-Order architecture

On-chip compression support (DEFALTE)

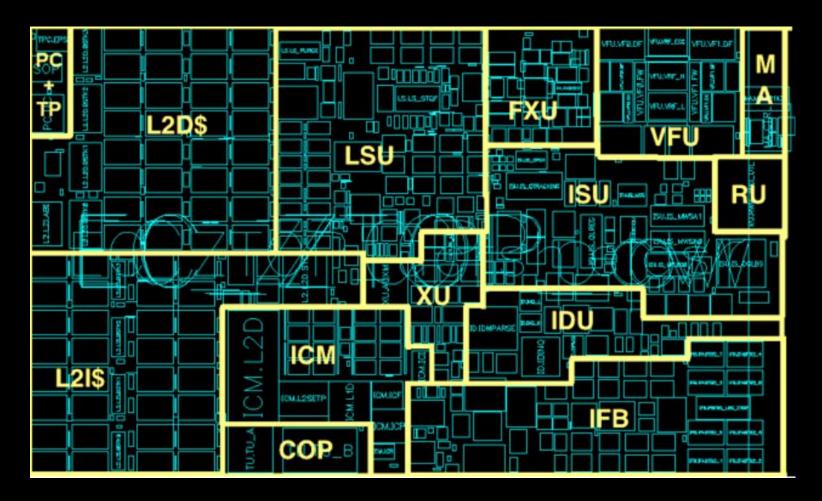
Elliptic curve cryptography acceleration



z15 Processor Design Summary



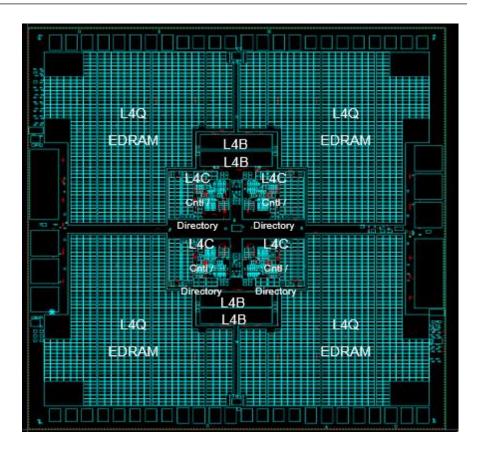
- More than 9.1 Billion transistors
- 15.6 miles of wire
- 696 mm² chip area
- 14nm SOI technology,
- 17 layers of metal
- 12 cores per CP-chip design
- 5.2 GHz core frequency
- Optimized to enable performance and capacity growth
 - 20% reduction in core area
 - 20% reduction in core power
 - Cache Growth
- Pipeline enhancements for performance
 - Improved out-of-order, improved branch prediction, Enhanced Store-Forwarding, 2x bandwidth vector load, double single-precision FP capacity, ...
- New instructions
 - Elliptic Curve Crypto, Vector, String & BCD Ops
- New accelerators
 - Modular Arithmetic, Compression, Sort



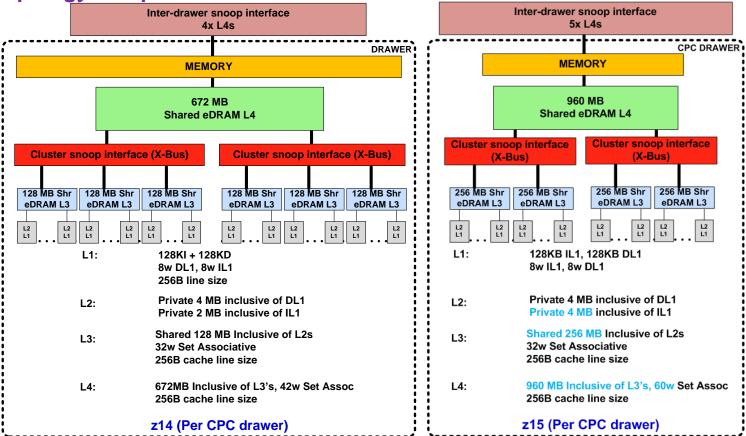


z15 SC Chip

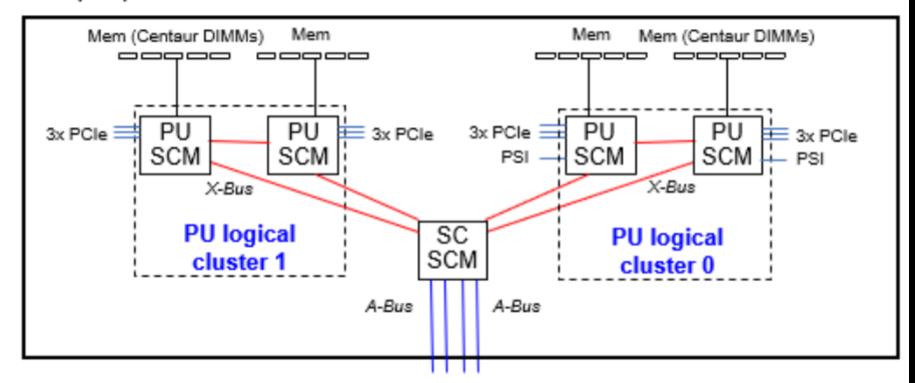
- SC Chip area: 696 mm²
- 9.7 Billion transistors
- 14nm SOI technology, 17 layers of metal
- 960 MB shared eDRAM L4 Cache
- System Interconnect
- System Coherency Manager
- X and A Bus Support for:
 - 4 CPs using 4 x-buses
 - 5 drawers using 4 A-buses (point-to-point).



Cache topology comparison: z15 vs. z14



Fully Populated Drawer



SMP cables to other drawers

