

What is Millicode and why do I care?

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TechU

2018 IBM Systems Technical University

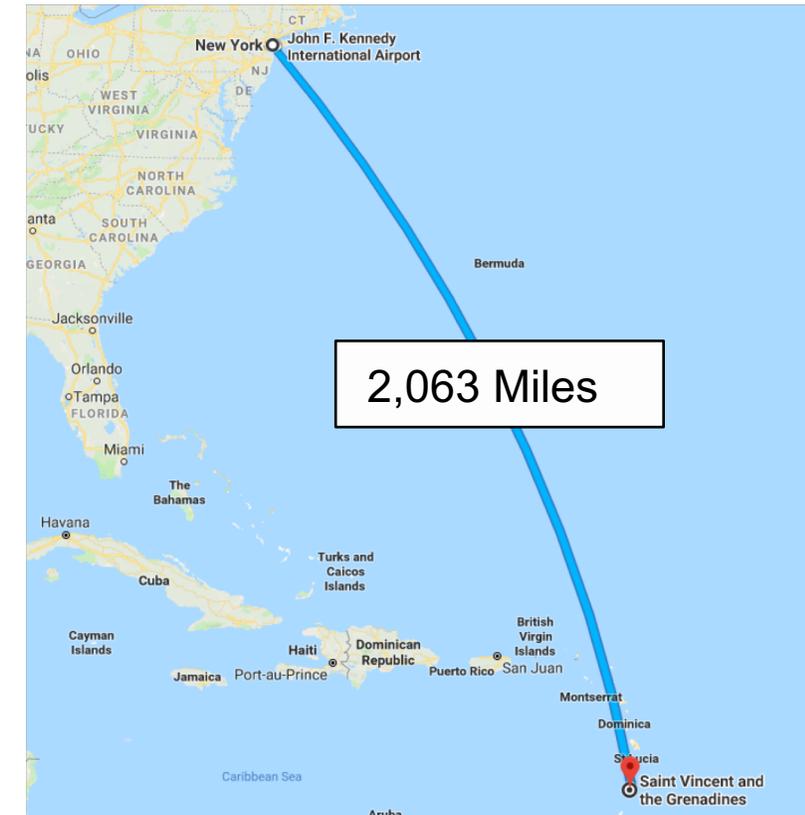
October 11th
Hollywood, FL

IBM[®]



About me

- B.S. degree in computer engineering from the New Jersey Institute of Technology
- M.Eng. degree in computer and systems engineering from Rensselaer Polytechnic Institute
- Senior Technical Staff Member (STSM)
- Worked on many generations of IBM Z processors
 - Hipersockets – 1st major assignment
- X'13' years at IBM
- 31 patents



Session Objectives

- You will be able to describe what Millicode is
- You will know more about where, when, and why it's used
- You will have a much better understanding than what's on the Internet
- You will understand why it's an important part of IBM Z

Topics

What is Millicode?

Fun Facts

Where is Millicode used?

The Millicode team

IBM Z instruction set

Millicode Structure

Updating Millicode

Millicode Control Registers

Millicode in Recovery and Serviceability

Millicode Startup and Exit

Millicode Interrupts

System Operations

Millicode Transformation

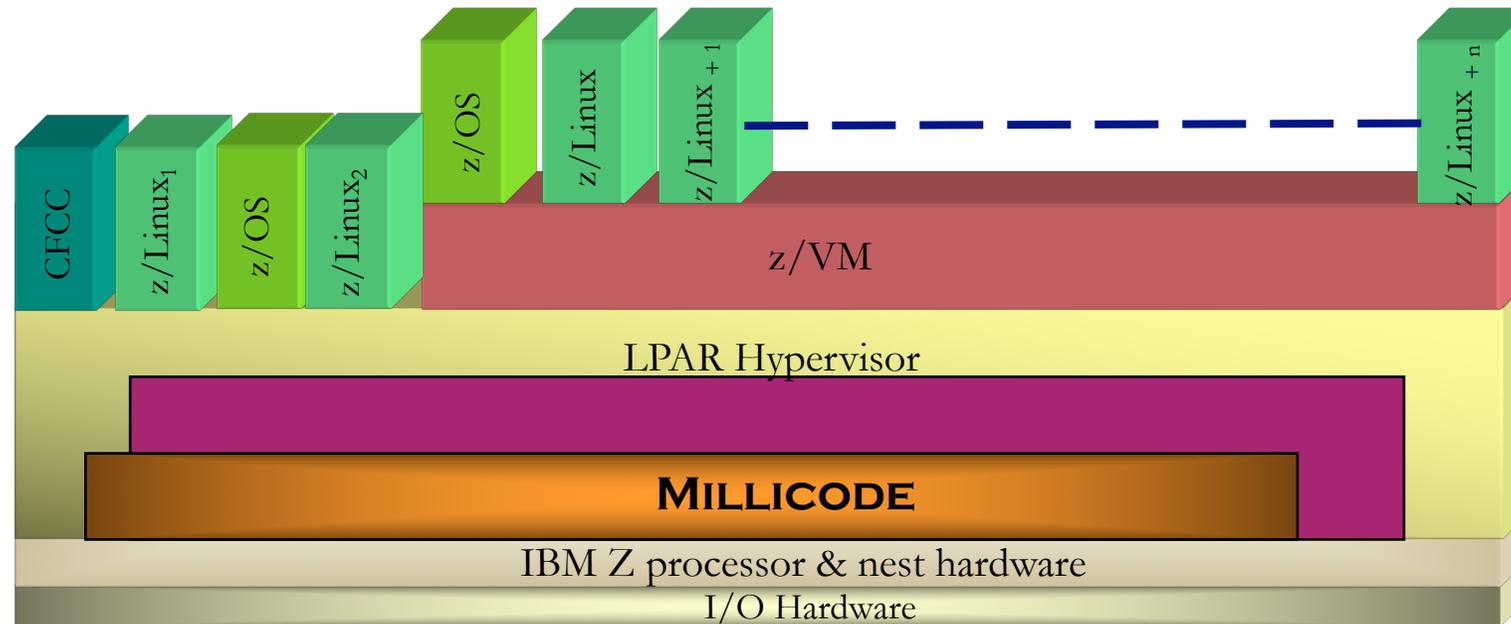
Summary

1. What is Millicode?

“In computer architecture, millicode is a higher level of microcode used to implement the instruction set of a computer. “

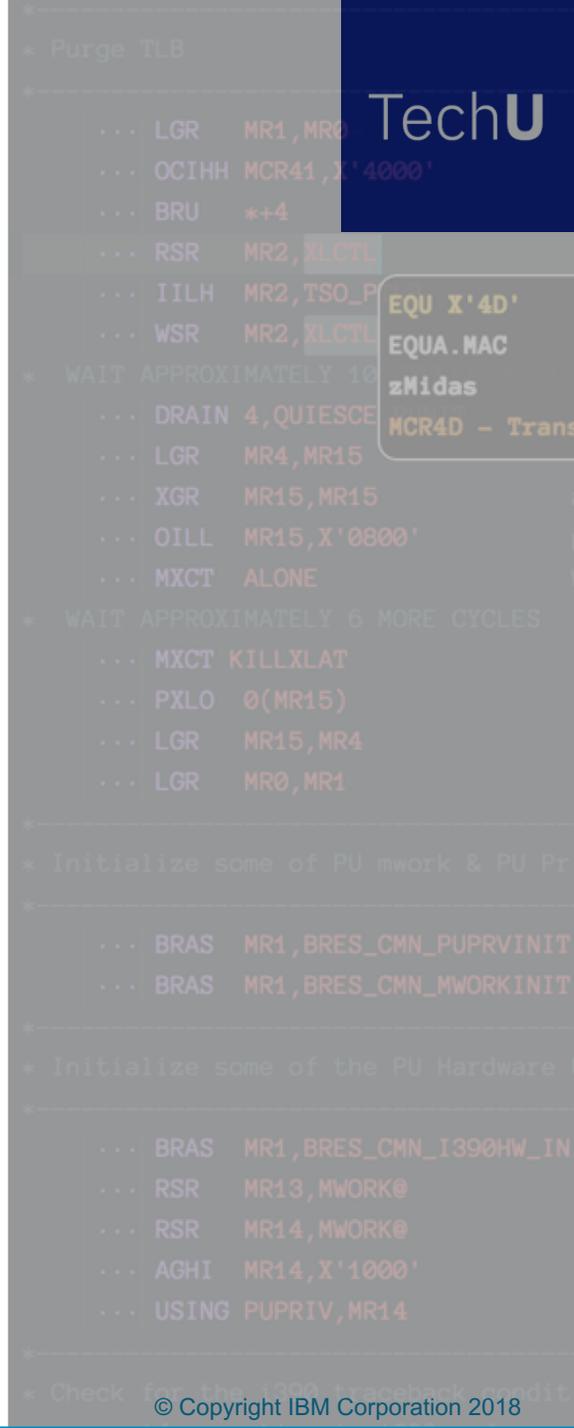
<https://en.wikipedia.org/wiki/Millicode>

IBM Z Hardware, Firmware and Software Layers

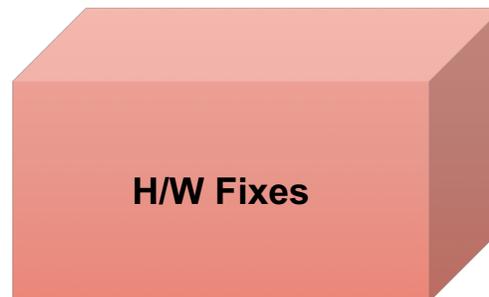
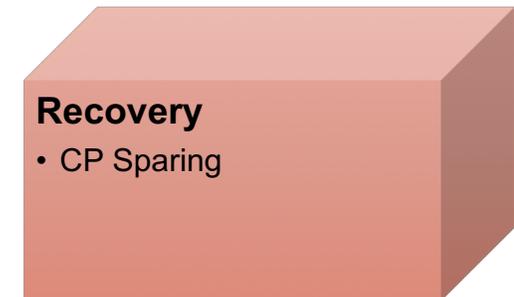
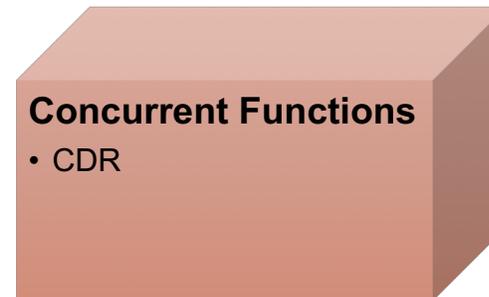
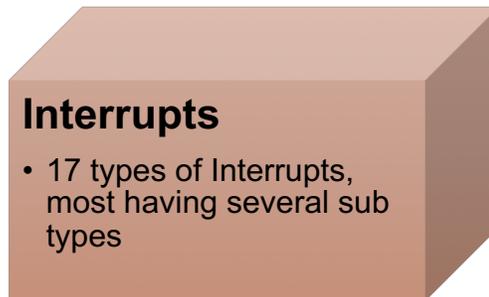
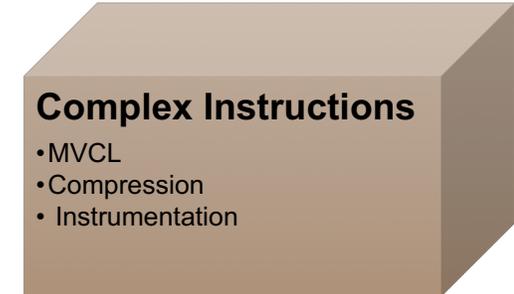
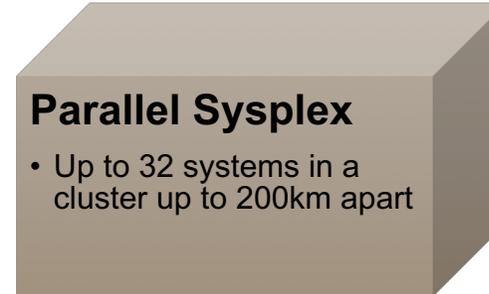
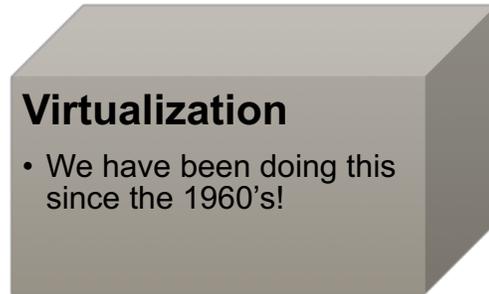


2. Millicode Fun Facts

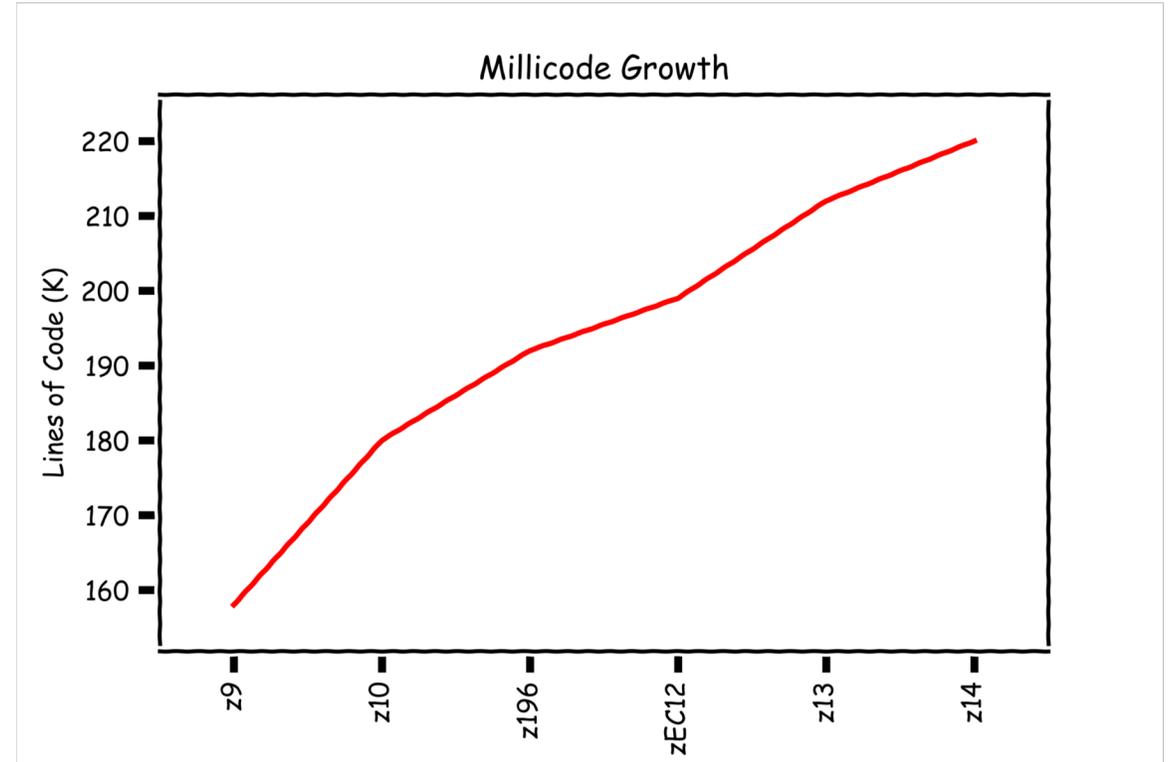
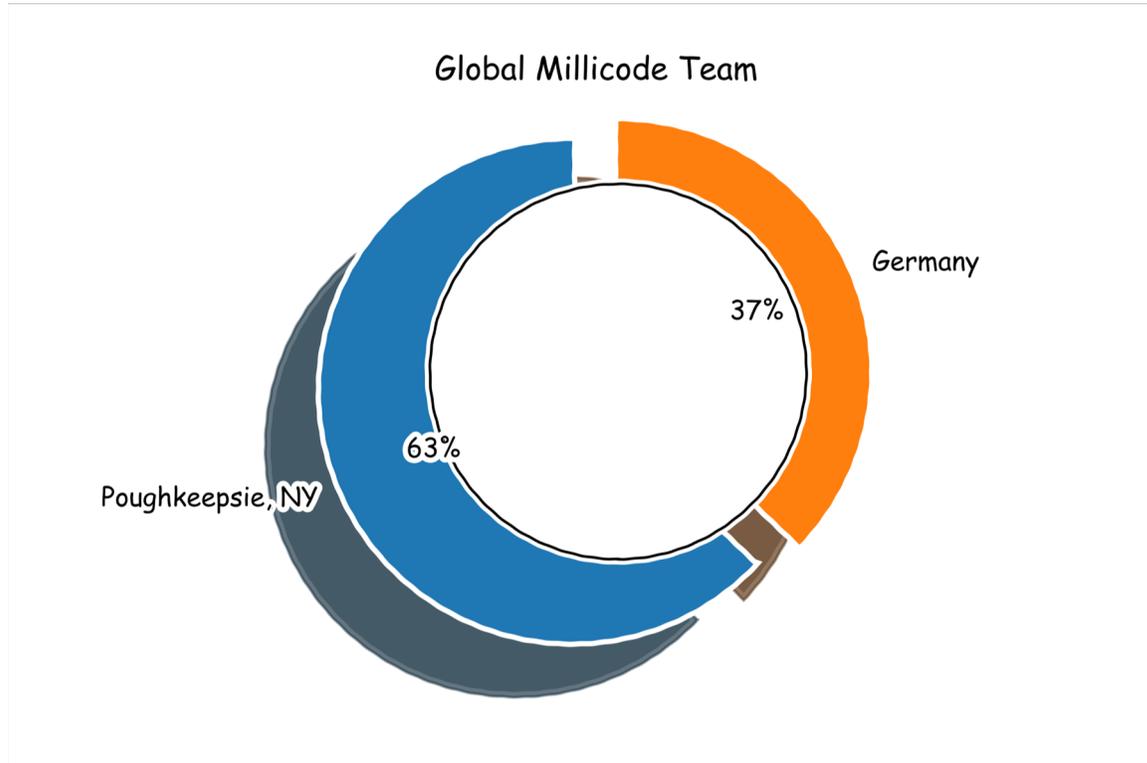
- Millicode is a form of firmware that runs on IBM Z
- It's also the micro-architecture on IBM Z processor
- It's a superset of the Principles of Operation
- It's written in HLASM – (IBM) High Level Assembler
- HLASM was introduced in 1992 replacing IBM's H assembler
- It's a form of vertical microcode that replaced horizontal microcode
- It was 1st introduced in 1997 on S/390 G4
- Millicode runs with the highest level of authority



3. Where's Millicode used?

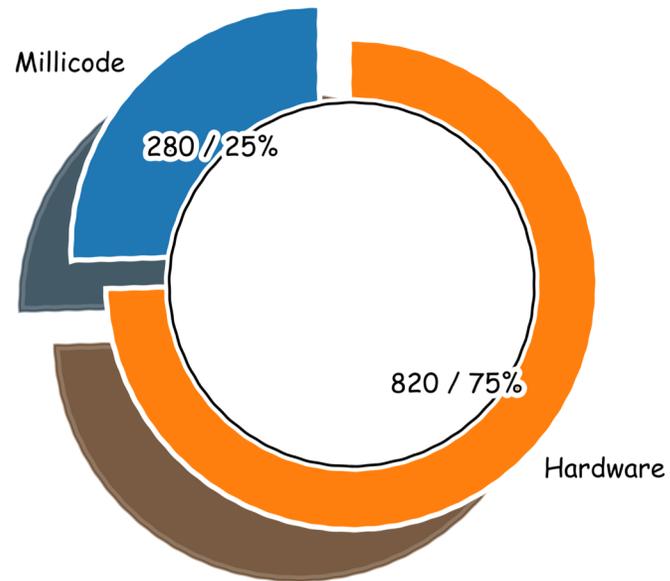


4. The Millicode Team and growth

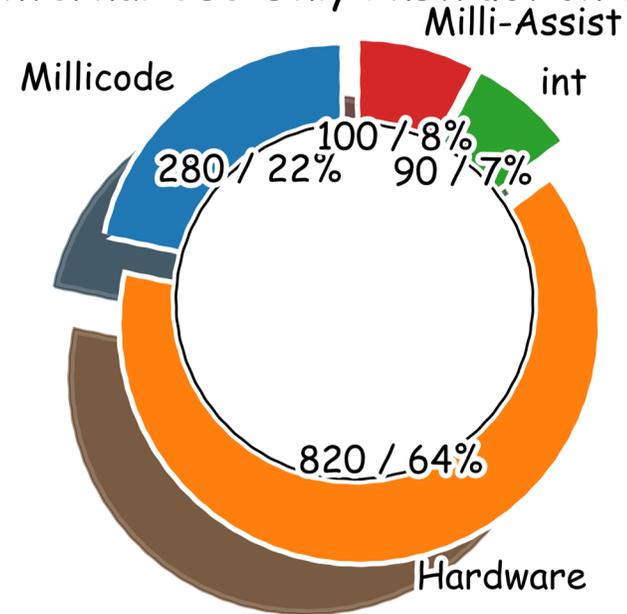


5. IBM Z instruction set

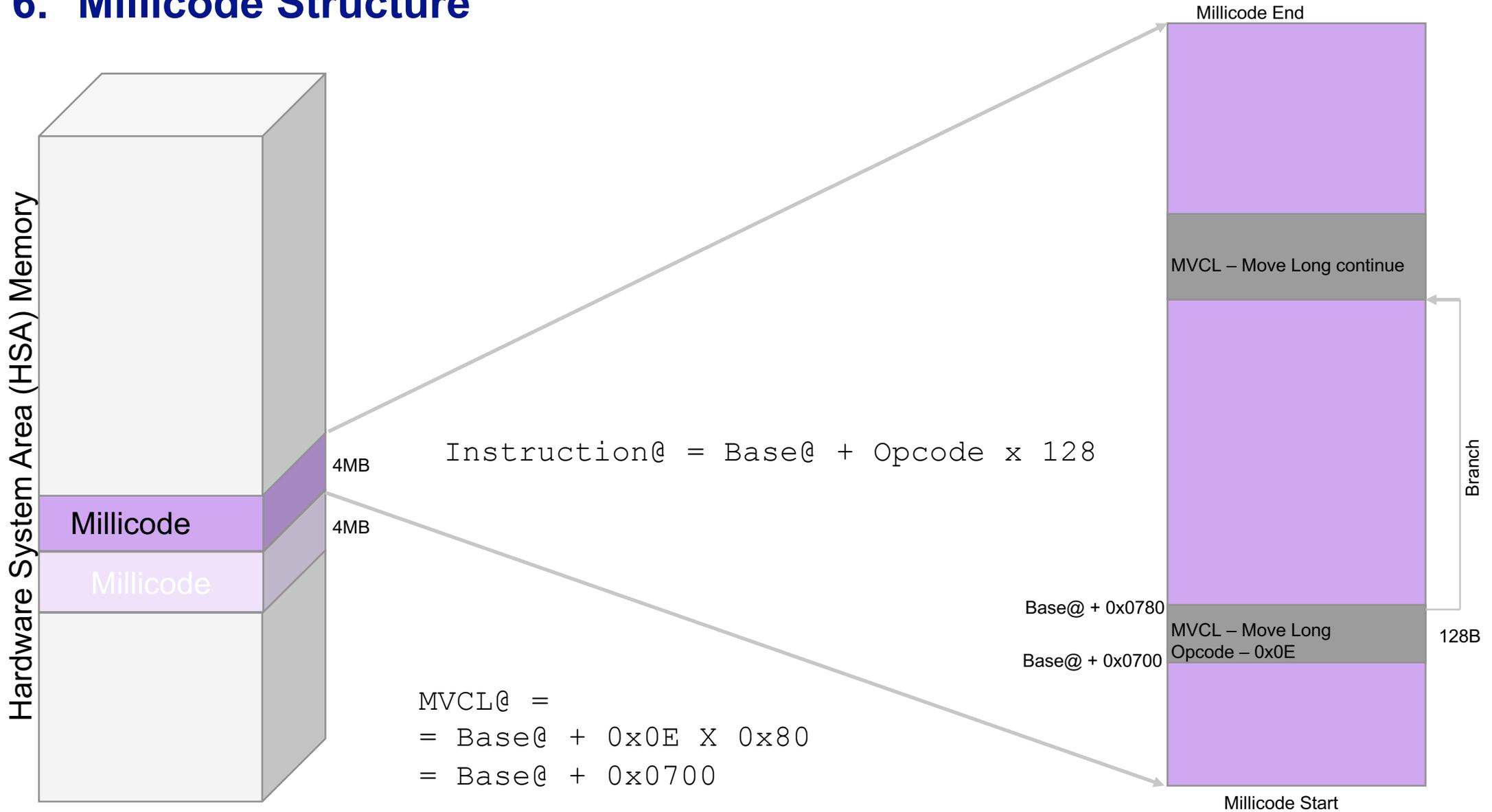
IBM Z Instruction Set (~1,100)



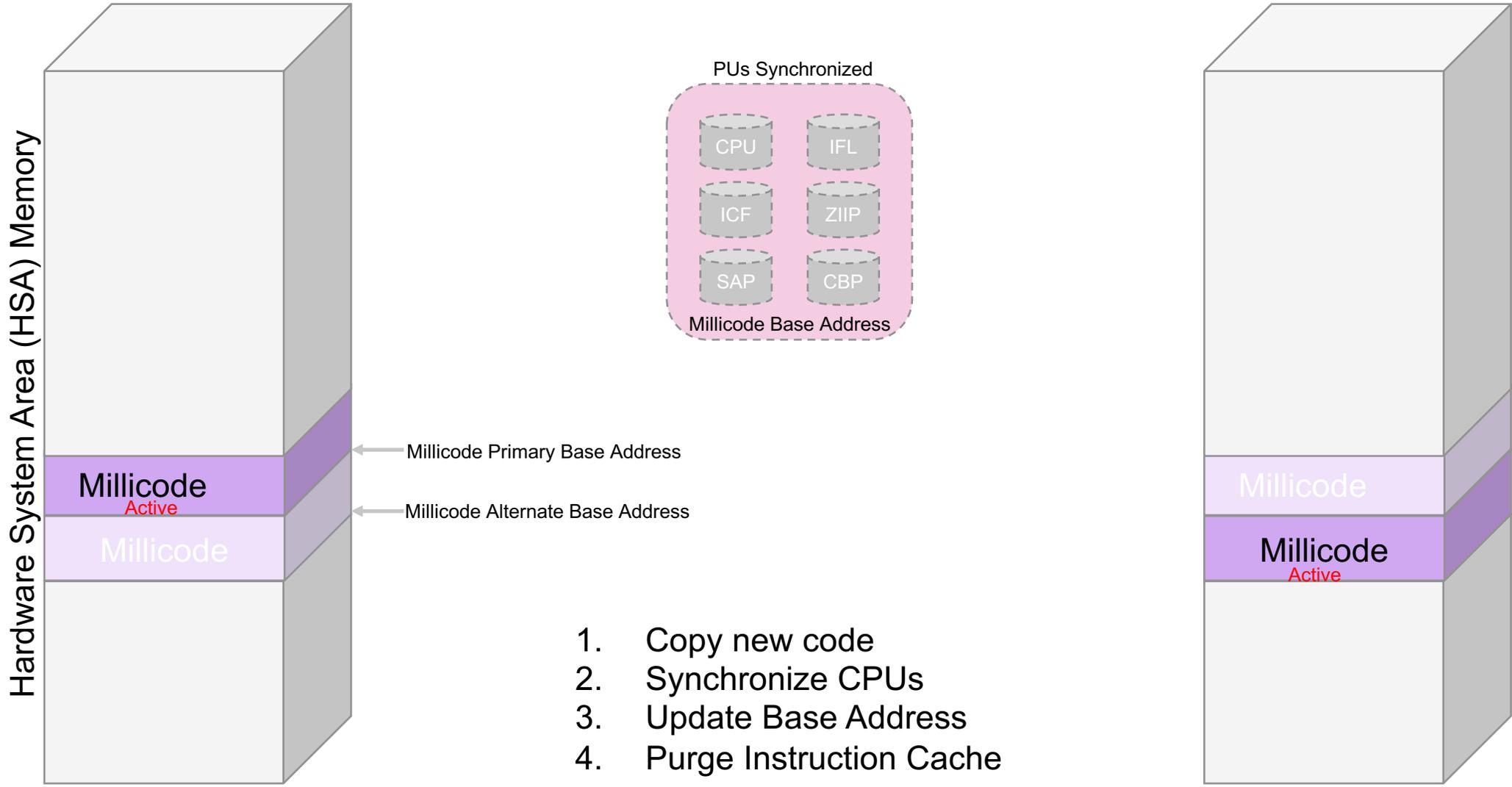
IBM Z Internal Use Only Instruction Set (~1,300)



6. Millicode Structure



7. Millicode Concurrent Update



1. Copy new code
2. Synchronize CPUs
3. Update Base Address
4. Purge Instruction Cache

8. Millicode Control Registers

Address	Mnemonic	Description
000-03F	MCR	Core Millicode Control Registers
t40-t4F	MCRs	Thread Millicode Control Registers
t50-t5F	G2CRs	Thread Guest-2 Program Control Registers
t60-t6F	G1CRs	Thread Guest-1 Program Control Registers
t70-t7F	HCRs	Thread Host Program Control Registers
t80-t8F	MCRs	Thread Millicode Control Registers
t90-t9F	MCRs	Thread Millicode Control Registers
tA0-tAF	MCR	Thread Millicode Control Registers
0B0-0BF	TF/MCR	Core TOD and Millicode Control Registers
tC0-tCF	TF	Thread Timing Facility Registers
tD0-tDF	MCR	Thread Additional Registers
tE0-tEF	COP	Thread Co-Processor Communications
tF0-tFF	IA	Thread Instruction Address, PSW, Exception Information

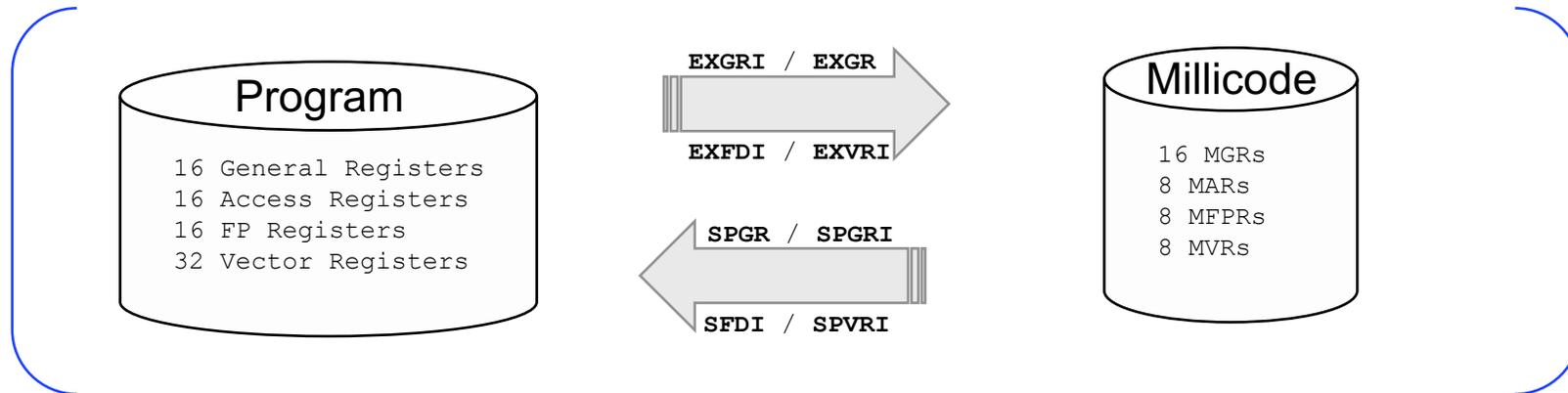
Milli-Assist Instructions

- RSR** - Read Special Register
- WSR** - Write Special Register

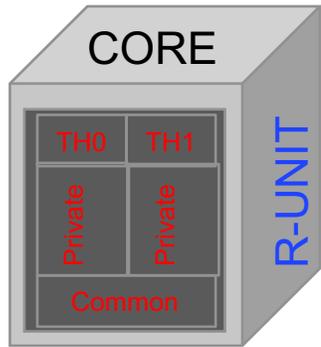
- NSR** - AND Special Register
- XSR** - XOR Special Register

- WASR** - Write Absolute Special Register
- RASR** - Read Absolute Special Register

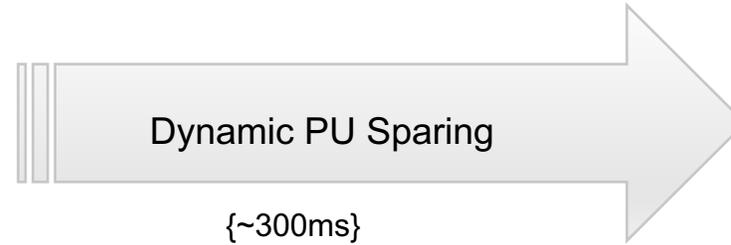
- TRBIT** - Test Register Bit
- TARBIT** - Test Register Bit



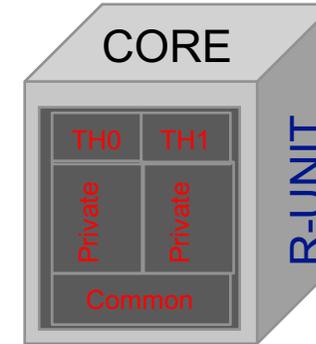
9. Millicode in Recovery



PU
{old core}

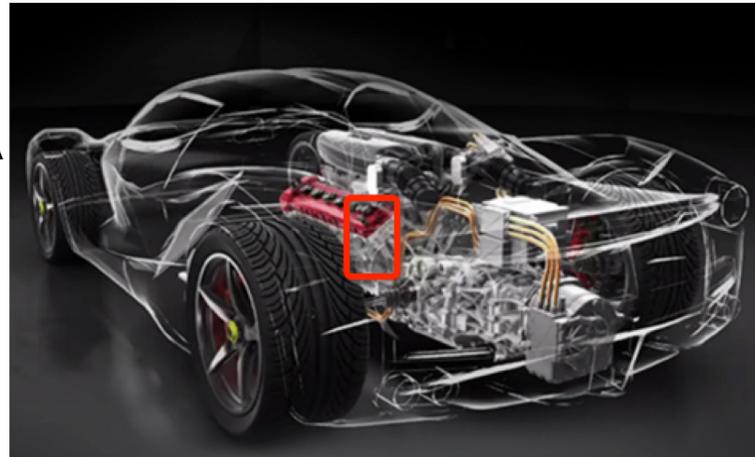


>512 64bit registers



SPARE
{new core}

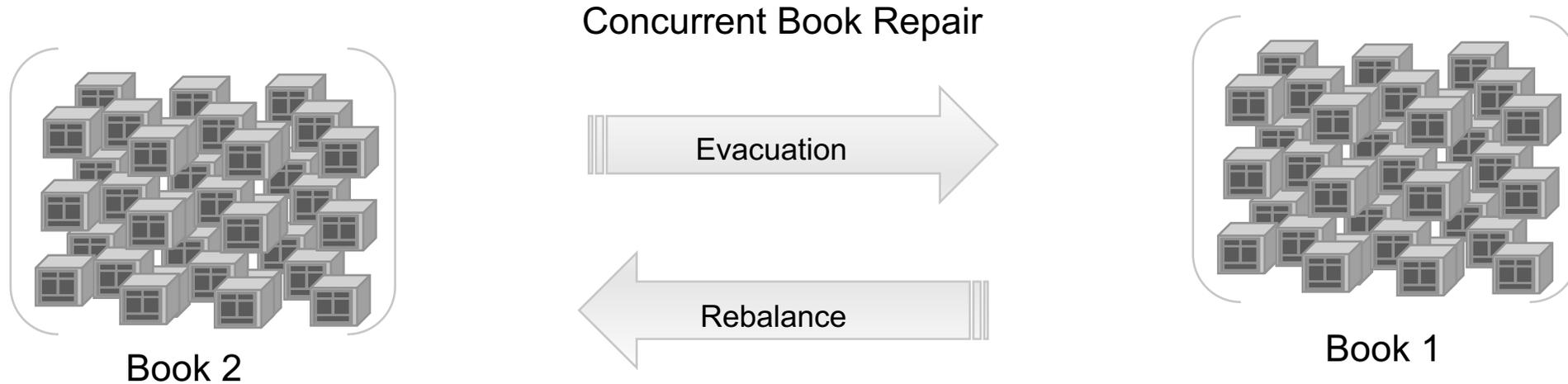
— Entire R-Unit copied to HSA



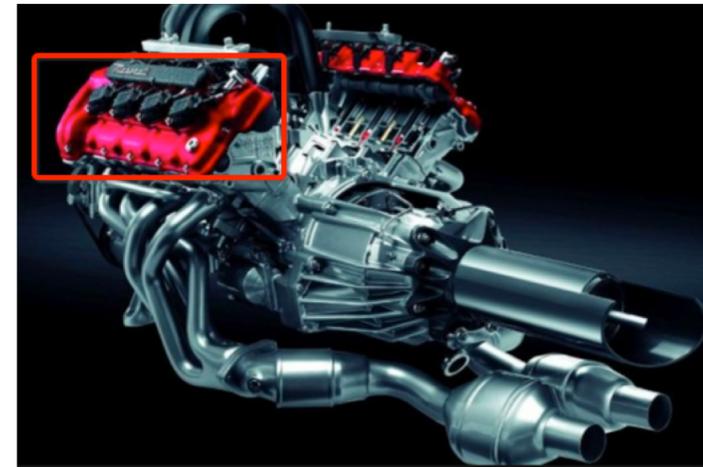
— Dead core R-Unit loaded into new core

- LRUS LRUSHSA@

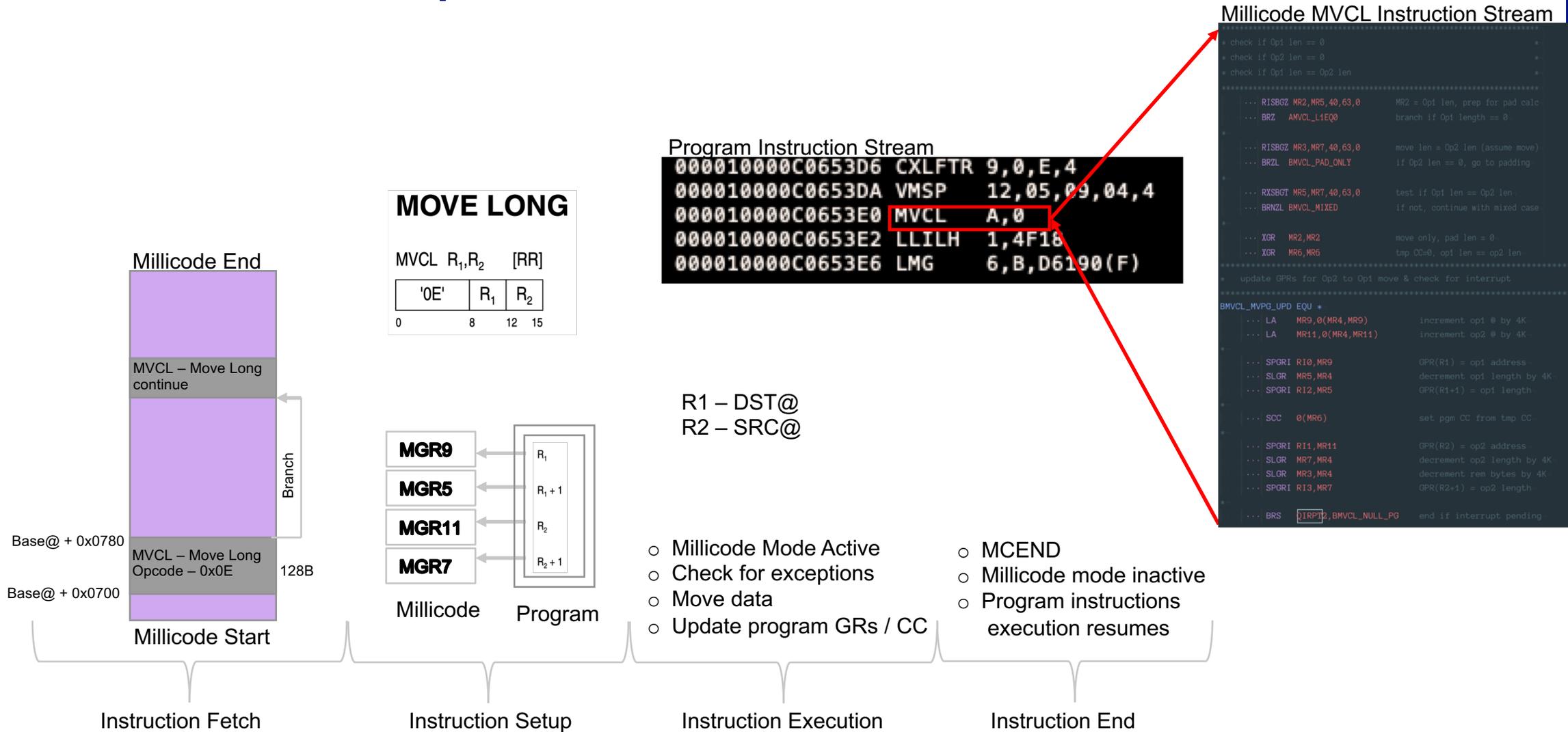
9. Millicode in Serviceability



- Production engines on Book 2 are moved to Spare engines on Book 1
- Book 2 can be removed, serviced, and returned to running system
- Production engines are then rebalanced from Book 1 back to Book 2



10. Millicode Start-up & Exit



11. Millicode Interrupts

```

Program Instruction Stream
000010000C0653D6 CXLFT 9,0,E,4
000010000C0653DA VMSP 12,05,09,04,4
000010000C0653E0 MVCL A,0
000010000C0653E2 LLILH 1,4F10
000010000C0653E6 LMG 6,B,D6,50(F)
    
```

Millicode MVCL Instruction Stream

```

* check if Op1 len == 0
* check if Op2 len == 0
* check if Op1 len == Op2 len
.....
... RISBGZ MR2,MR5,40,63,0 MR2 = Op1 len, prep for pad calc
... BRZ AMVCL_L1EQ0 branch if Op1 length == 0
.....
... RISBGZ MR3,MR7,40,63,0 move len = Op2 len (assume move)
... BRZL BMVCL_PAD_ONLY if Op2 len == 0, go to padding
.....
... RXSBGT MR5,MR7,40,63,0 test if Op1 len == Op2 len
... BRNZL BMVCL_MIXED if not, continue with mixed case
.....
... XGR MR2,MR2 move only, pad len = 0
... XGR MR6,MR6 tmp CC=0, op1 len == op2 len
    
```

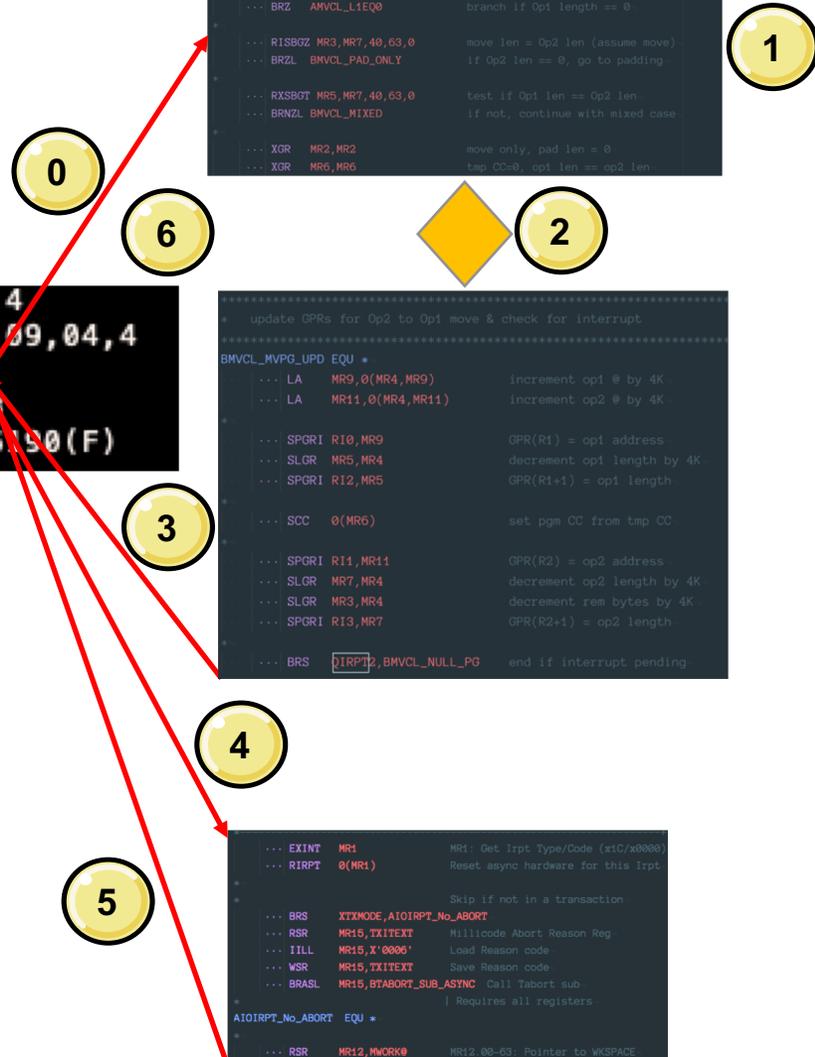
```

* update GPRs for Op2 to Op1 move & check for interrupt
.....
BMVCL_MVPG_UPD EQU *
... LA MR9,0(MR4,MR9) increment op1 # by 4K
... LA MR11,0(MR4,MR11) increment op2 # by 4K
.....
... SPGR1 R10,MR9 GPR(R1) = op1 address
... SLGR MR5,MR4 decrement op1 length by 4K
... SPGR1 R12,MR5 GPR(R1+1) = op1 length
.....
... SCC 0(MR6) set pgs CC from tmp CC
.....
... SPGR1 R11,MR11 GPR(R2) = op2 address
... SLGR MR7,MR4 decrement op2 length by 4K
... SLGR MR3,MR4 decrement rem bytes by 4K
... SPGR1 R13,MR7 GPR(R2+1) = op2 length
.....
... BRS [DIRPT2, BMVCL_NULL_PG] end if interrupt pending
    
```

```

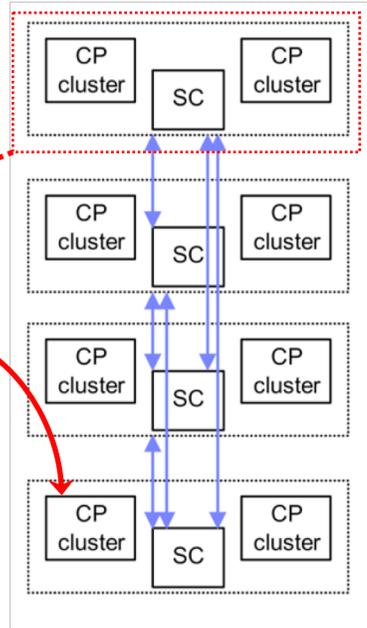
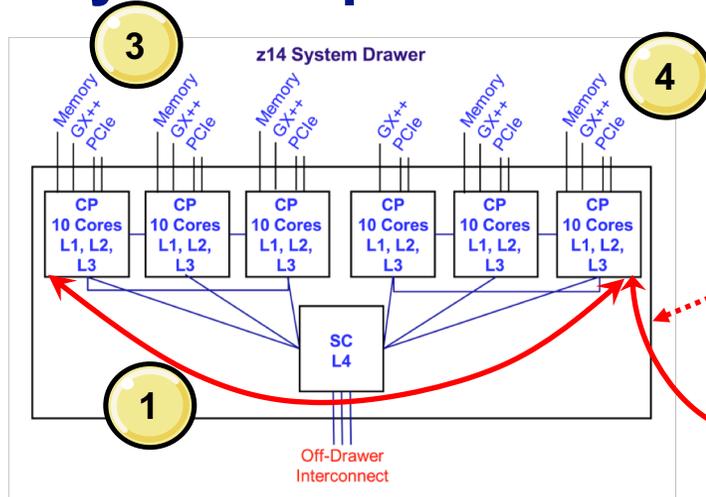
... EXINT MR1 MR1: Get Irpt Type/Code (x1C/x0000)
... RIRPT 0(MR1) Reset async hardware for this Irpt
.....
... BRS XTMODE_AIOIRPT_No_ABORT Skip if not in a transaction
... RSR MR15,XTITEXT Millicode Abort Reason Reg
... IILL MR15,'0000' Load Reason code
... WSR MR15,XTITEXT Save Reason code
... BRASL MR15,BTABORT_SUB_ASYNC Call Tabort sub
... BRASL MR15,BTABORT_SUB_ASYNC Call Tabort sub
| Requires all registers
AIOIRPT_No_ABORT EQU *
... RSR MR12,MWORK0 MR12: 00-03: Pointer to WKSPACE
    
```

Millicode I/O Interrupt Instruction Stream



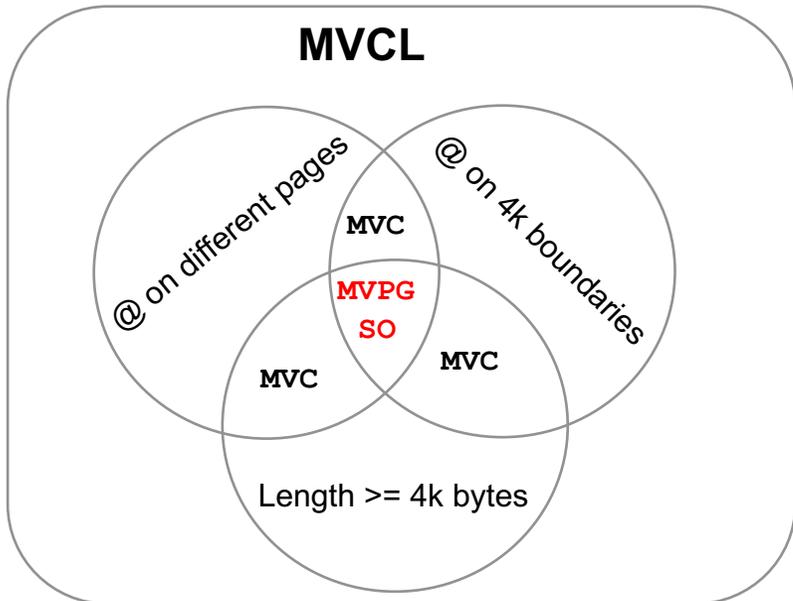
- 0 IFetch MVCL Millicode
- 1 Millicode executing MVCL
- 2 Millicode detects a pending I/O interrupt
- 3 Millicode ends MVCL {Nullifying}
- 4 H/W dispatches Millicode I/O Interrupt handler
IO_OLD = PSW
PSW = IO_NEW
- 5 Millicode ends – z/OS I/O Interrupt handler starts
- 6 z/OS eventually loads IO_OLD and returns to MVCL

12. System Operations - SYSOPs



~ 50 primary functions + sub functions

- 1 Intra-drawer communications
- 2 Inter-drawer communications
- 3 Memory Initialization
- 4 I/O Initialization



Cache level	z13		z14
L1	96 KB I-Cache 128 KB D-Cache (private-to-core)	MVC	128 KB I-Cache 128 KB D-Cache (private-to-core)
L2	2 MB I-Cache 2 MB D-Cache (private-to-core)		2 MB I-Cache 4 MB D-Cache (private-to-core)
L3	64 MB (shared by 8 cores)	MVPG SYSOP	128 MB (shared by 10 cores)
L4	480 MB + 224 MB Non-Inclusive Coherent (NIC) Directory (shared by 3 CP chips)		672 MB L4 (shared by 6 CP chips)

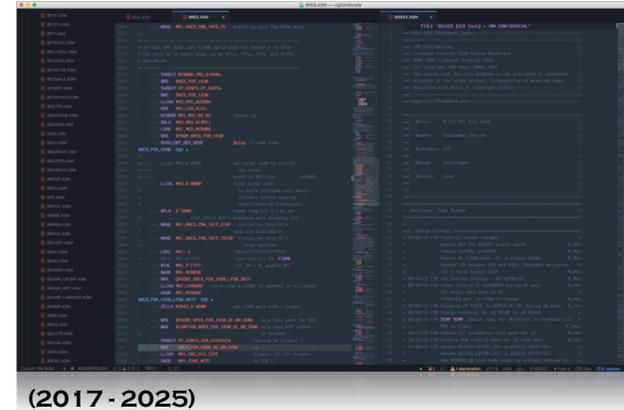
13. Other uses of Millicode

- Rapid instruction development
- Bug fixes in early H/W prototypes
- Early H/W function
 - Long Displacement Facility introduced on z990, retro fitted on z800 and z900 systems
- Sophisticated traps to aid debugging of complex H/W and S/W problems
- Some instructions are executed in H/W until it becomes difficult

14. Millicode Transformation

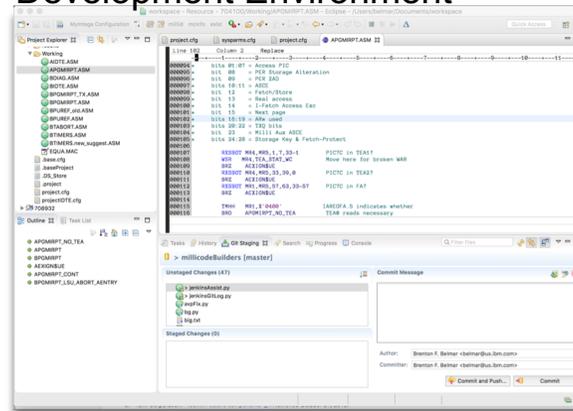
State-of-the-art software development environment

Atom – Millicode IDE



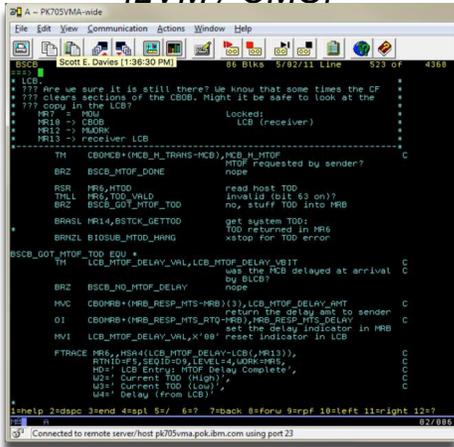
(2017 - 2025)

Eclipse - Integrated Development Environment

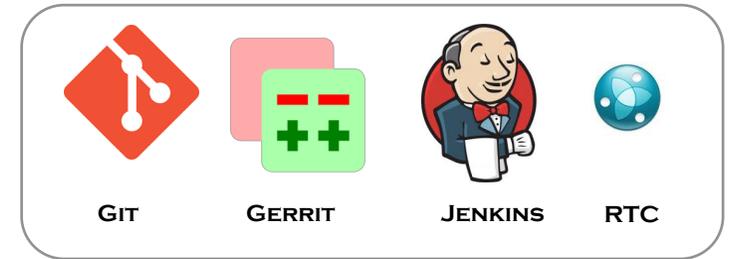


(2003 - 2018)

Mainframe Development
IzVM / CMSI

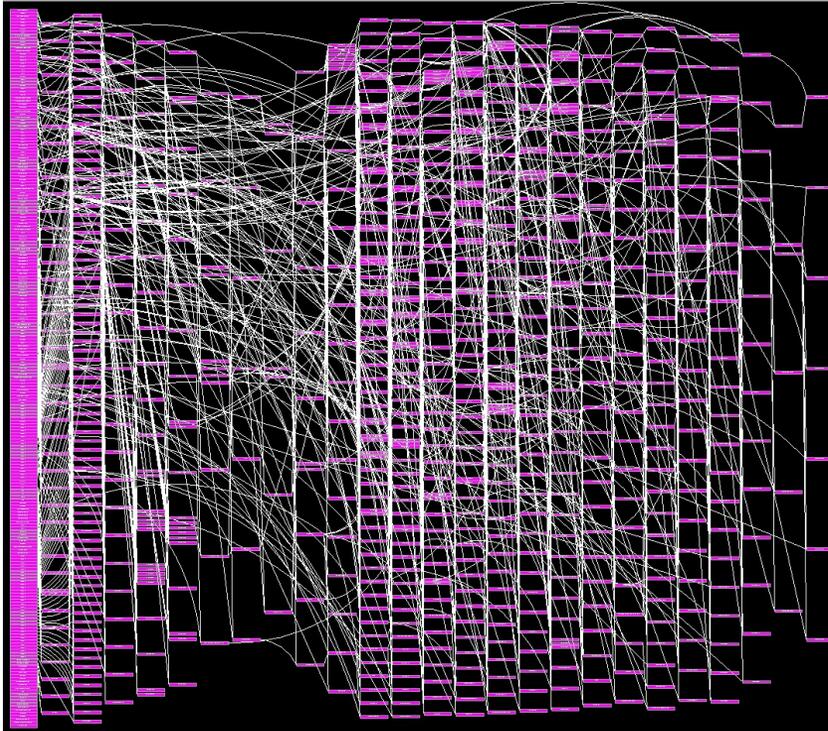


(1997 - 2004)



15. Millicode in Summary

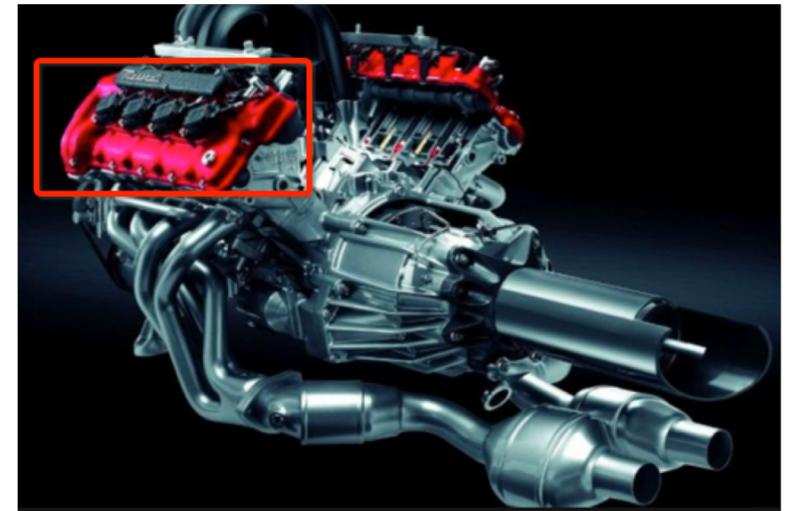
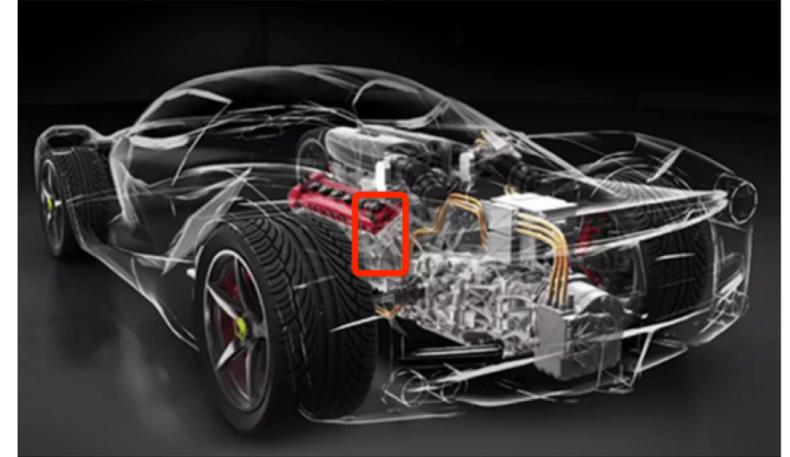
- Complex instructions



- Millicode and do anything hardware can do... but a little slower

15. Millicode in Summary

- Performs complex Recovery / Serviceability functions



15. Millicode in Summary

- Fixes hardware problems



15. Millicode in Summary

- Concurrently adds features or fixes



Thank you!

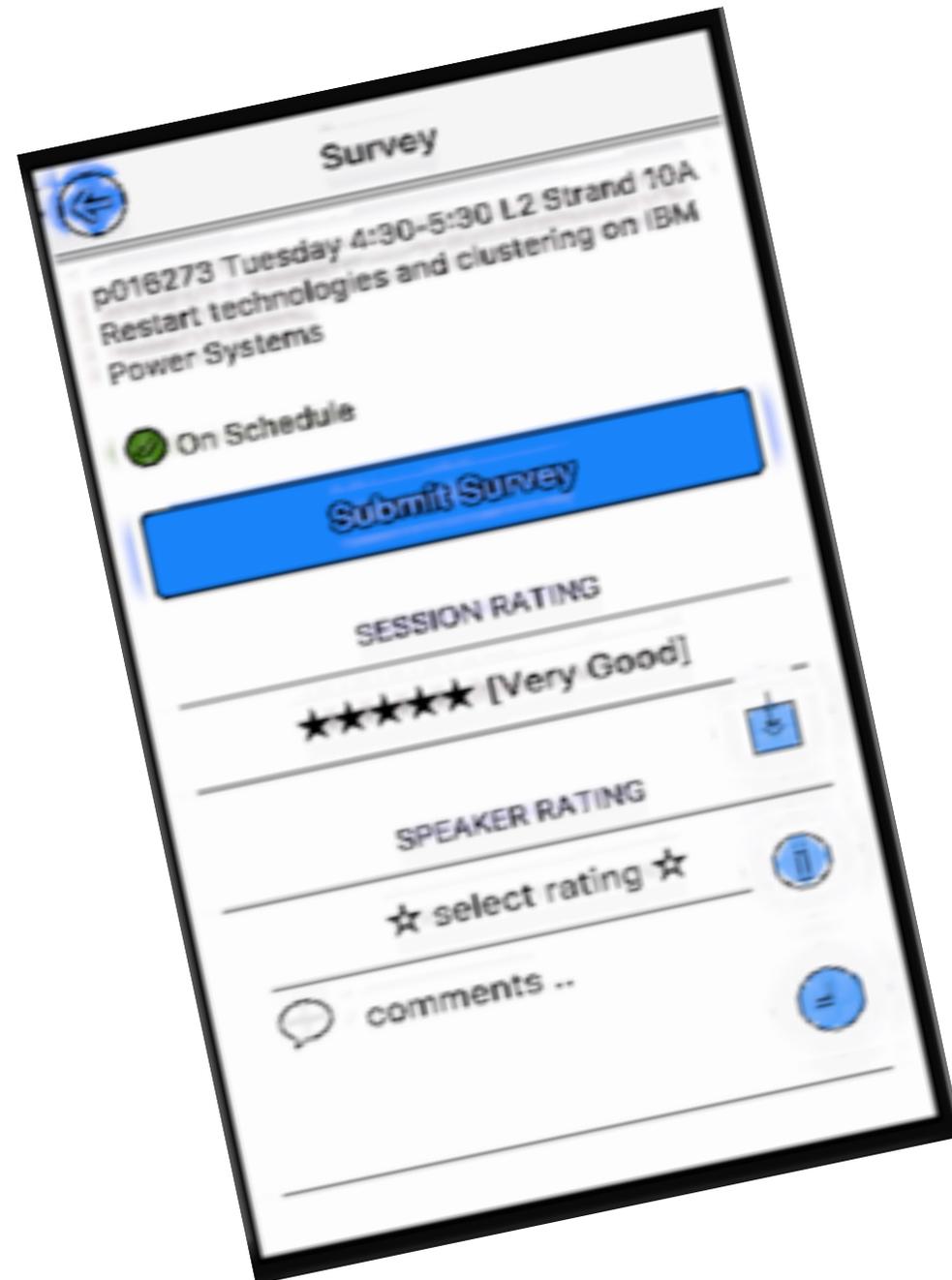
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Evaluation!**



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