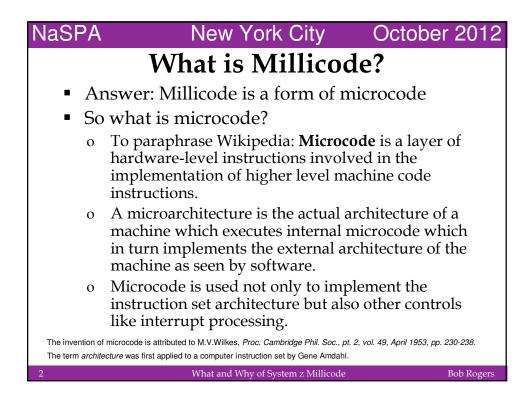
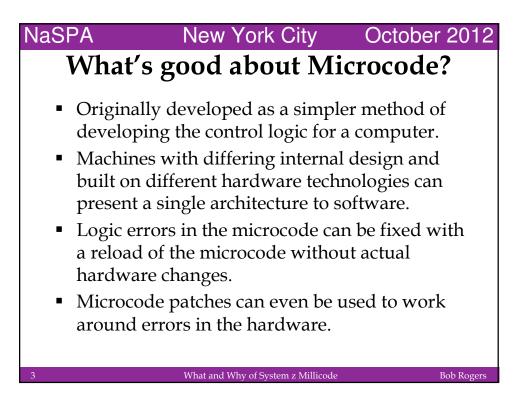
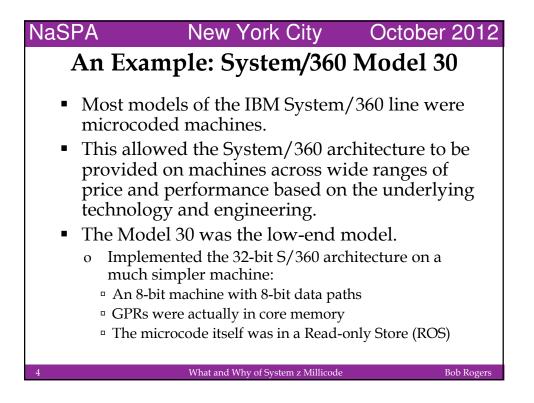
## What and Why of System z Millicode

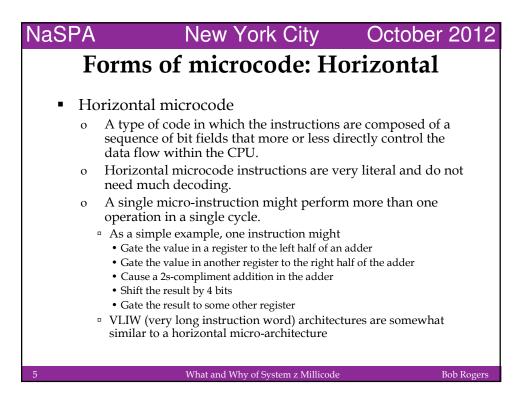
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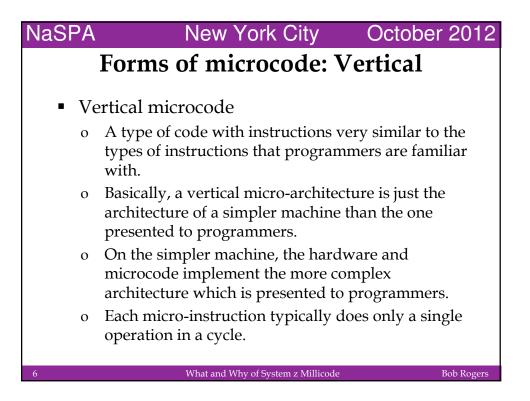
> Bob Rogers IBM Corporation tetterrogers@gmail.com

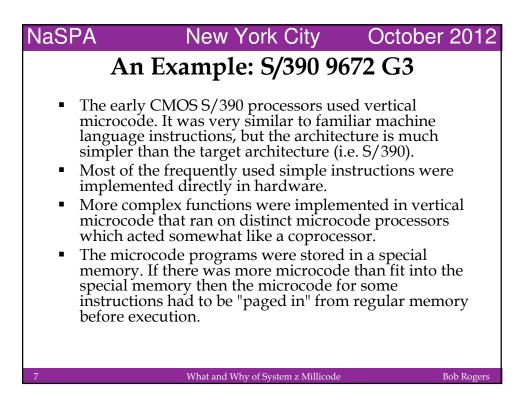


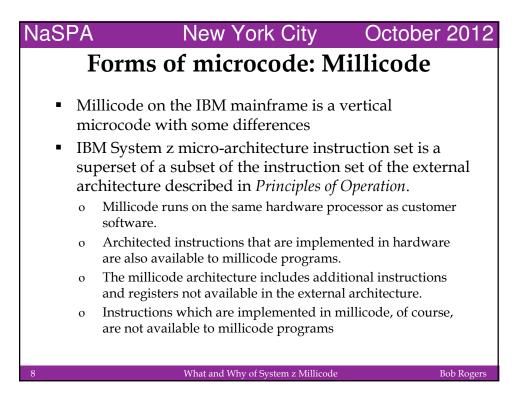


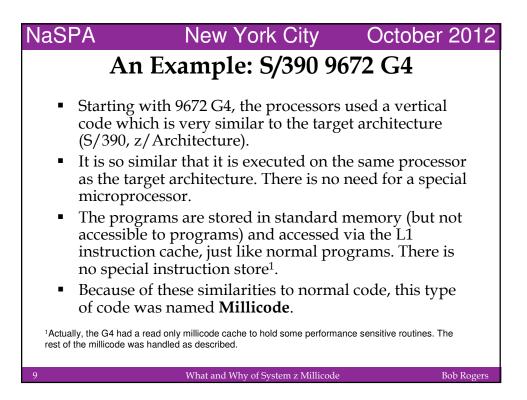




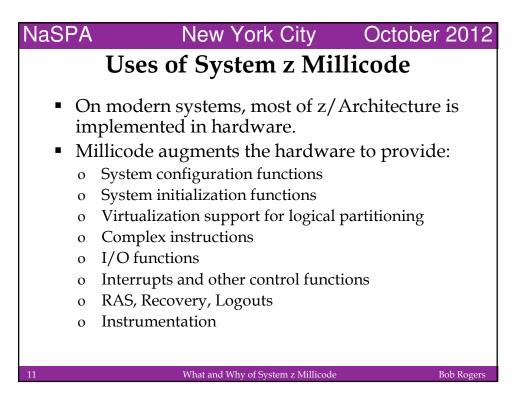


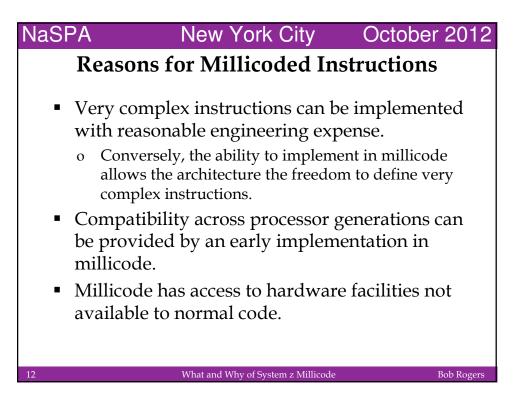


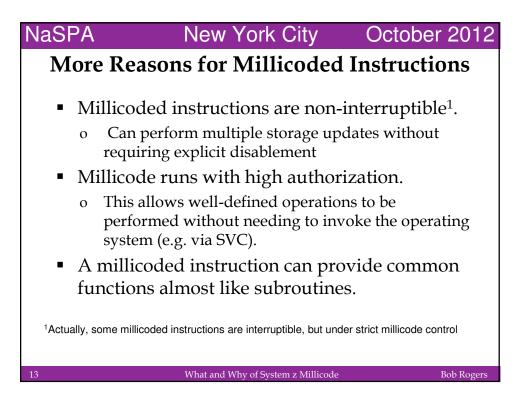




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Millicode Implementation				
zA aug	ce millicode executes on the same rchitecture instructions, that proce gmented with additional state info pable of executing additional instr- there is a "millicode mode" - millimode millicode status: milli-GPRs, milli-ARs, instruction address register plus other r there are instructions to move data betw register and the millicode registers. other special instructions only available cannot use instruction implemented in r when millicode is entered, specific milli loaded before the millicode is given com	essor must be ormation and be uction types. milli-CRs, millicode nillicode registers veen the architected in millimode millicode code registers are		
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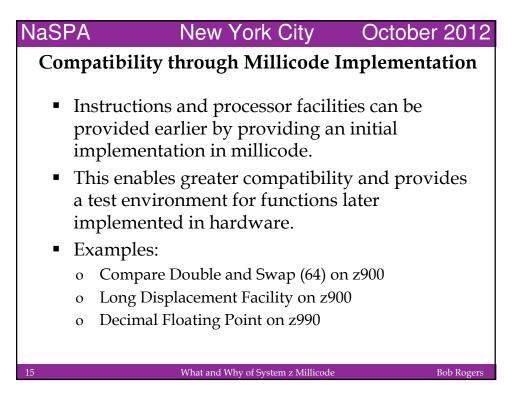


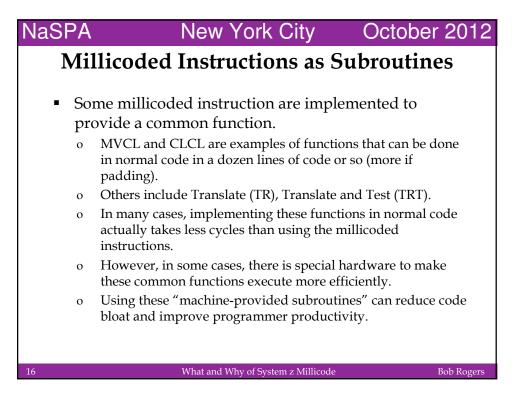


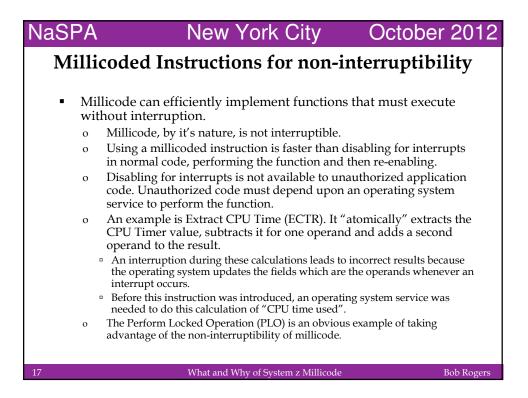


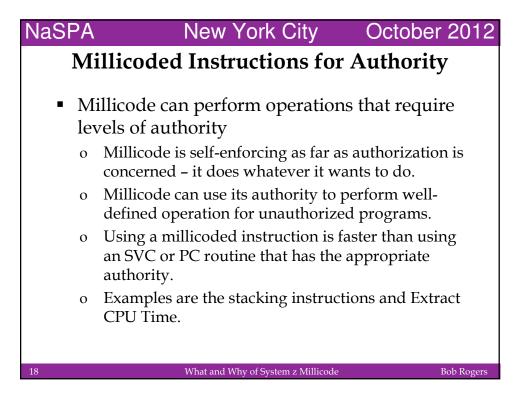
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Very Complex Millicoded Instructions				
<ul> <li>Using millicode allows engineers to provide complex functions without complex logic design.</li> <li>Many of the most complex z/Architecture instruction include over 100 cycles of activity</li> </ul>				
	Examples: Program Call (PC), Branch and Stac Transfer (PT) Load Address Space Parameters (LA Perform Locked Operation (PLO) Cipher Message (KM) I/O Instructions (SSCH, TSCH, HSC	k (BAKR), Program ASP)		

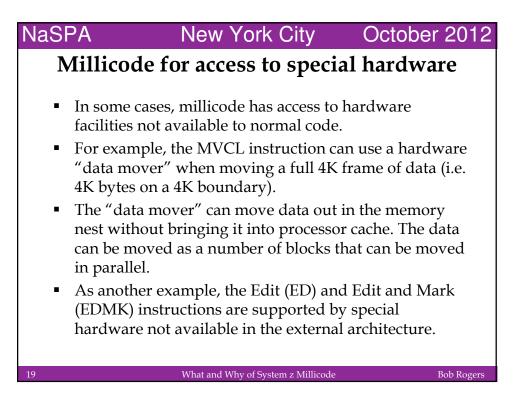
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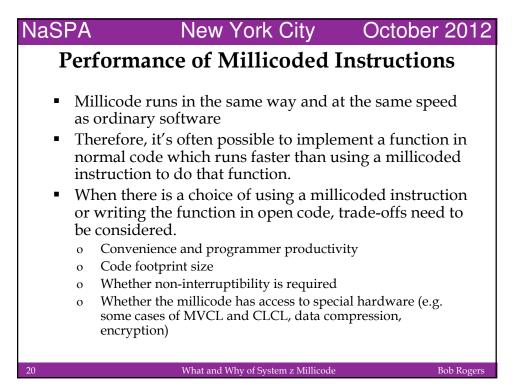


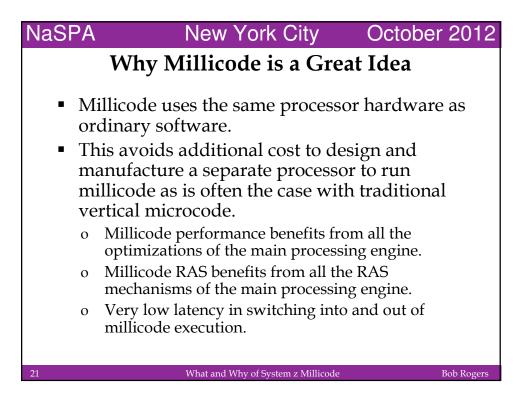






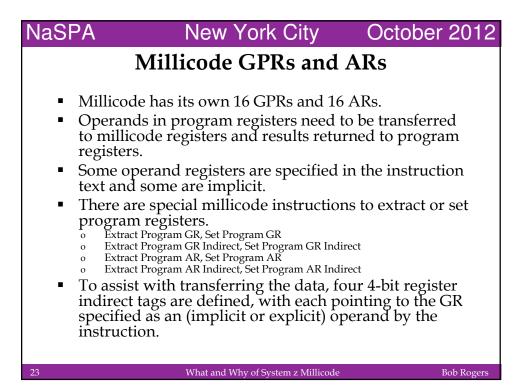








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Millicode Startup				
<ul> <li>Even for instructions implemented in millicode, the hardware performs some setup before branching to the millicode routine.</li> </ul>				
<ul> <li>For example, here is the setup for Compare Until Substring Equal (CUSE):</li> <li>Machine Check if Millicode Mode</li> </ul>				
0 0 0	Specification Exception if $R_1$ or $R_2$ are O IAREGA7. <sub>0:31</sub> set to Instruction Text	dd GRs		
0 0	$RI_0$ set to $R_1$ GR number $RI_1$ set to $R_2$ GR number			
0 0	$RI_2$ set to $R_{1+1}$ GR number $RI_3$ set to $R_{2+1}$ GR number			
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