



# **1394 Open HCI Self ID Receive Physical Requests**

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# Agenda

- ◆ **Self ID DMA Controller**
  - **Self ID Packets on 1394**
  - **Self ID DMA operations**
- ◆ **Physical Requests**
  - **What is a Physical Request?**
  - **Physical Requests handling**



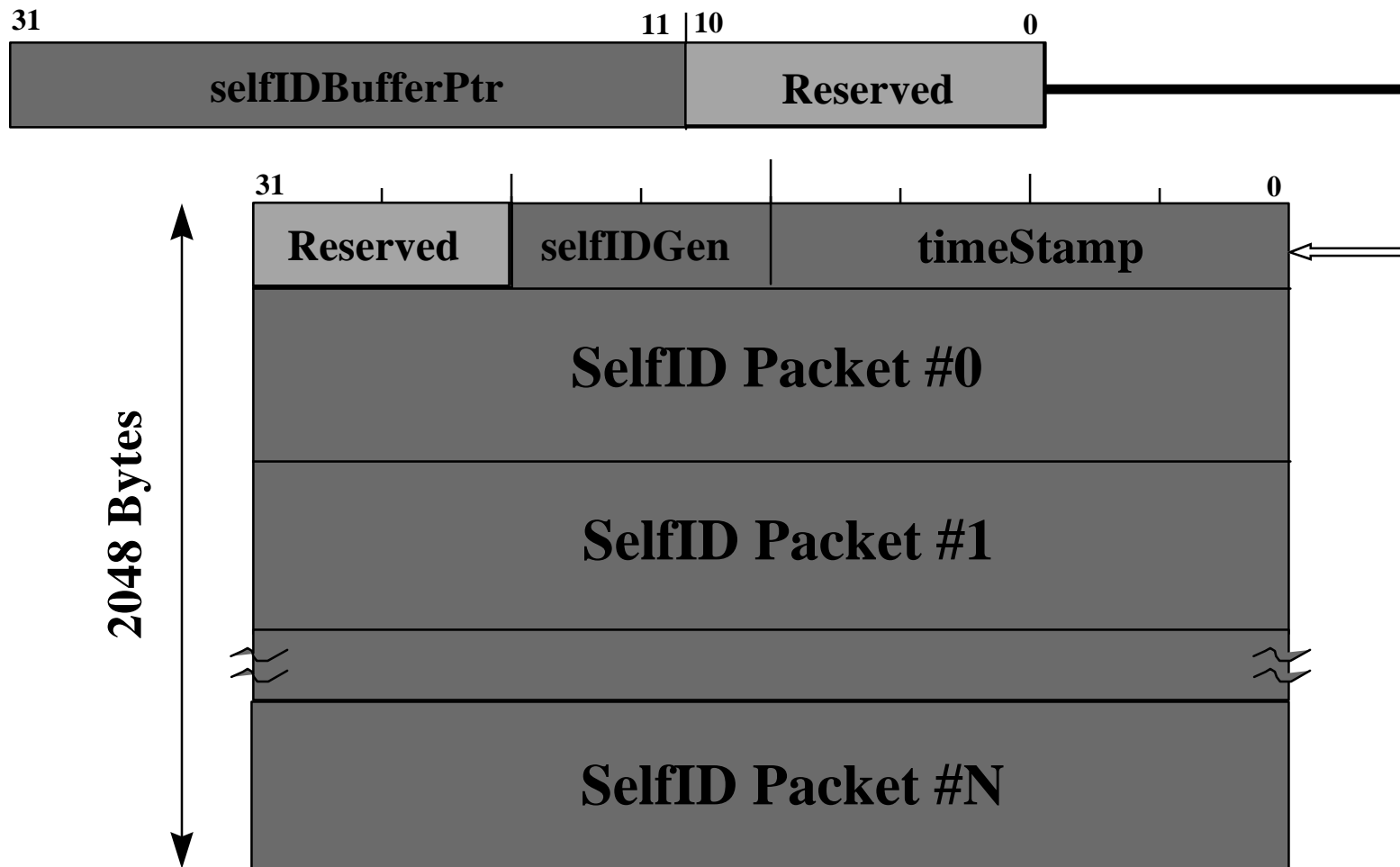
# Self ID DMA Controller



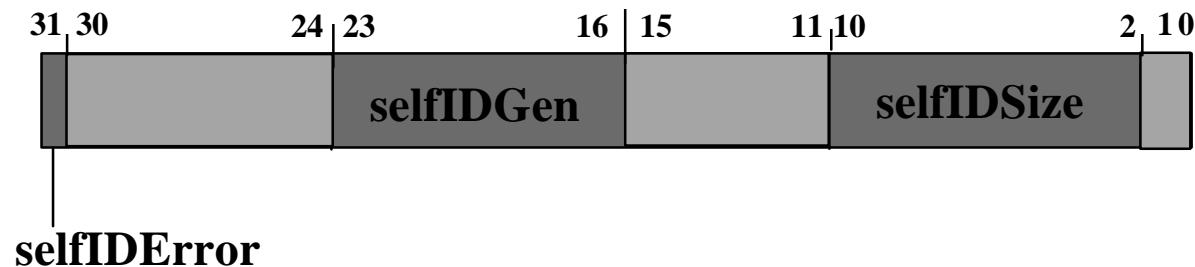
# Self ID Packets on 1394

- ◆ **During bus reset processing, each node sends out a Self-ID packet.**
- ◆ **A SelfID packet contains 1394 node information such as the Node Number and Phy Speed.**
- ◆ **The Serial Bus Manager uses the Self-ID information to build the speed map and topology map.**

# Self ID Buffer Pointer Register & Buffer Format



# Self ID Count Register



- ◆ **SelfIDSize** is the length in quadlets of selfID data
- ◆ **SelfIDGeneration** is incremented after the bus reset
- ◆ **SelfIDError** - any error during SelfID reception

# Other Issues

- ◆ **Enabling**
  - **RcvSelfID bit in the LinkControl register**
- ◆ **Interrupts**
  - **SelfIDcomplete bit in the IntEvent register**
- ◆ **Self IDs Outside of Bus Initialization**
  - **go to AR DMA in PHY packet format**



# Physical Requests





# What is Physical Request?

- ◆ **Host Memory Addresses**  
**4 GB  $\Leftrightarrow$  32 bits**
- ◆ **Compare-Swap Registers of Isochronous Resource Management**
- ◆ **1KB of the Configuration ROM Address Space**
- ◆ **Other requests are directed to AR DMA**



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# 4GB Host Memory Reads & Writes

- ◆ **48'h0000xxxxxxxx**
- ◆ **the lower 32 bits are used as the memory address of the transaction.**
- ◆ **Filter registers are used to determine if the request will be accepted.**



# 4 CSRs of Isochronous Resource Management

- ◆ **48'hFFFFFF000021C - 48'hFFFFFF0000228**
- ◆ **Mapped to the corresponding HC registers**
  - **BUS\_MANAGER\_ID**
  - **BANDWIDTH\_AVAILABLE**
  - **CHANNELS\_AVAILABLE\_HI**
  - **CHANNELS\_AVAILABLE\_LO**



# 1KB of the Config ROM Address Space

- ◆ **48'hFFFFFF0000400 - 48'hFFFFFF00008FC**
- ◆ **Mapped to/by the corresponding HC registers**
  - **Config ROM header**
  - **Bus ID**
  - **Bus options**
  - **Global unique ID**
  - **Configuration ROM**
- ◆ **Only quadlet reads are permitted.**
- ◆ **Larger ROMs can be emulated by the AR DMA.**

# Request Filter Registers

- ◆ **64 b AsynchronousRequestFilter Register**
- ◆ **64 b PhysicalRequestFilter Register**
- ◆ **The request filters are not applied to quadlet read requests directed at the Config ROM nor to accesses directed to the isochronous resource management registers.**

# Other Issues

- ◆ **Physical request handling never generates an interrupt.**
- ◆ **On a bus reset, all pending physical requests are discarded.**
- ◆ **If the target is busy the `MaxPhysRespRetries` in the `ATRetries` Register gives the number of retries.**