1394 HCI PEN

OHCI Registers and Interrupts

Lee Wilson, IBM

Joe Bennett, Intel

1394 HCI OPEN

Set/Clear Registers

- Some registers have separate set and clear addresses
- This avoids the need to perform read/mask/write operations
  - A ‘1’ in the set register sets the bit. A ‘1’ in the clear register clears the bit
  - A ‘0’ in either register leaves the bit unchanged
- These registers are marked as “set” and “clear” registers

1394 HCI OPEN

Interrupt Registers

- **Event (set and clear) and Mask (set and clear)**
- **Specific bits**
  - **DMA complete**
    - **Asynch request & response, isoch transmit & receive**
  - **Asynch Context Progress**
    - **Receive Request Received, Receive Response Received**
  - **Erroneous Behavior**
    - ***Posted write*: Asynch data received and acknowledged, but there was an error sending it to memory**
    - ***Cycle Lost*: A cycle start was expected, not received**
    - ***Cycle Inconsistent*: Cycle start number didn't match Cycle Timer Register**
    - ***Unrecoverable*: Some error causing all or some subunits to stop (such as master abort on a context program fetch)**
    - ***Cycle Too Long*: > 125 usec between cycle start and subaction gap**

1394 HCI OPEN

Interrupt Registers

- **Specific Bits (continued)**
  - **Self ID Complete**
  - **Bus Reset Encountered**
  - **Phy request through status transfer**
  - **Phy register received**
  - **New isoch cycle started**
  - **Cycle 64 Seconds**
  - **Vendor Specific**

Isoch Interrupt Registers

- Additionally, the Isochronous registers have more specific interrupts, with interrupt masks
  - Isoch Transmit Event (set and clear)
  - Isoch Transmit Mask (set and clear)
  - Isoch Receive Event (set and clear)
  - Isoch Receive Mask (set and clear)
- All registers are 32 bits. Each bit represents an isochronous context number

1394 HCI OPEN

Filter / Mask Registers

- **Isoch Receive Channel Mask (set and clear)**
  - **64 bit register: Bit location indicates channel number**
  - **When set, channel is masked. Packets are ignored**
- **Asynch Request Filter (set and Clear)**
  - **Used for requests that do not access first 1K of CSR Configuration ROM**
  - **64 bit register: Bit location indicates channel number**
  - **When set, request is ignored.**
- **Physical Request Filter**
  - **Used for asynch requests when the offset is below 48'h0001_0000_0000**
  - **64 bit register: Bit location indicates channel number**
  - **When set, request is ignored.**

Compare/Swap Registers

- CSRReadData - 32 bits
- CSRCompareData - 32 bits
- CSRControl
  - Compare/swap done
  - Selection
    - 2'h0 = BUS_MANAGER_ID
    - 2'h1 = BANDWIDTH_AVAILABLE
    - 2'h2 = CHANNELS_AVAILABLE_HI
    - 2'h3 = CHANNELS_AVAILABLE_LO

Host / Link Registers

- **Host Control**
  - **Link Enabled, Host Controller soft reset, PostedWriteEnable**
- **LinkControl: Specific bits**
  - **External/Internal cycle source**
  - **Enables OHCI as cycle master, enables cycle timer**
  - **Allows PHY packet and self ID reception**
- **NodeID**
  - **Valid ID, is root, cable power is OK**
  - **Bus Number, Node Number**
- **PhyControl: Register reads/writes**
  - **Register access done**
  - **4 bit address, 8 bit read data, read/write direction, 8 bit write data**

1394 HCI OPEN

ROM Registers

- **Config Rom Header (1394 spec, section 8.3.2.5.3)**
  - **Info_Length, CRC_Length, Rom_CRC_Value**
- **Bus Info Block (1394 Spec, section 8.2.3.5.4)**
  - **Bus ID**
    - **32'h31333934 = "1394"**
  - **Bus Options**
    - **IRMC, CMC, ISC, BMC, Max_Rec, Cyc_Clk_Acc**
  - **Global Unique ID Hi**
    - **24 bit Node_Vendor_ID, 8 bit Chip_ID_Hi**
  - **Global Unique ID Lo**
    - **32 bit Chip_ID_Lo**

1394 HCI OPEN

Other Registers

- **Version: OHCI major and minor versions**
  - **For 0.9, major version = “0h”, minor version = “9h”**
- **GUID ROM (optional)**
  - **Used to access the GUID ROM, if it exists**
  - **8 bit data, data ready**
- **Retries: maxiumum # of transmit retries that will be performed**
  - **4 bit Physical Response Count**
  - **4 bit Asynch Transmit Response Count**
  - **4 bit Asynch Transmit Request Count**
- **Cycle Timer**
  - **7 bit second count, 13 bit cycle count, 12 bit cycle offset**

1394 HCI OPEN Other Registers cont.

- **Configuration Rom Mapping Register**
  - **1k Aligned 32 bit address**
- **Posted Write Address**
  - **64 bit address**
  - **When a posted write error occur, 16 bit sourceID, 48 bit address stored, interrupt event is set**
  - **This is a Queue: When interrupt event cleared, next in queue appears at this address**
- **Vendor Company ID**
  - **registration number with IEEE**
  - **8 bit vendor unique, 24 bit company ID**

1394 HCI OPEN

Other Registers cont.

- ContextControl
- CommandPtr
- ContextMatch
- SelfID Registers