Software Overview of 1394 OpenHCI

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OpenHCI

An overview of the design from the driver writer's point of view

Agenda

- Asynchronous Request / Response Transmission
- Asynchronous Response Reception
- General Receive Queue
- Isochronous Transmission
- Isochronous Reception
- Physical Response Generation

Asynchronous Request / Response Transmission

DBDMA Registers

ChannelStatus

	r	p	f	w	d	a		bt	s[7:0]

For AsyncTx DMA s[5] means ‘retry needed’

ChannelControl

mask	data

CommandPtr

command pointer	

DBDMA Registers

IntSelect

	mask		value

Interrupt condition = ((ChannelStatus.s[7:0] & IntSelect.mask) == (IntSelect.value & IntSelect.mask))

BranchSelect

	mask		value

Branch condition = ((ChannelStatus.s[7:0] & BranchSelect.mask) == (BranchSelect.value & BranchSelect.mask))

WaitSelect

	mask		value

Wait condition = ((ChannelStatus.s[7:0] & WaitSelect.mask) == (WaitSelect.value & WaitSelect.mask))

DBDMA Command

cmd	s	key		i	b	w	requested count
address							
cmd dependent							
xfer status							residual count

i - interrupt:
0 - never interrupt
1 - when interrupt condition is true
2 - when interrupt condition is false
3 - always interrupt

b - branch:
0 - never branch
1 - when branch condition is true
2 - when branch condition is false
3 - always branch

w - wait:
0 - never wait
1 - when wait condition is true
2 - when wait condition is false
3 - always wait

Requests and Responses

- **Separate DBDMA channels for each**
  - **Prevents requests from blocking responses**
  - **Avoids deadlock conditions**

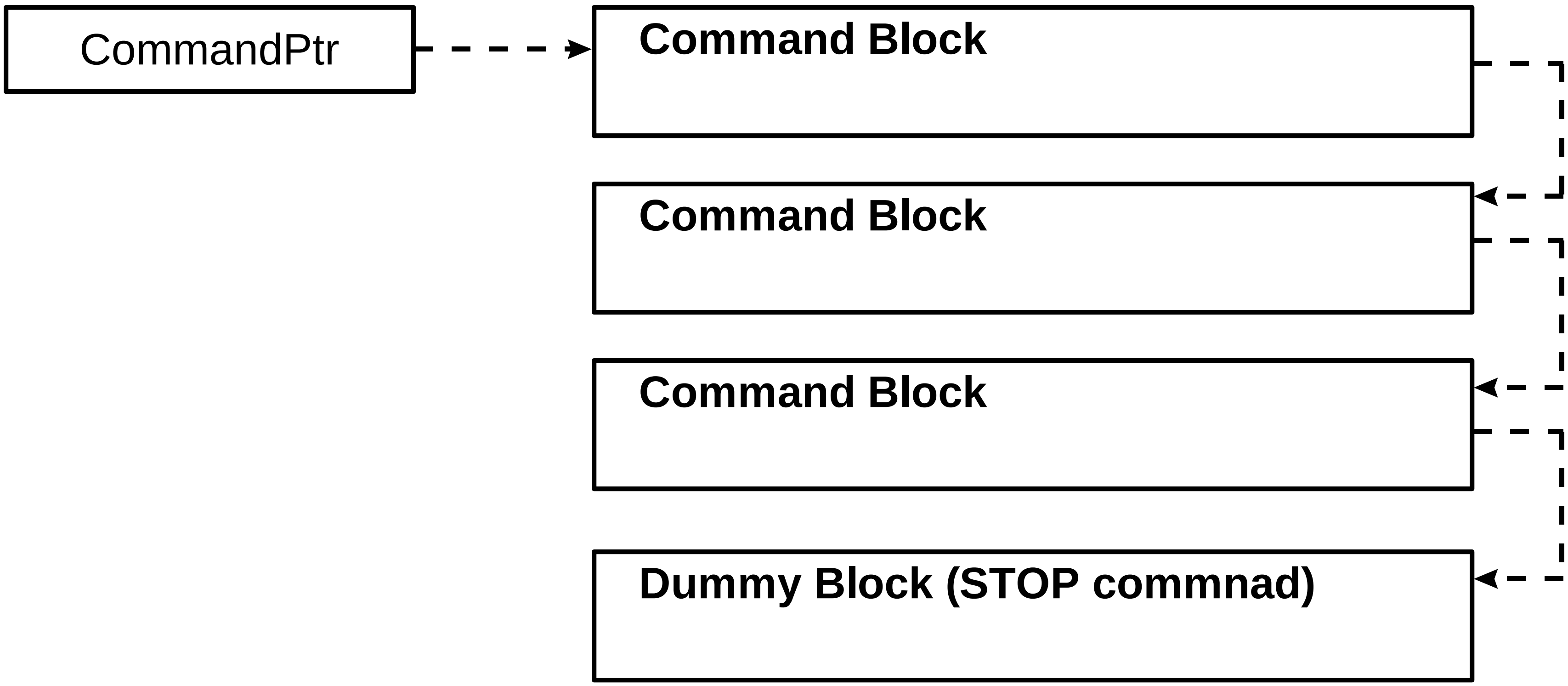
Queue Packet for Xmit

- Get memory for command block and format 'STOP' command
- Overwrite previous command block with commands for packet, overwrite 'STOP' last
- Ping ChannelControl register to set 'WAKE' bit

Start:	OUTPUT_MORE		Ad=HeaderAddr	Cnt=HeaderLen
	OUTPUT_LAST	Br(s[5])=Start	Ad=PacketAddr	Cnt=PacketLen
	NOP	Br(Always)=Next		

Next:	STOP

DBDMA Command Queue



Asynchronous Response Reception

Asynchronous Response Unit (ARSU)

- Automates response reception for tLabels between 32 and 63
- ARSU_Enable / Set / Clear registers
- ARSU_Status / Clear registers
- ARSU_TablePointer register
- ARSU table entry:

respAddr					
errCode		rCode		l	respSourceID

ARSU Use

- **Allocate an unused tLabel**
- **Set ARSU table entry**
- **Write enable bit for tLabel**
- **Wait for interrupt**
- **Clear status bit for tLabel**
- **Process stored response**

ARSU Timeouts

- **Split transaction timeout done is s/w**
- **What to do on timeout:**
  - **clear enable for tLabel**
  - **wait for pipeline to clear (next cycle start is convenient)**
  - **check status bit for tLabel**

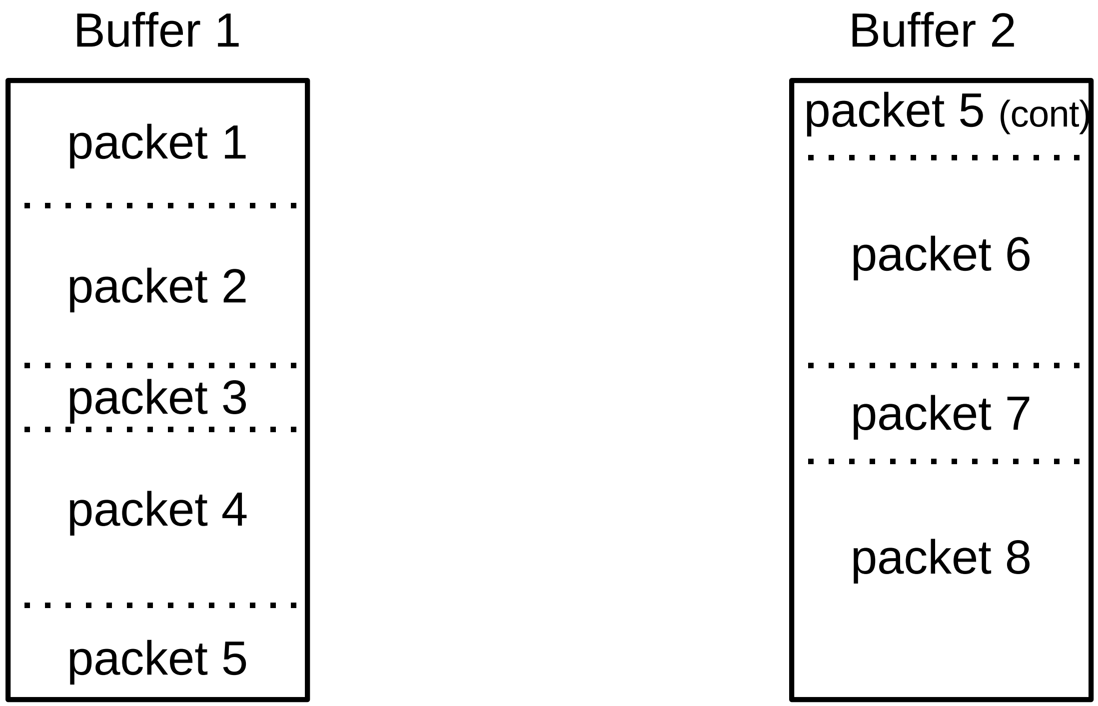
General Receive Queue

General Receive Unit (GRU)

- **Responses not handled by ASRU**
- **Requests not handled automatically**
  - **Most of CSR space**
  - **Addresses below CSR & above 4 GB**
  - **Addresses below 4 GB for untrusted nodes**
  - **All 1394 lock requests (except to Isochronous Resource Manager registers)**

GRU

- **Packets concatenated in buffer**
- **Packets may cross buffer boundaries**



GRU DBDMA Cmd Queue

CommandPtr

Start: INPUT_MORE key=bf i(packet) br(always)=Next1 Ad=buffer1 Cnt=length1

Next1: INPUT_MORE key=bf i(packet) br(always)=Next2 Ad=buffer2 Cnt=length2

Next2: INPUT_MORE key=bf i(packet) br(always)=Next3 Ad=buffer3 Cnt=length3

Next3: STOP

Isochronous Transmission

Iso Transmit (IT) Registers

Isochronous transmit table base

tablePointer	

Isochronous transmit cycle pointer

	cyclePointer	

Isochronous transmit cycle pointer limit

	cyclePointerLimit	

Isochronous transmit page size

ones	pageSizeMask	zeros

IT Table Entry

ITPDpointer		I	E	C

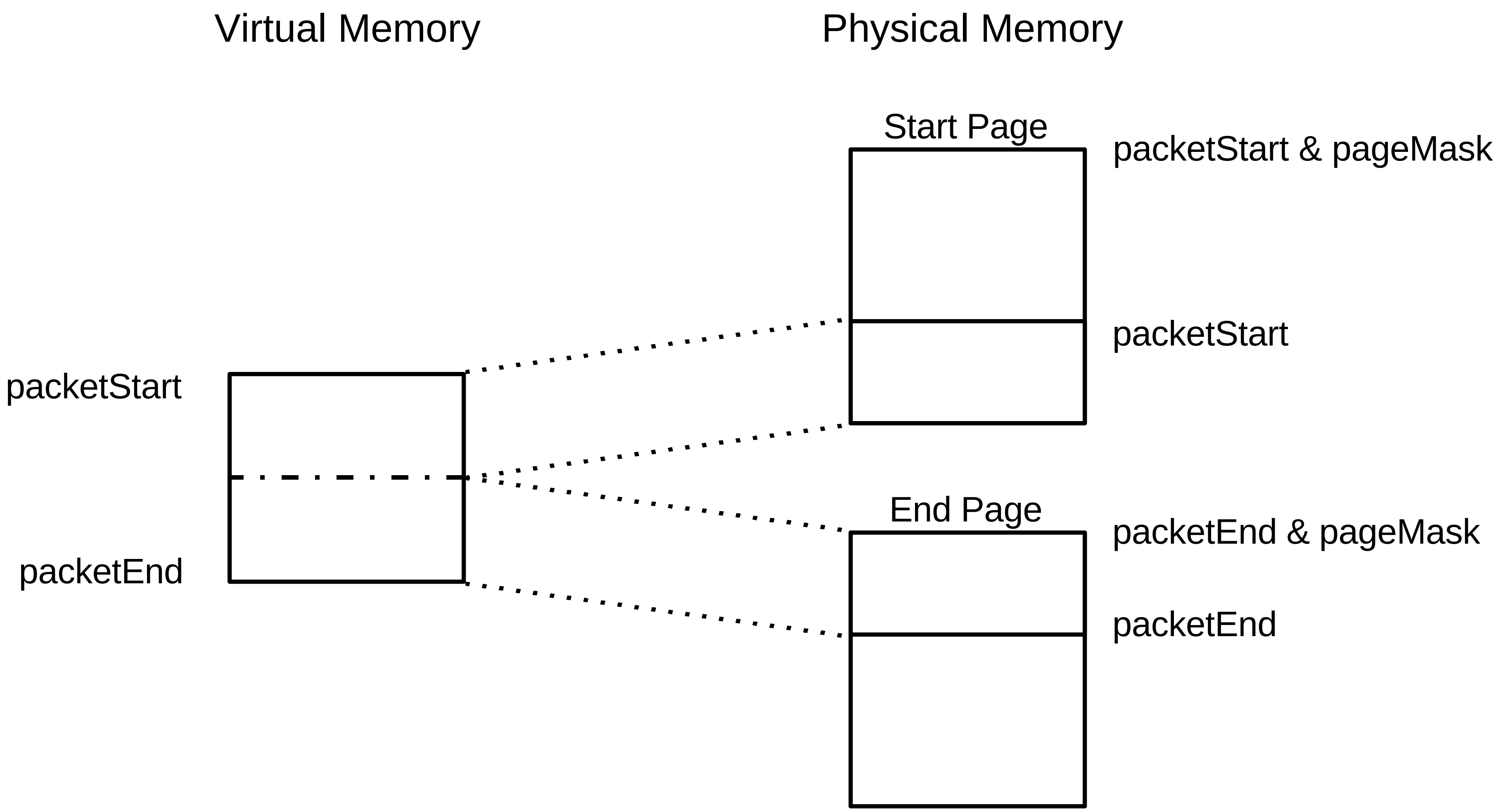
I = interrupt at this cycle
E = error in this cycle
C = complete

IT Packet Descriptor (ITPD)

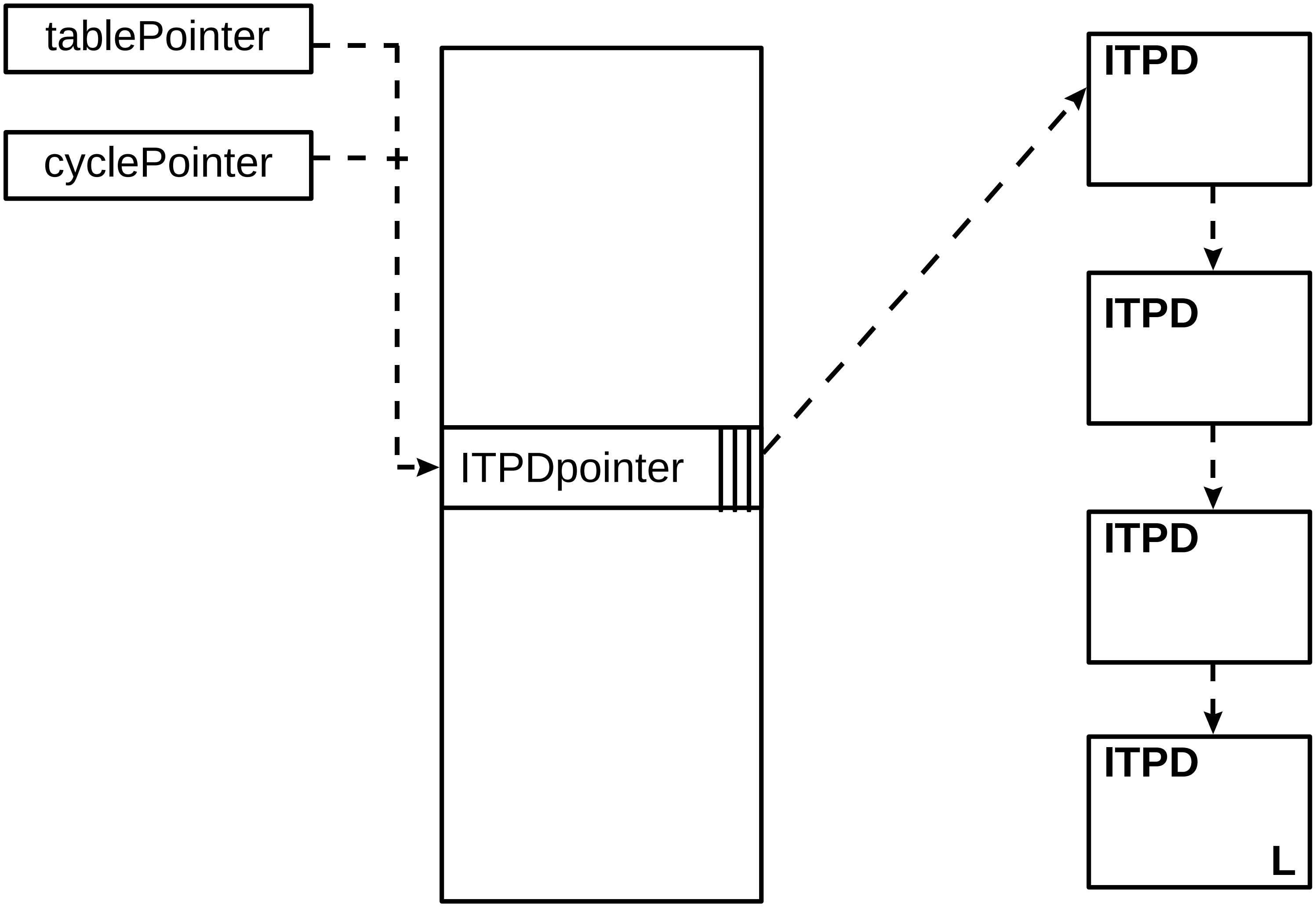
<table>
<tr><td>dataLength</td><td>tag</td><td>channel</td><td></td><td>spd</td><td>sync</td></tr>
<tr><td colspan="6">packetStart</td></tr>
<tr><td colspan="6">packetEnd</td></tr>
<tr><td colspan="4">nextITPD</td><td></td><td>L</td></tr>
</table>

L = Last in chain

Virtually Contiguous Buffer



IT DMA



tablePointer
cyclePointer
ITPDpointer
ITPD
ITPD
ITPD
ITPD
L

Isochronous Reception

Isochronous Receive (IR)

- Can use these modes
  - Buffer fill mode (like GRU)
  - Packet / buffer mode with headers
  - Packet / buffer mode without headers
- Additional DBDMA controls
  - Isochronous channel number
  - Packet SYNC match
  - Cycle seconds/count match

Packet / Buffer Example

Set cycle match register for desired start cycle

```
L1:   INPUT_LAST  key=pph  br(false)=L1        Ad=buffer1  Cnt=packetSize
      INPUT_LAST  key=pph  br(always)=Nxt1  Ad=buffer2  Cnt=packetSize

Nxt1: INPUT_LAST  key=pph  br(always)=Nxt2  Ad=buffer3  Cnt=packetSize
      ...

Last: STOP
```

Physical Response Generation

Physical Response Unit (PRSU)

- **Automatically generates responses for requests received**
  - **Isochronous Resource Manager registers**
  - **Config ROM area**
  - **Addressess below 4 GB (qualified)**

PRSU Qualifiers

- Qualifiers only apply to addresses below 4 GB
- physDMAEnable in Control register
- RequestFilterHi & RequestFilterLo registers
  - One bit to enable each node on the local bus (3FF or BusID)
  - One bit to enable all nodes on all buses
- Unqualified requests go to GRU

Questions?