IEEE 1394-1995
High Performance Serial Bus Implementation Examples

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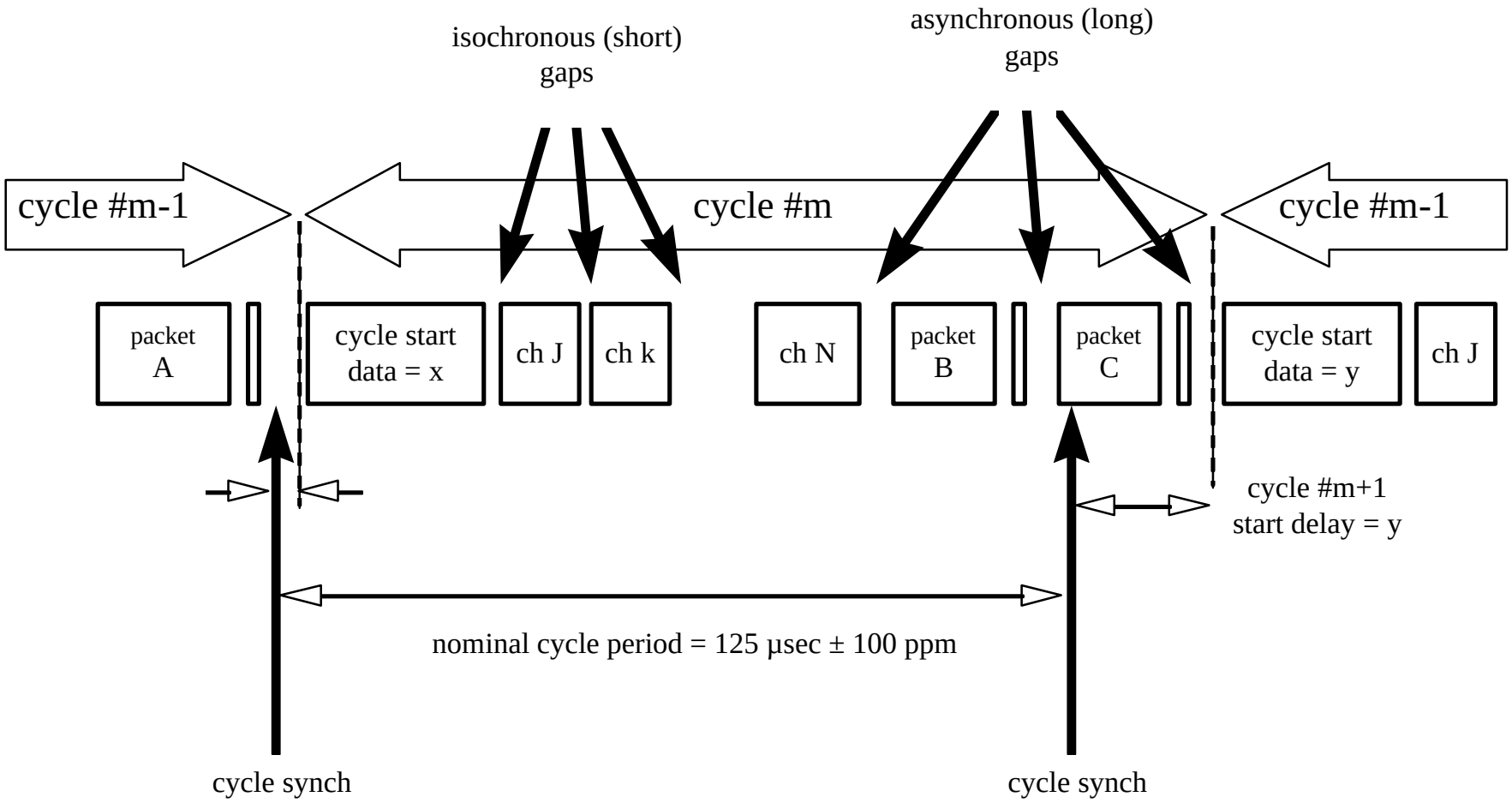
Isochronous timing

- Calculate timings for isochronous packets, and its effect on PCI requirement
- Bandwidth requirements for some example applications

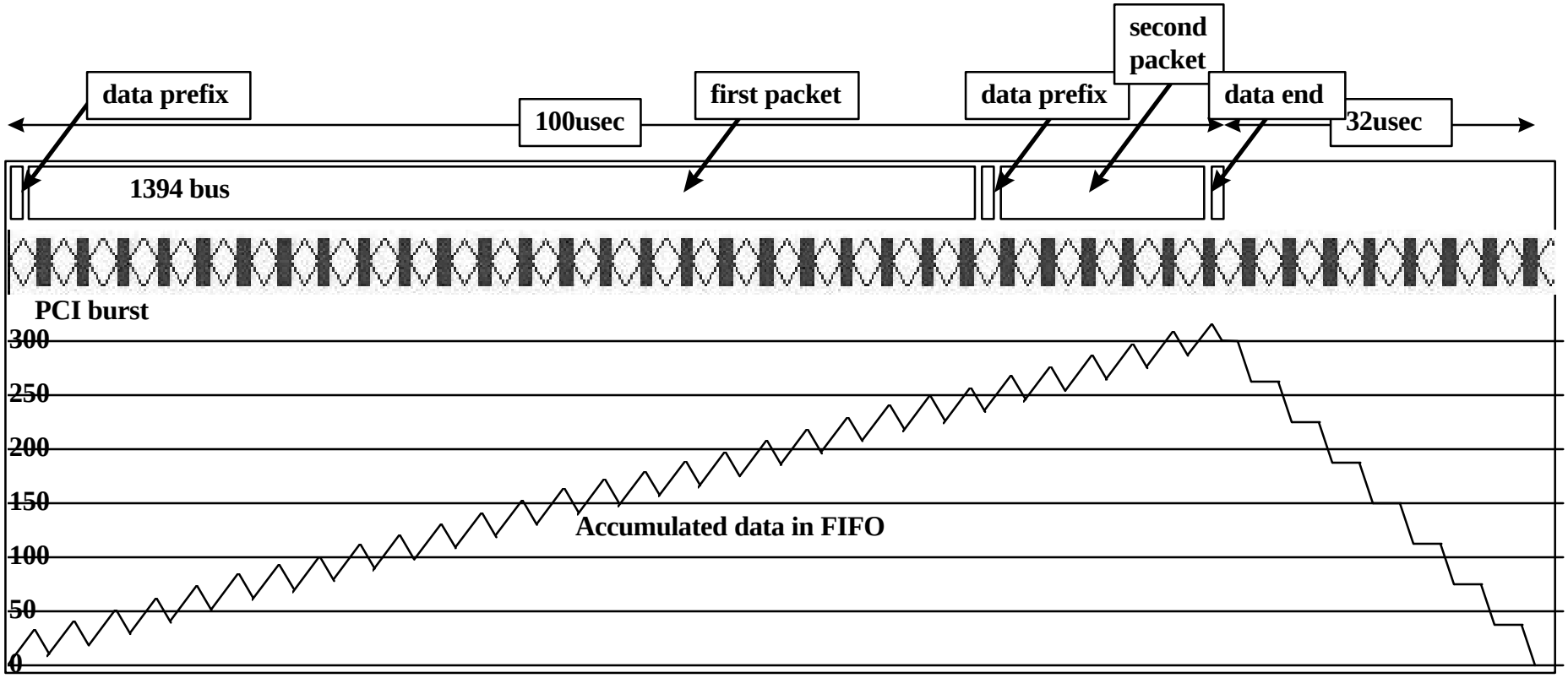
Cycle Structure



Time Components of High Efficiency Isochronous Packet

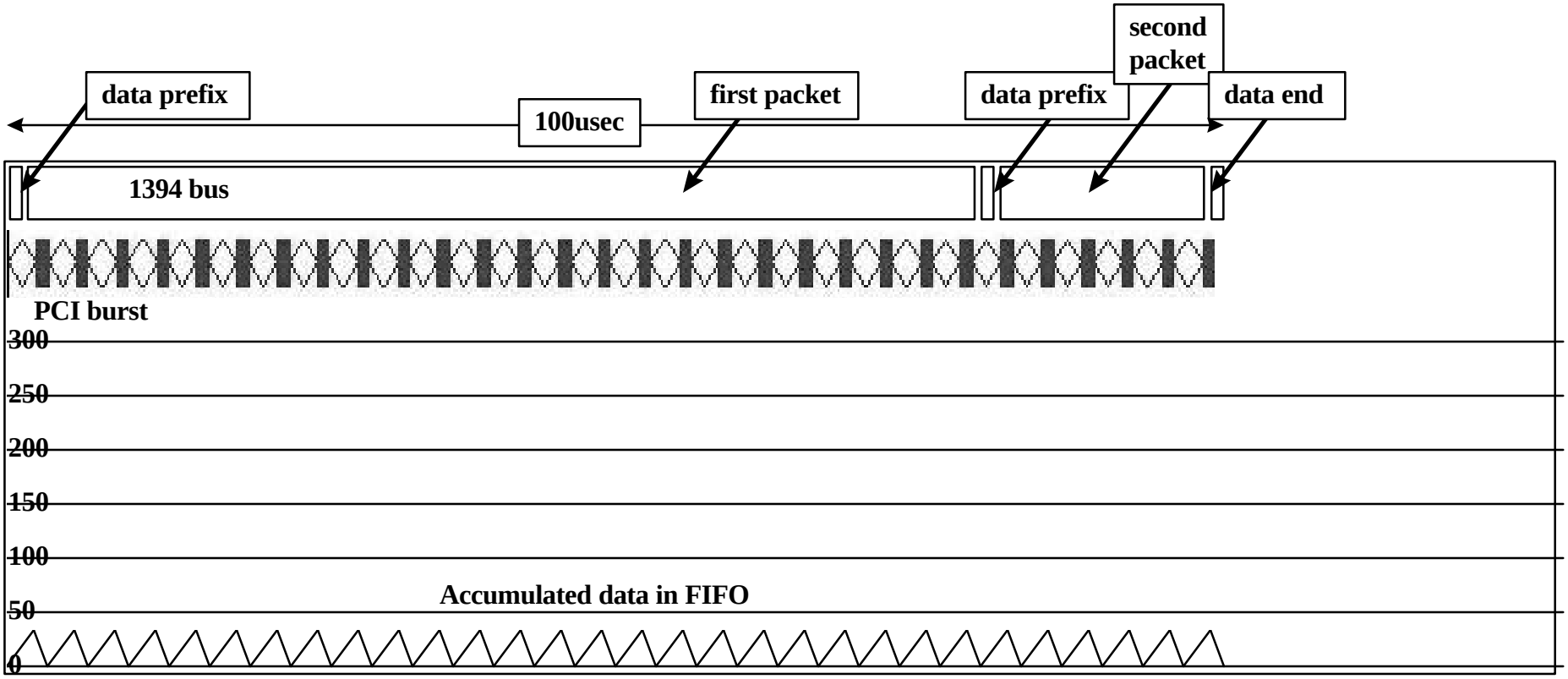
Timing parameter	time (µs)
speed_signal with data_prefix	.10
post_speed signal data_prefix	.04
Iso packet @400Mbps max size of (4096B Data+12B Header)	83.58
Min packet separation	.34
Iso packet @400Mbps size of (758B Data+12B Header)	15.67
data end time	.24
Total	~100.00
Peak bandwidth	50MB/s
Average bandwidth	48.7MB/s

PCI FIFO Size Test Case #1



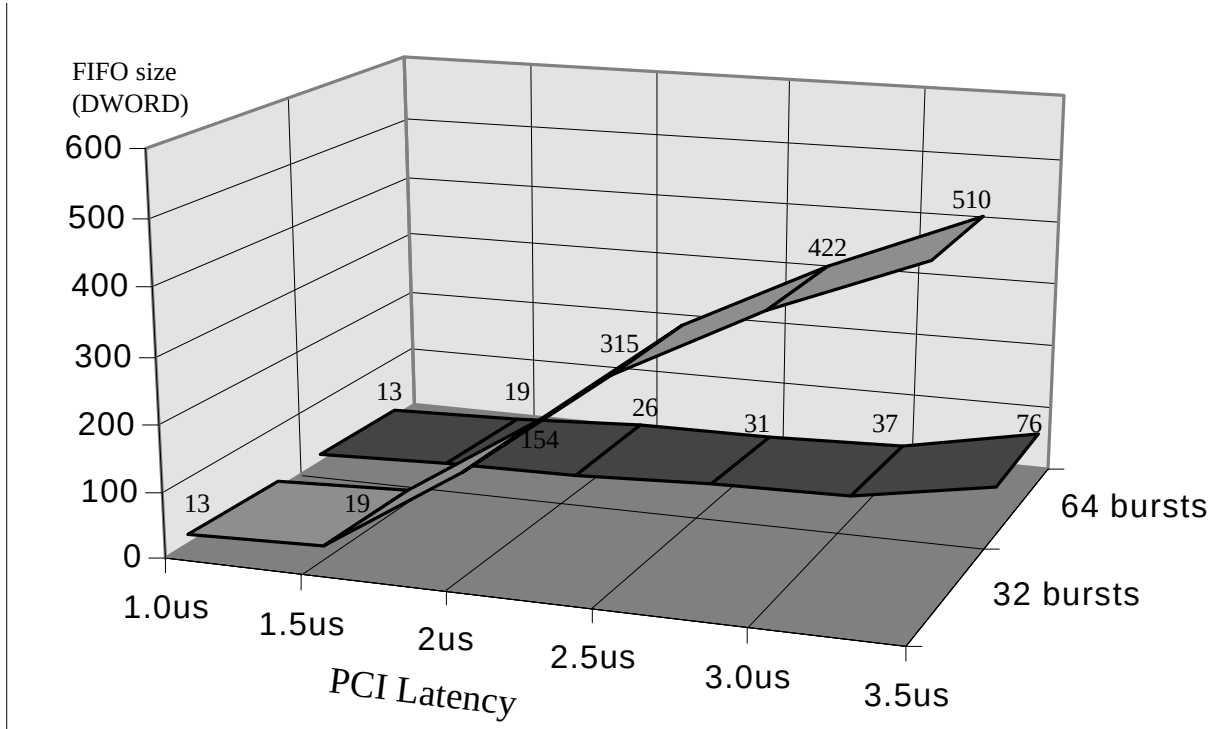
- with 2.5usec arbitration latency and burst size of 32

PCI FIFO Size Test Case #2



- with 1.6usec arbitration latency and burst size of 32

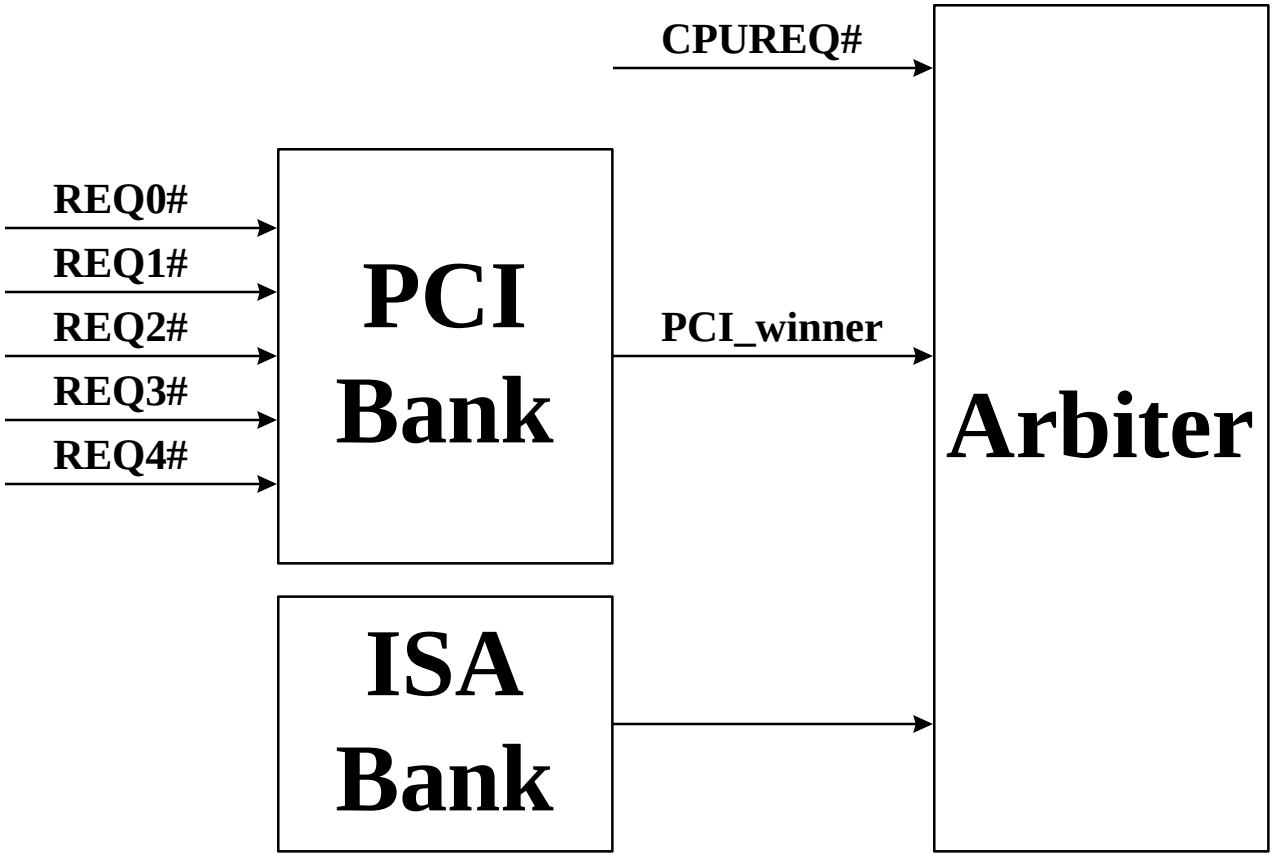
Relationship between Burst size, Latency and FIFO length



PCI Arbiter

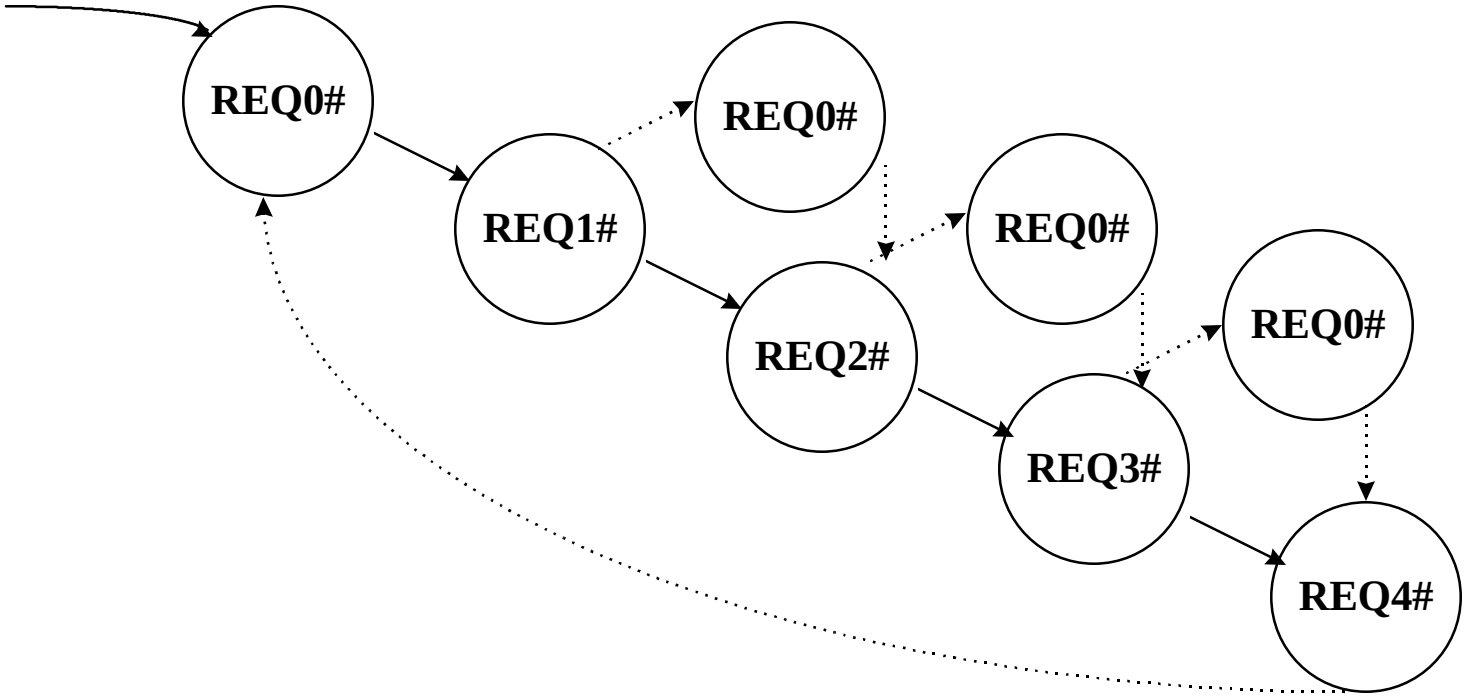
- Implementation reflects the time to assert the GNT# signal line of a PCI bus master that asserted its REQ# signal line to request bus ownership
- Arbitration algorithm of the central arbiter and the priority of the PCI resources requesting bus ownership affect the FIFO requirement
- Predictability and low latency are important

Implementation of PCI Arbiter



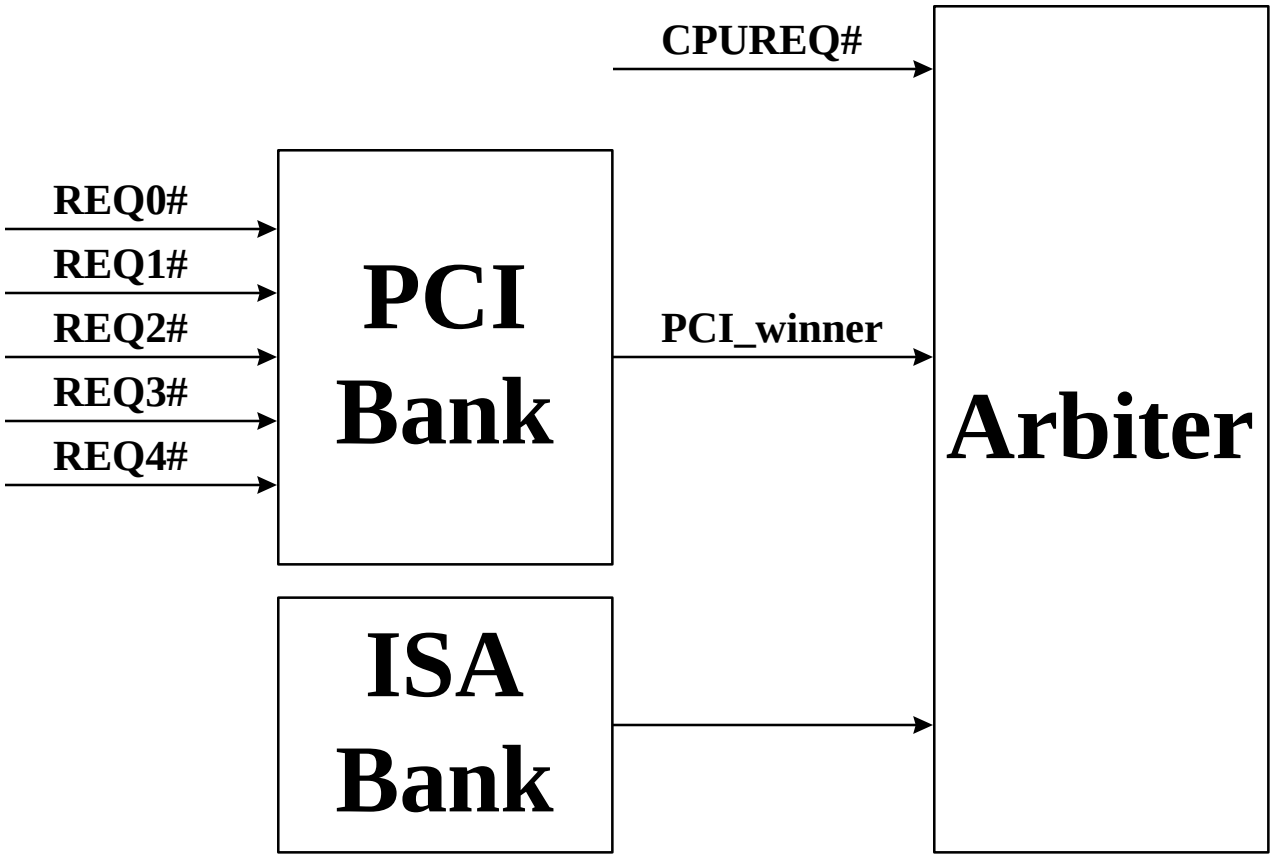
Round-robin mode

Implementation of PCI bank priority scheme



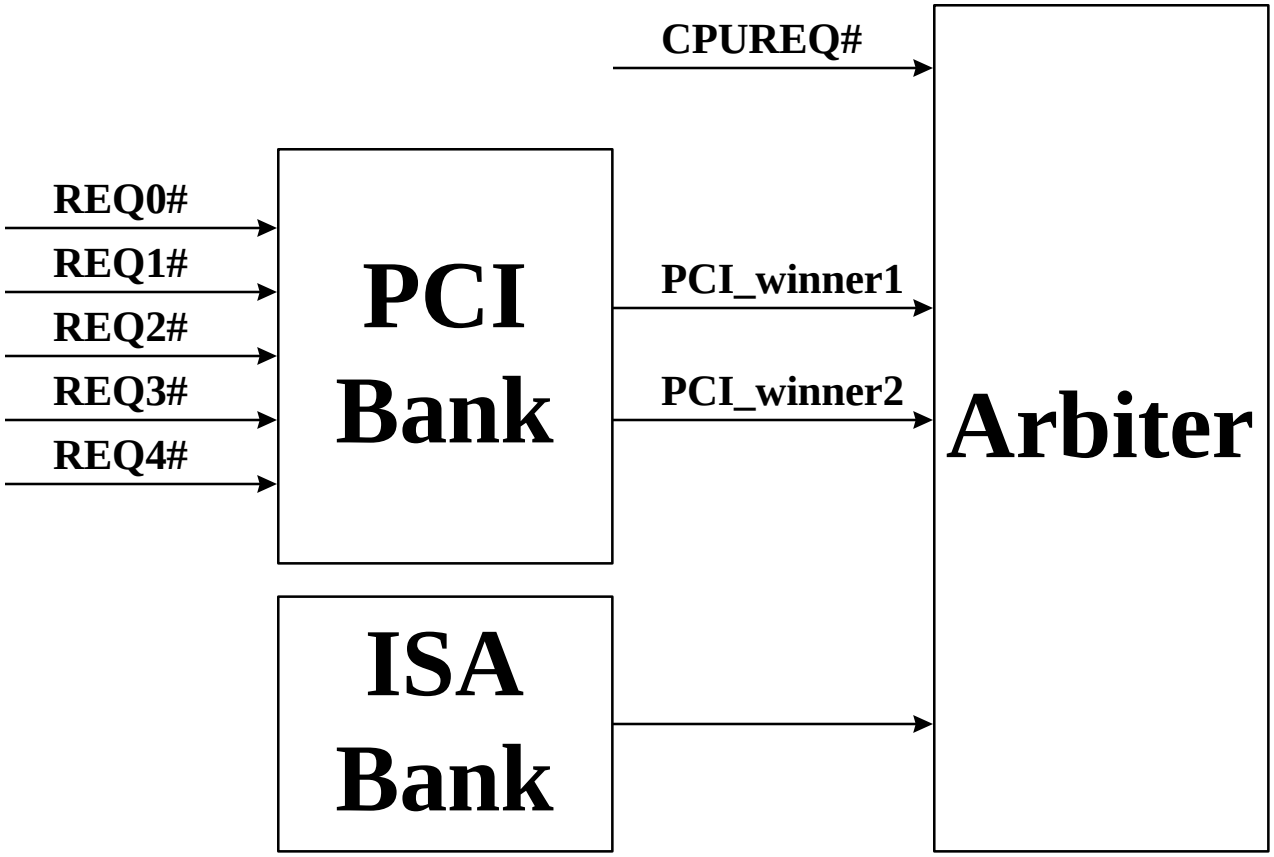
- **In controlled environment, REQ0# can win every other PCI arbitration. This gives priority to performance-hungry application like 1394 with 50% of total PCI bandwidth**

Implementation of PCI Arbiter



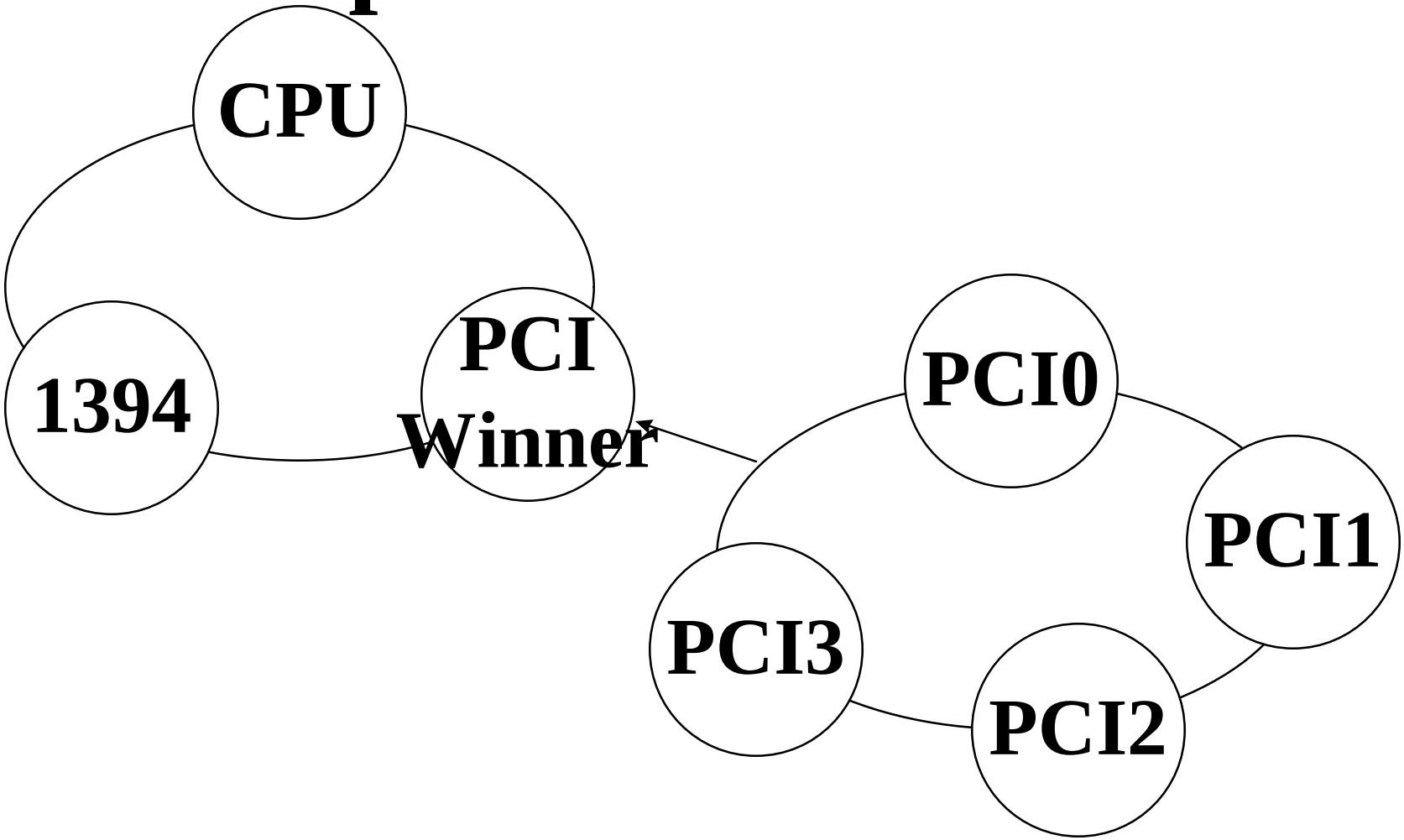
Round-robin mode with 50% chance of winning the arbitration

Other Implementation of PCI Arbiter



PCI high priority mode

One of North Bridge Implementatations



PCI Features Needed

- **FIFO requirement depends on**
  - **long bursts**
  - **fastest possible TRDY as a target**
  - **continuous IRDY# as initiator**
  - **fast back-to-back**

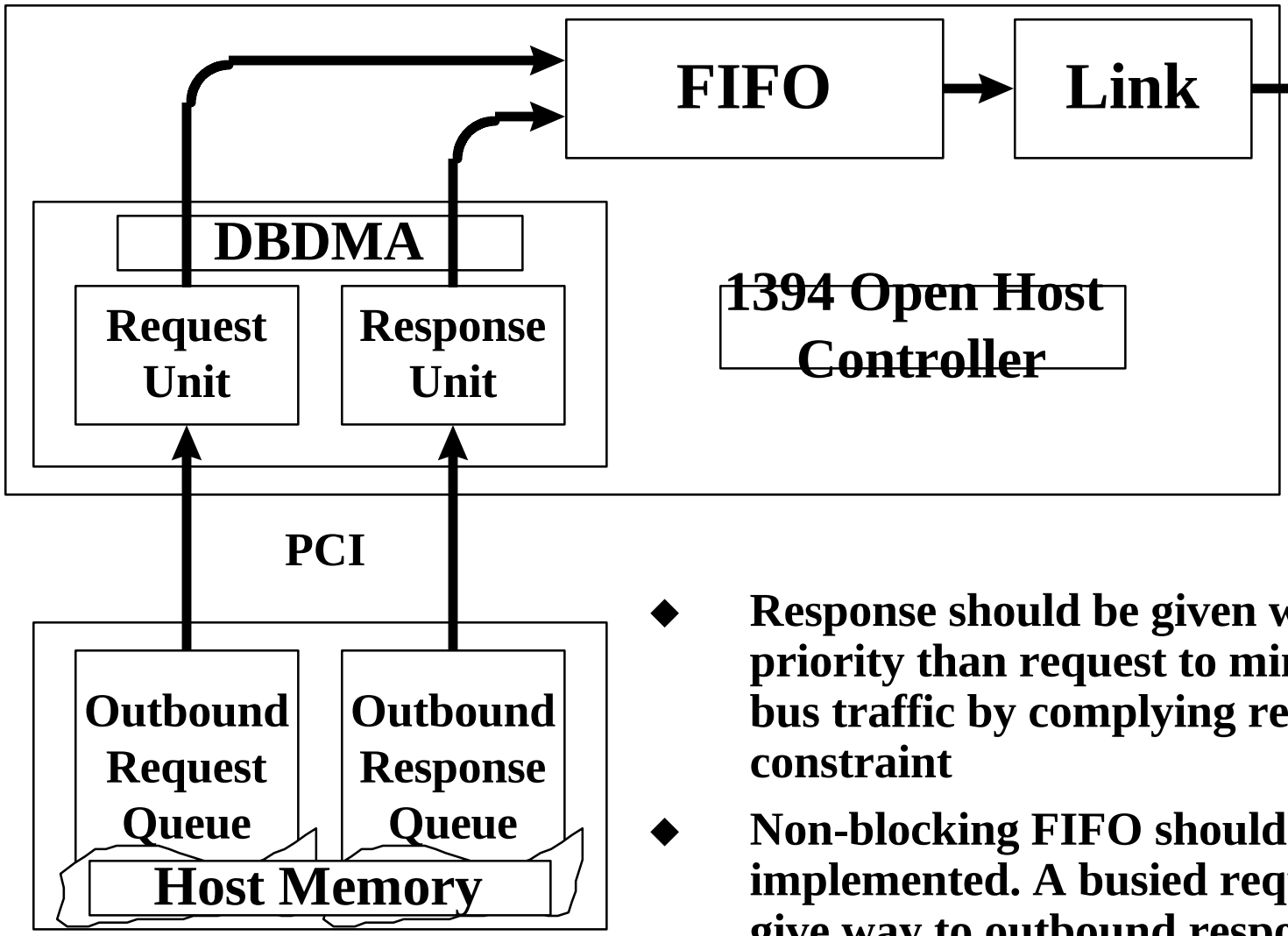
    eliminates idle cycle following a write
  - **memory write and invalidate**
    eliminates system cache snoop
  - **memory read line multiple**

    optimize system memory pre-fetching

Some Example Applications

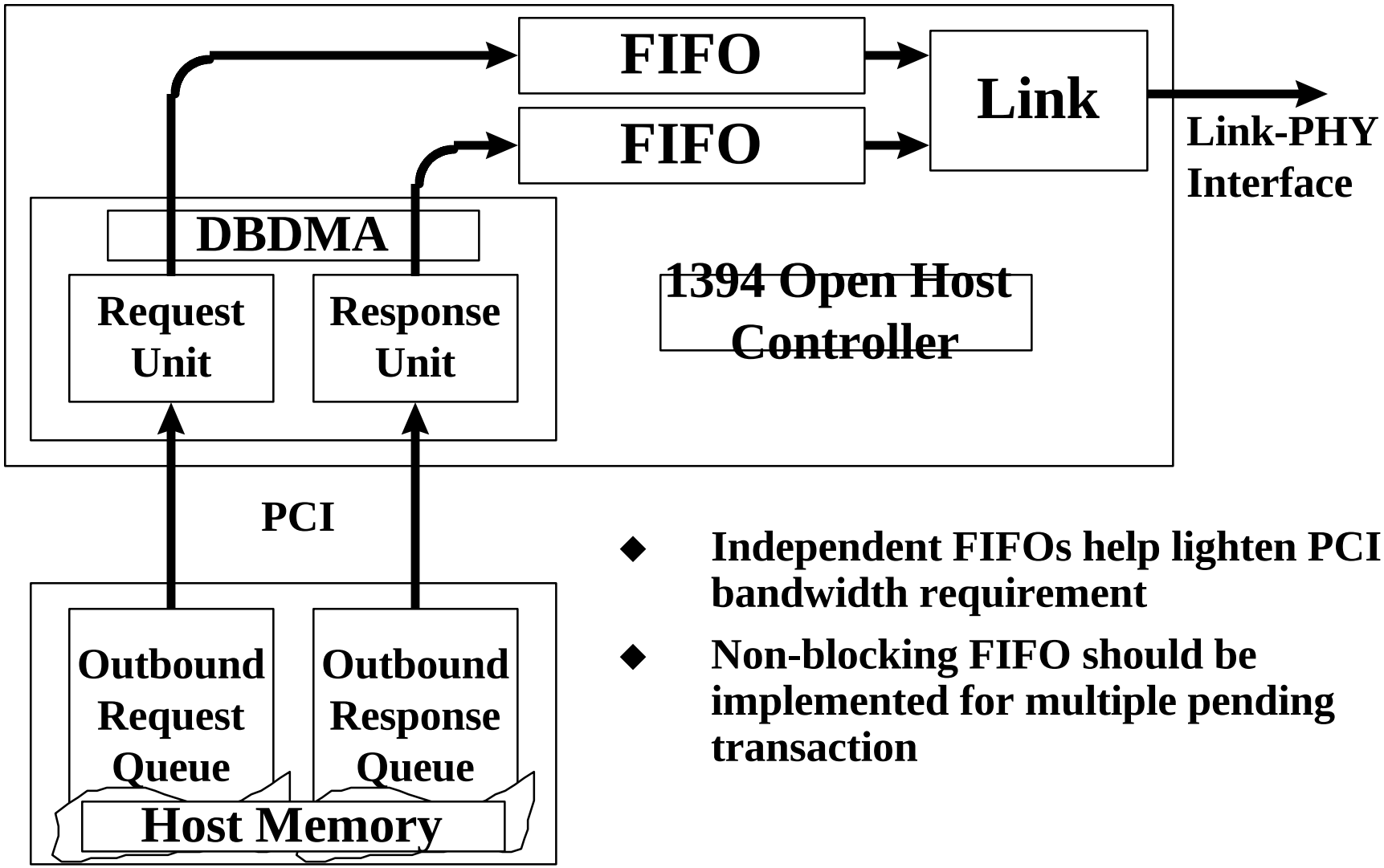
- DVCR-SD
  - Compressed video 4MB/s
- Video conferencing
  - uncompressed video 2.3MB/s
- Digital Audio
  - uncompressed audio .2MB/s

PCI Implementations



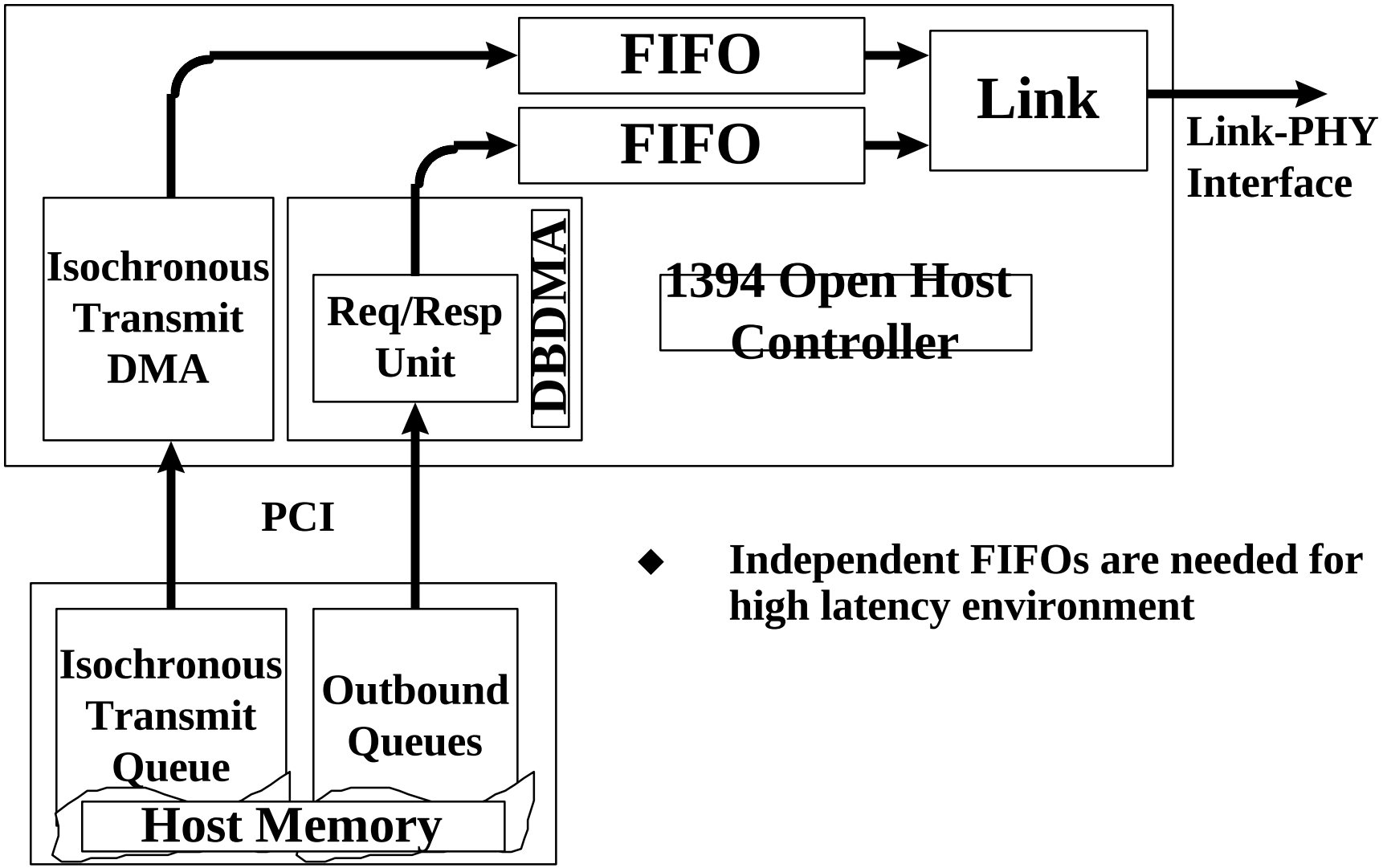
- Response should be given with higher priority than request to minimize 1394 bus traffic by complying retry timeout constraint
- Non-blocking FIFO should be implemented. A busied request should give way to outbound response

PCI Implementations



- Independent FIFOs help lighten PCI bandwidth requirement
- Non-blocking FIFO should be implemented for multiple pending transaction

PCI Implementations

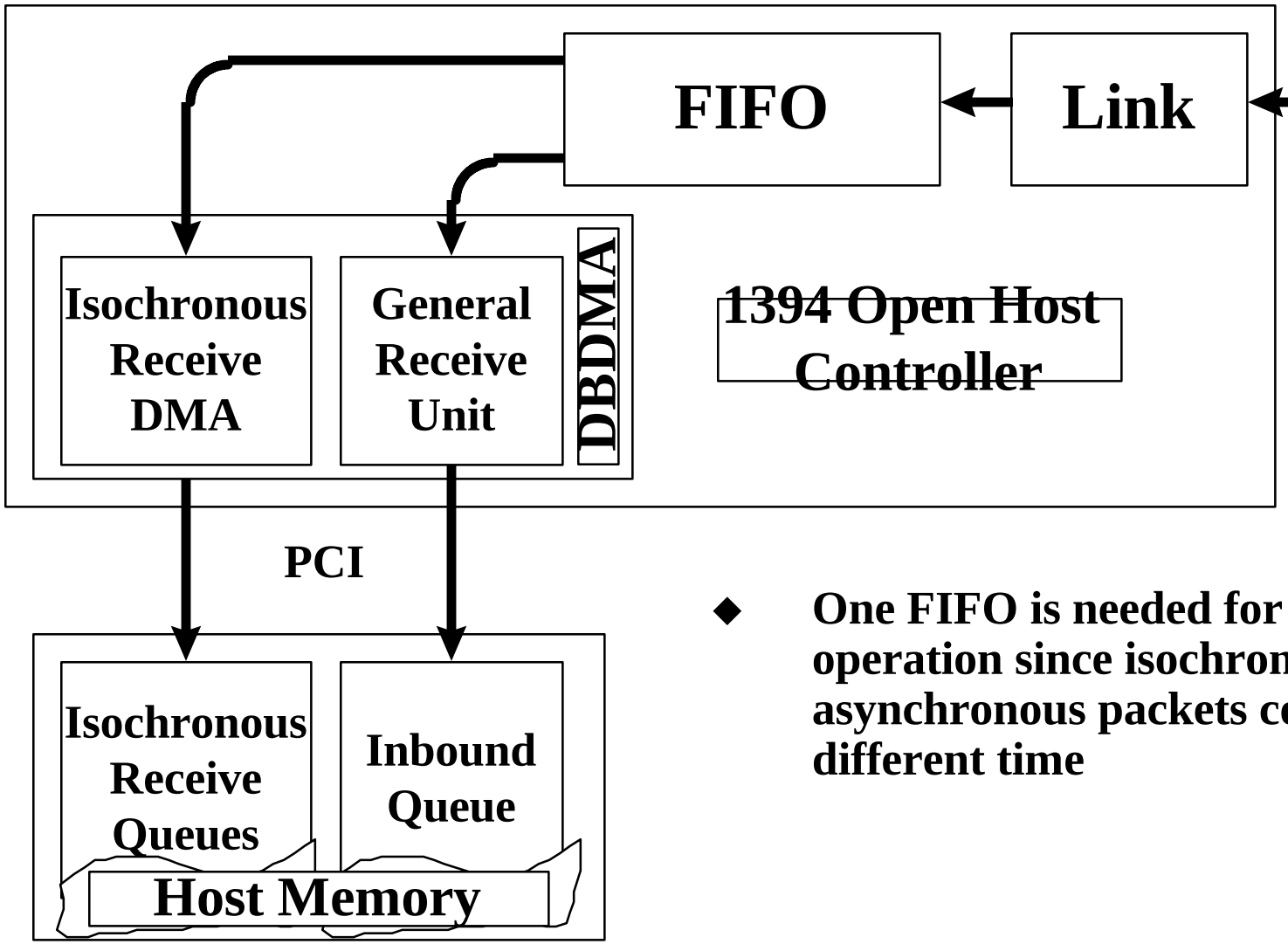


- Independent FIFOs are needed for high latency environment

High Latency Problem

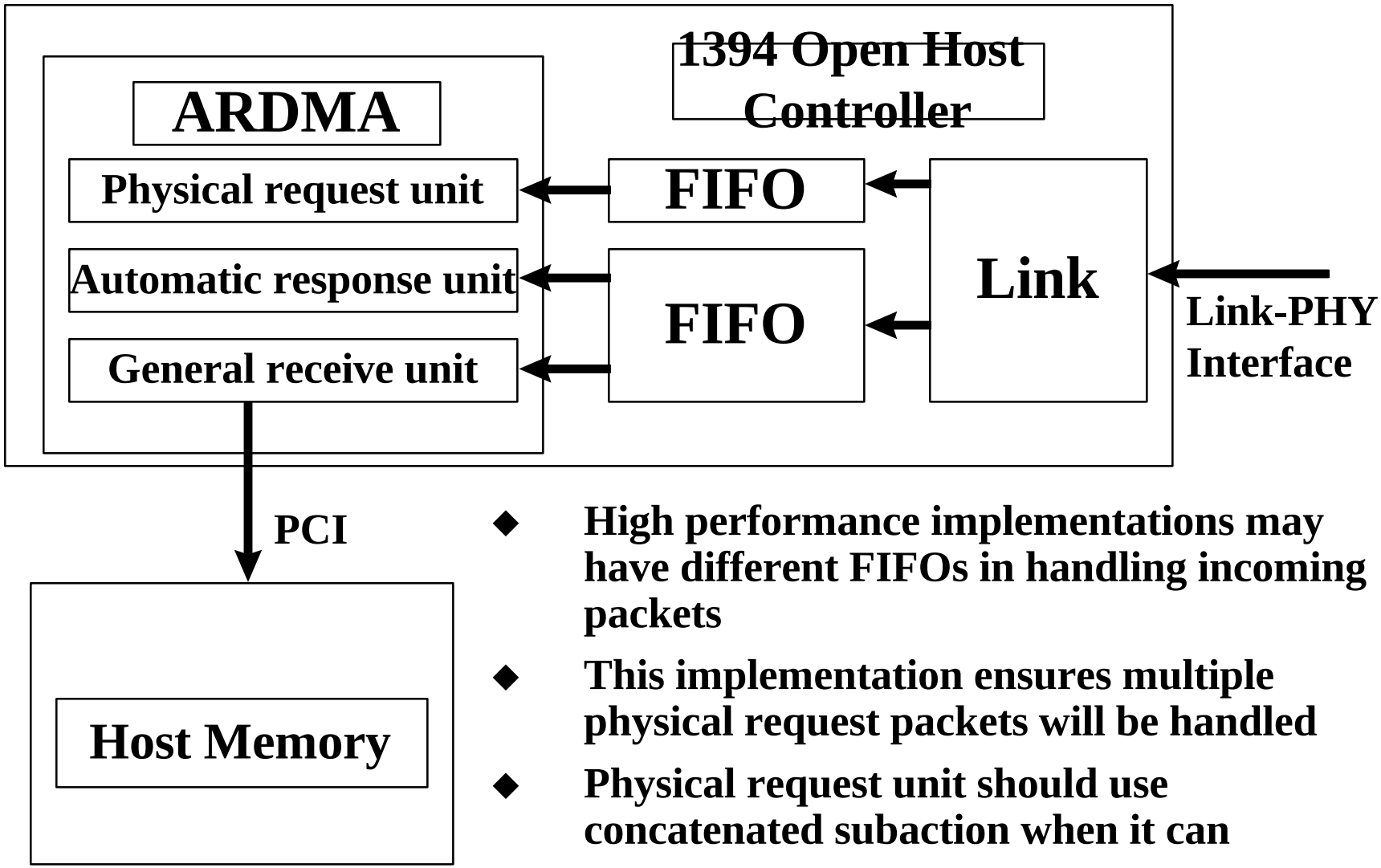
- If host bus latency can not catchup in the middle of packet in outbound async transmit,
  - FIFO underrun flag is raised
  - The DBDMA stops fetching the queue.
  - Link proceeds with partial packet. But make sure that the packet is “wrong“.
  - Link sends 2 IDLE cycles on link-PHY interface
  - PHY sends DATA_END to indicate the end of the packet
  - The receive side responds back with ACK DATA ERROR
  - DBDMA program detected the error and restarted to fetch the data

PCI Implementations



- One FIFO is needed for receive operation since isochronous and asynchronous packets come in at different time

PCI Implementations



- High performance implementations may have different FIFOs in handling incoming packets
- This implementation ensures multiple physical request packets will be handled
- Physical request unit should use concatenated subaction when it can

DBDMA Implementations

- If interrupt, branch and wait are all used and their conditions are all true in a single command descriptor, the sequence of execution is
  - processes the command, updates the status bits
  - the DBDMA engine waits until the condition is false,
  - interrupt sends to the host, and DBDMA engine jumps to the specified branch address

Retry Protocol

- Only retry_X is supported on outbound to minimize cost on a generic host controller since context per transmit has to be saved
- Retry_X and Retry_A/B may both be implemented for inbound.
- Leaf node may want to implement retry A/B on both inbound and outbound.

Bus Management CSR Register Operation

- **To update the Bus Management CSR registers:**
  - **updates csrData with the desired value**
  - **updates csrCompare with the current value**
  - **updates csrSel with proper offset**
  - **the csrData should have the old content as the one updated in the csrCompare value if compare-swap operation is successful when csrDone is set.**

Bus Management CSR Register Operation

- To read the Bus Management CSR registers
  - updates the csrData and csrCompare with the same arbitrary values
  - updates the csrSel with proper offset
  - the value is returned on the csrData if csrDone is set

Open HCI Compliant P1394A Requirements

- **Disable control per port**

  This ensures the Open HCI systems is safe from the external environment by running only on the internal nodes

Open HCI Compliant P1394A Requirements

- During self-ID process, the maximum physical_ID remains at 63 if more than 63 nodes are on the local bus. No roll over of physical_ID is allowed.
- Any PHY of physical_ID of 63 will ignore link-on and PHY-configuration packet.
- Link of physical_ID of 63 will not send any packet

Open HCI Compliant P1394A Requirements

- **Bus manager algorithm must support 3 bit speed code.**
- **If LK_EVENT.ind(cycle_too_long) is set, CONTROL.cyclemaster is cleared.**

  The cycle_too_long is defined as since the last cycle start packet was received, an 125usec has passed, and a subaction gap was not yet detected.

Open HCI Compliant P1394A Requirements

- A timeout interrupt for PHY register read shall be implemented.
- Response in first try need not to follow the fairness protocol

BUS INFO BLOCK Implementations

- **BUS INFO BLOCK is loaded by:**
  - **Hardware - loaded after chip reset by serial or parallel ROM.**
  - **Software - loaded during execution of boot code**

BUS INFO BLOCK Implementations

Info_length					CRC_length	ROM_CRC_value	
31_{16}(“1”)					33_{16}(“3”)	39_{16} (“9”)	34_{16}(“4”)
irmc	cmc	isc	bmc	reserved	cyc_clk_acc	max_rec	reserved
node_vendor_ID							chip_id_hi
chip_ID_lo							

- **Info_length specifies length of info block up to chip ID**
- **CRC length and CRC value specify area of the config ROM are CRC protected.**
- **Bus identification contains “1394”**
- **Bus Option contains irmc, cmc, isc, bmc, cyc_clk_acc, and max_rec**
- **Global Unique ID contains vendor ID and chip ID.**

BUS INFO BLOCK Implementations

- Only Bus Identification register is hardwired
- Info_length may be written with 0 to indicate that the BUS INFO BLOCK is not ready
- Bus Option, CRC length and ROM CRC value register is read/write-able. But shall be programmed first before the link on is set.

BUS INFO BLOCK Implementations

- Global Unique ID may only be written once either by hardware or software and shall be write-protected afterward
- No link on is allowed before the Global Unique ID is written

Source node's BUS ID in Response Packet

- Two BUS IDs may be used from requesters to identify the node

  3FFH (local-bus) or Specific BUS ID assigned from bus manager
- Same ID shall be used for read response packet as was used in the request packet

Source node's BUS ID in Response Packet

- Bit 23 SrcBusID of the first quadlet is provided to tell the link layer which BUS ID to be used in the response packets
  - 0 - 10h3FF is used
  - 1 - BusNumber.Node_ID is used

Other Implementation Details

- Any complete packet resided in the FIFO should not be dropped, if an ACK of COMPLETE and PENDING has been sent back to the requester. Any incoming packet will be responded with ACK of BUSY if the FIFO is not available.
- If non-header stripped mode is used, timestamp is put in the buffer. The value shall be copied from the ISO CYCLE TIMER at the time when the link sends back the ACK, or when the link receives the end of iso packet.

Other Implementation Details

- **OpenHCI implements only CSR registers of BUS MANAGEMENT CSR, and BUS INFO BLOCK in hardware. All other request packets shall be sent to GRU and PRQU accordingly for software processing.**
- **Only quadlet read/write within HCI implemented CSR registers are allowed. Otherwise, type error in response code is returned.**

End