1394 Open HCI
DMA Part II

Diana Klashman
Sun Microsystems

Agenda

- **Self-ID Buffer**
- **Automatic Response Unit**
- **Physical Requests**
- **Isochronous Transmit DMA**

Self-ID Buffer

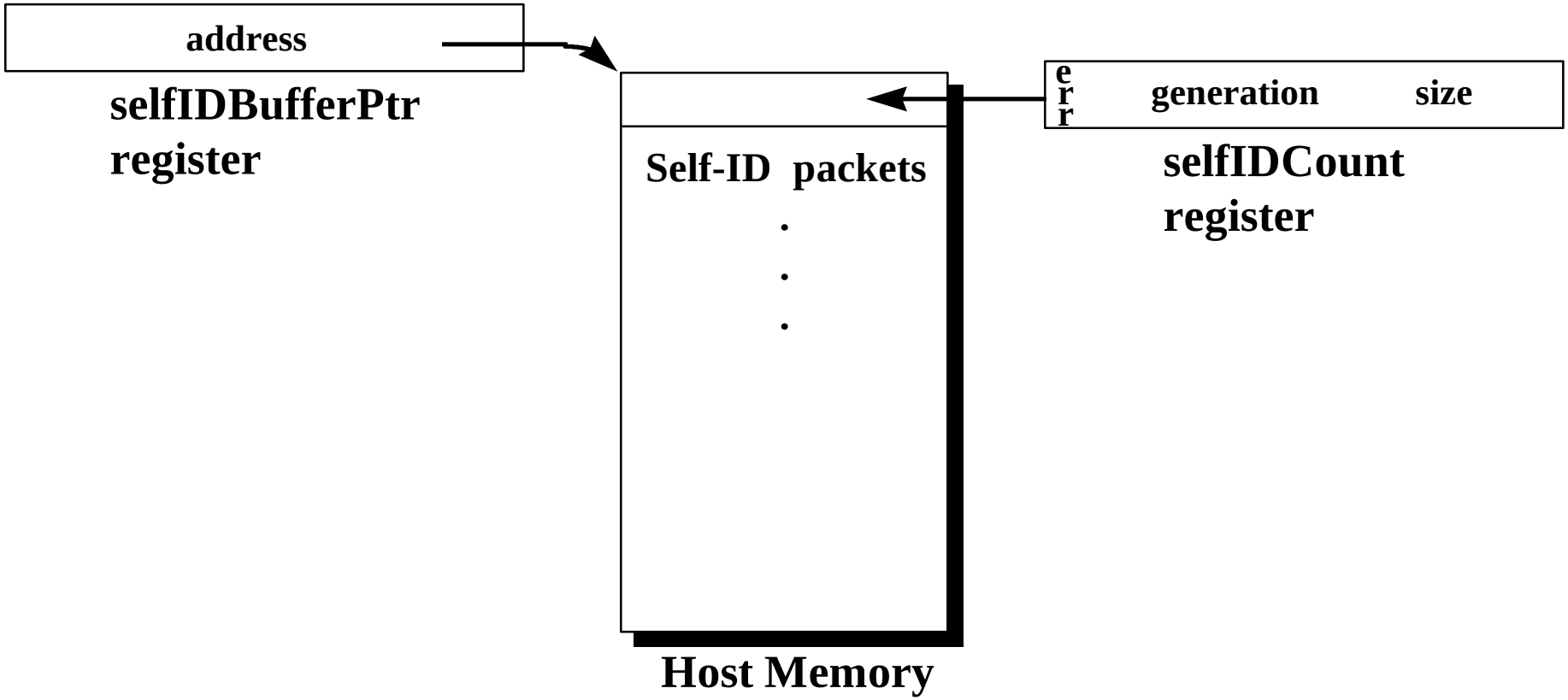
1394 OpenHCI
6.4.3

1394 Context

- During bus reset processing, each node sends out a Self-ID packet.
- A Self-ID packet contains 1394 node information such as the Node Number and Phy Speed.
- The Serial Bus Manager uses the Self-ID information to build the speed map and topology map.

Self-ID DMA

- **Open HCI will collect Self-ID packets into a specified buffer.**



Self-ID Management

- **Enabled via rcvSelfID bit in Control Register.**
- **Interrupt enabled via selfIDcomplete bit in IntEvent Register.**

Automatic Response Unit

ARSU

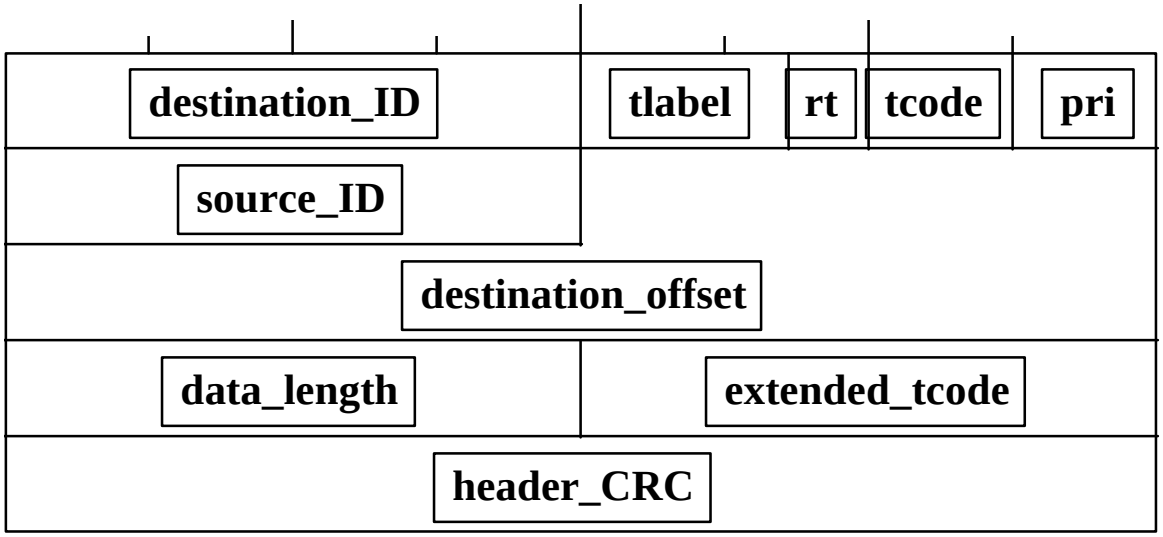
1394 OpenHCI
6.4.2

Purpose

- **Handles RESPONSES to Asynchronous Read Requests.**

1394 Context

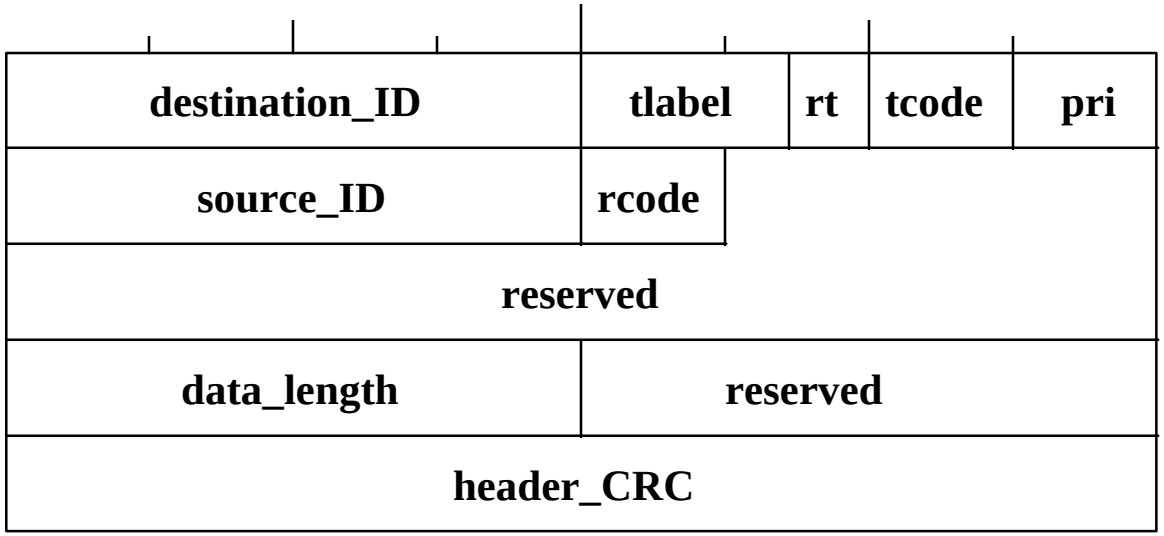
- **Asynchronous Block Read REQUEST Packet**



IEEE 1394-1995
6.2.2.2.1

1394 Context (cont)

- **Asynchronous Block Read RESPONSE Packet**

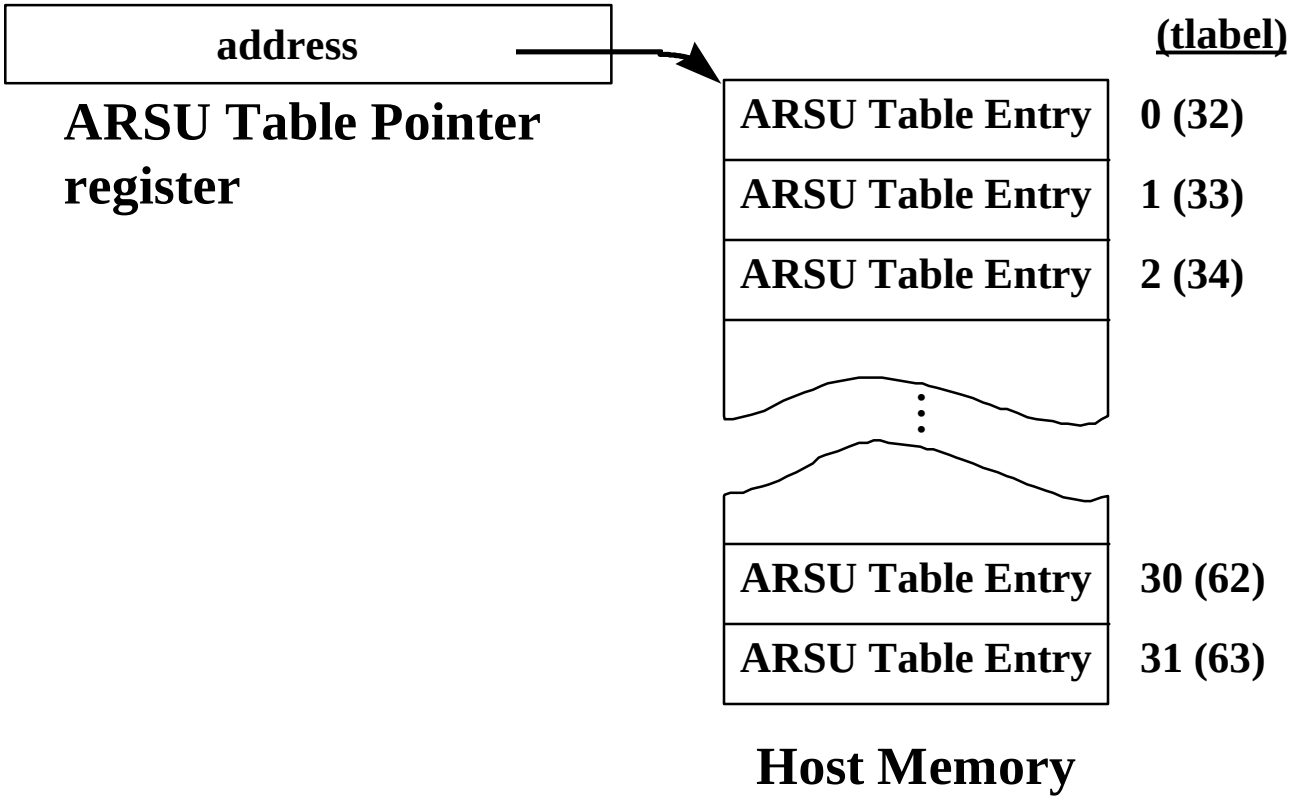


IEEE 1394-1995
6.2.2.3.3

Automatic Response Unit Description

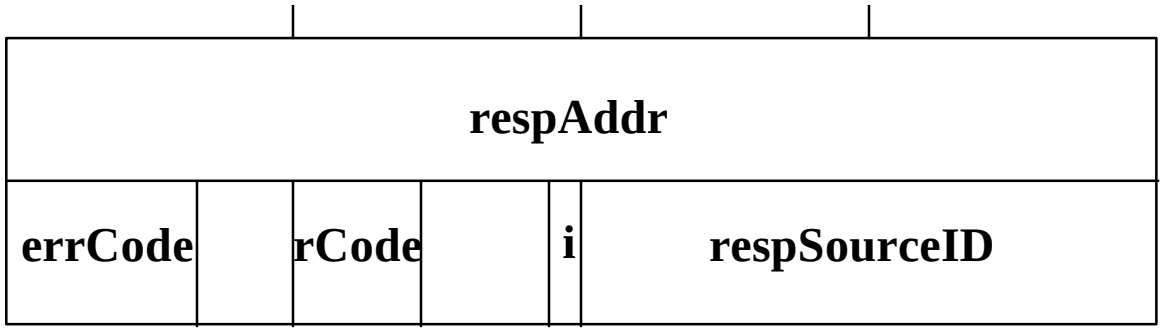
- Mechanism to direct response data into Host Memory.
- Accomplished by keying off of the transaction label.
- Otherwise, Response Packets
  - Would go into General Receive Buffer
  - Must be parsed by the host processor
  - Must be copied to the final destination

Automatic Response Unit Table

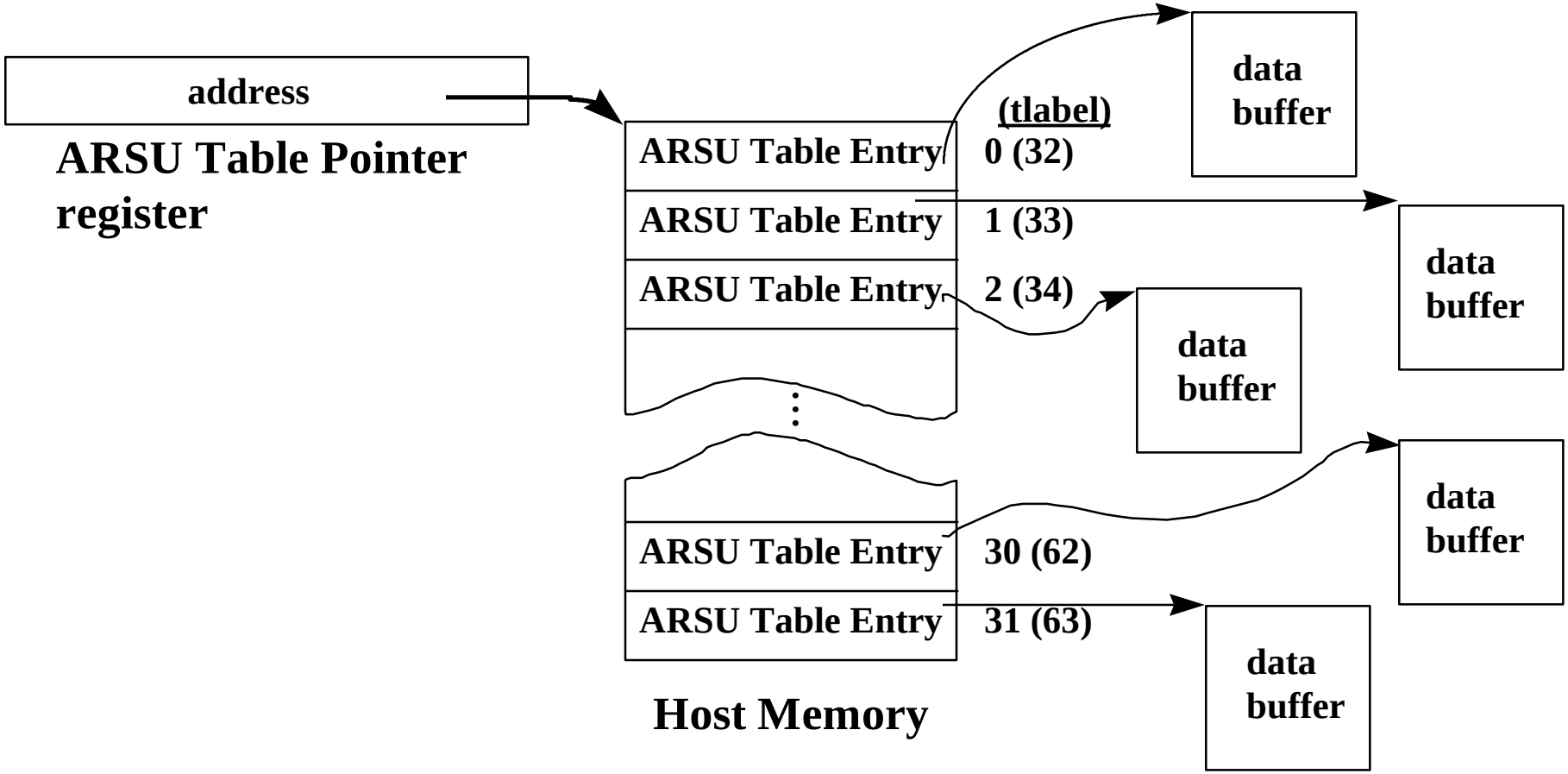


Automatic Response Unit Table Entry

- 2 Quadlets
- Points to Receive Data Buffer
- Contains Expected Source ID

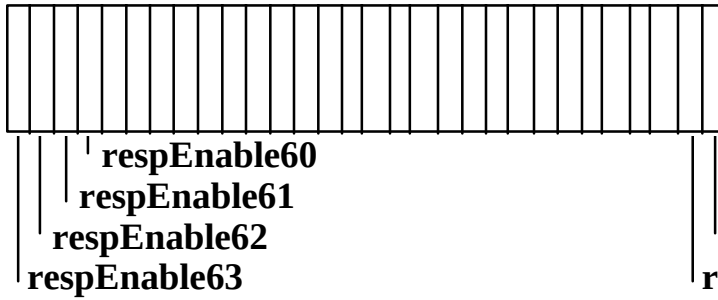


Automatic Response Unit Data Structures

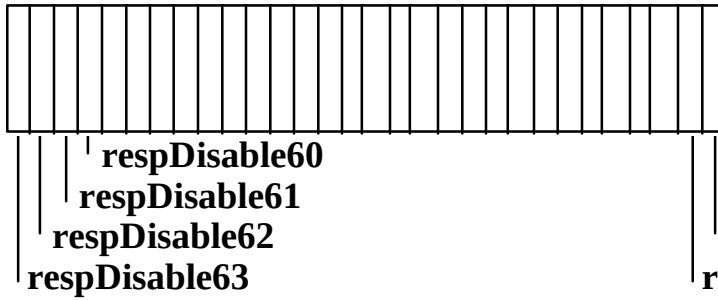


Automatic Response Unit Enable Registers

ARSU Enable register

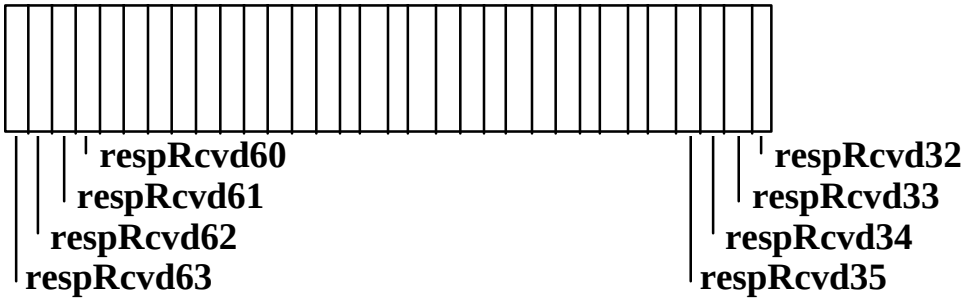


ARSU Enable Clear register

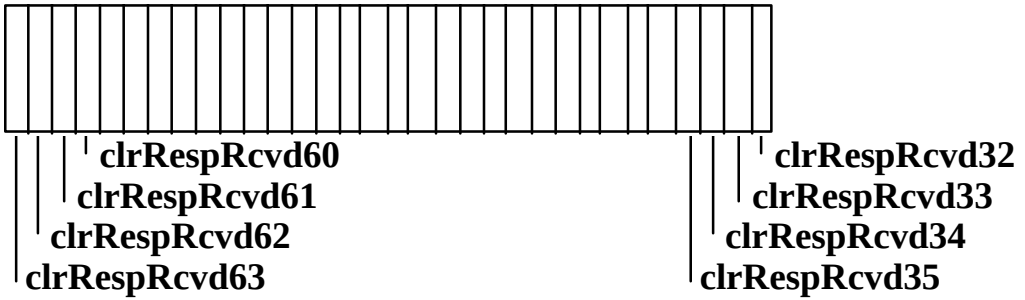


Automatic Response Unit Status Registers

ARSU Status register



ARSU Status Clear register



Physical Requests

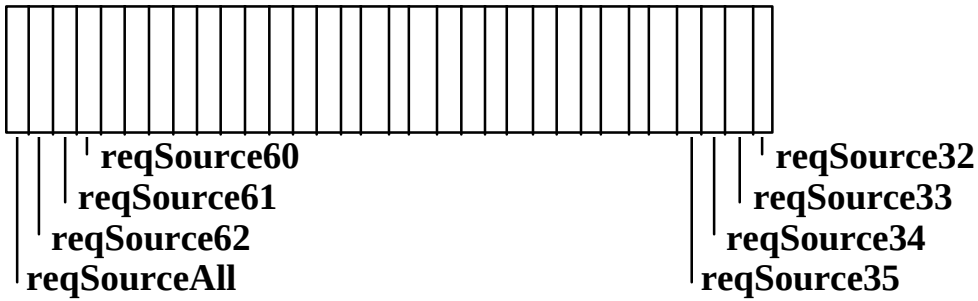
1394 OpenHCI
6.4.4

Memory Address Reads & Writes

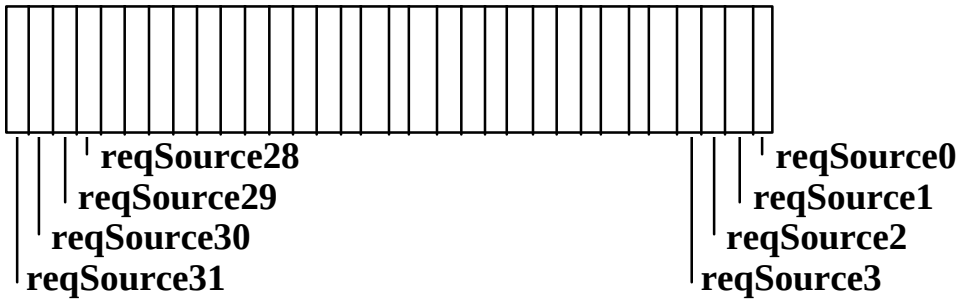
- In a Request, if the high order 16 bits of the offset address are 0, the lower 32 bits are used as the memory address of the transaction.
- Filter registers are used to determine if the request will be accepted.

Request Filter Registers

RequestFilterHi register



RequestFilterLo register

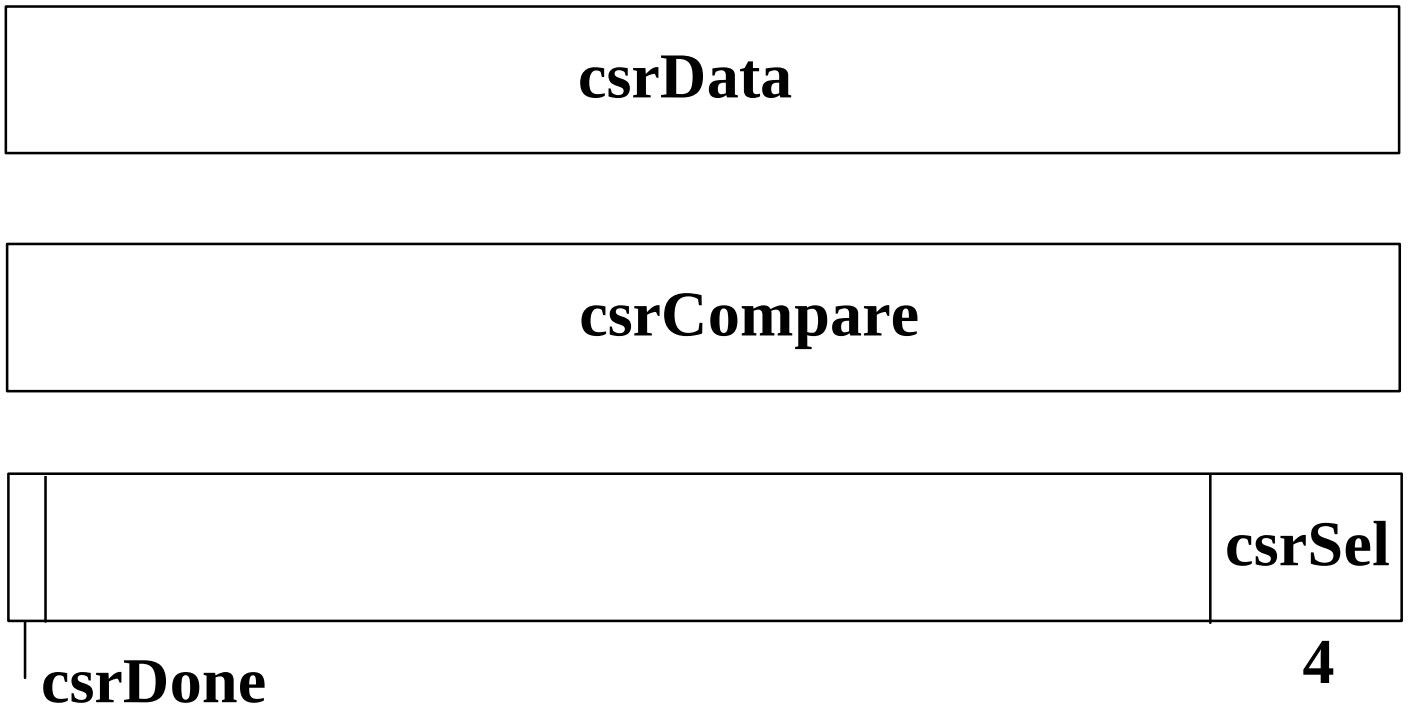


Isochronous Resource Management Register Addresses

- Reads and compare swaps to the following addresses will be handled by the OpenHCI chip.
  - BUS_MANAGER_ID
  - BANDWIDTH_AVAILABLE
  - CHANNELS_AVAILABLE_HI
  - CHANNELS_AVAILABLE_LO

Compare/Swap Registers

- **Provide compare swap functionality to local system software.**



Bus_Info_Block Quadlet Reads

- A quadlet read to any of the following addresses will be handled by the Open HCI chip.
  - Bus ID --- 1st quadlet of the Bus_Info_Block
  - Bus options --- 2nd quadlet of the Bus_Info_Block
  - Global Unique ID --- 3rd & 4th quadlet

Configuration ROM Mapping Register

- Contains start address within system bus space that maps to 1394 Config ROM.
- First 1K bytes are mapped.
- Only quadlet reads are permitted.
- Larger ROMs can be implemented in the GRU.
- First 5 quadlets (bus_info_block) are mapped to registers.

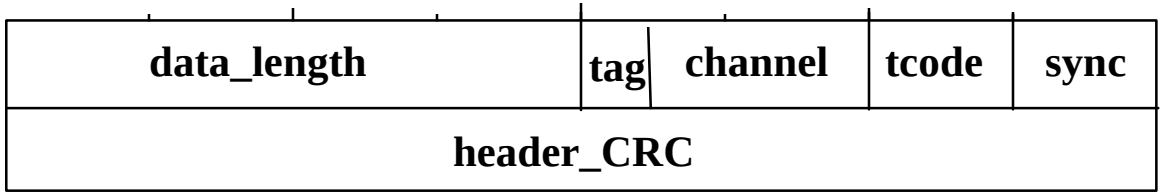
Isochronous Transmit

1394 OpenHCI
6.3

1394 Context

- Isochronous bandwidth is allocated for use by a specific channel.
- Isochronous packets contain a Channel Number
  - They do NOT contain a Destination Node ID or Address.

Isochronous Data Block Packet Header



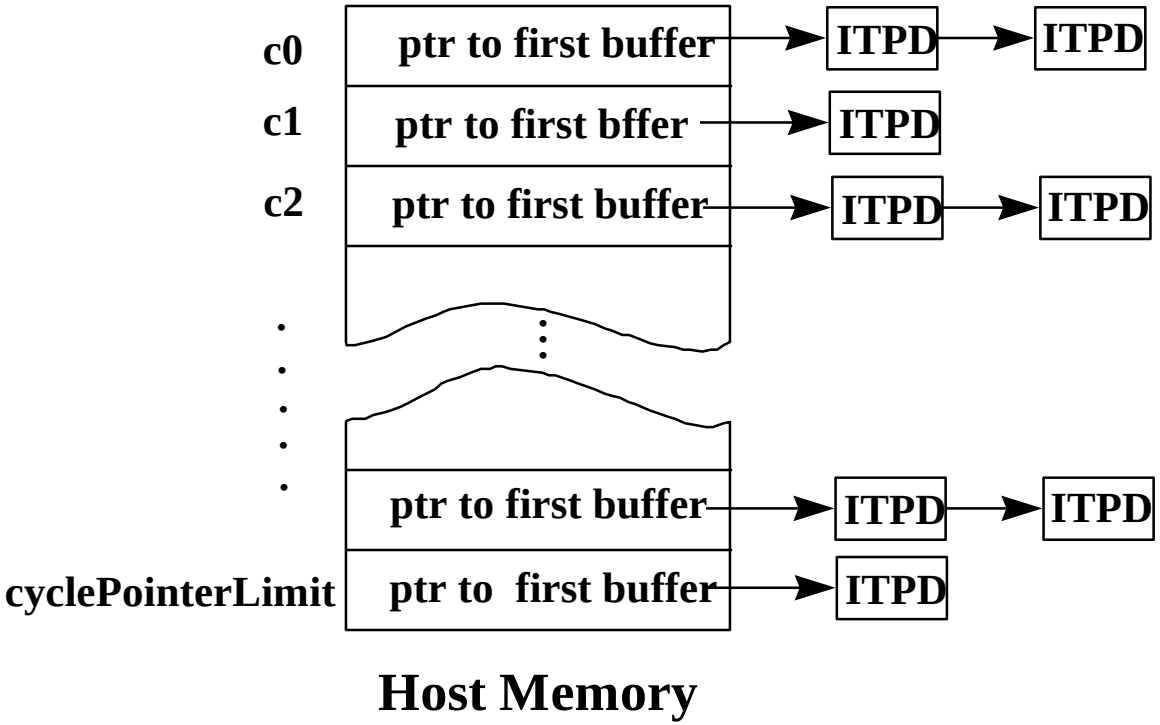
IEEE 1394-1995
6.2.3.1

Isochronous Transmit DMA

- Open HCI has 1 DMA context for Isochronous Transmit.
- Used to transmit data on multiple isochronous channels.

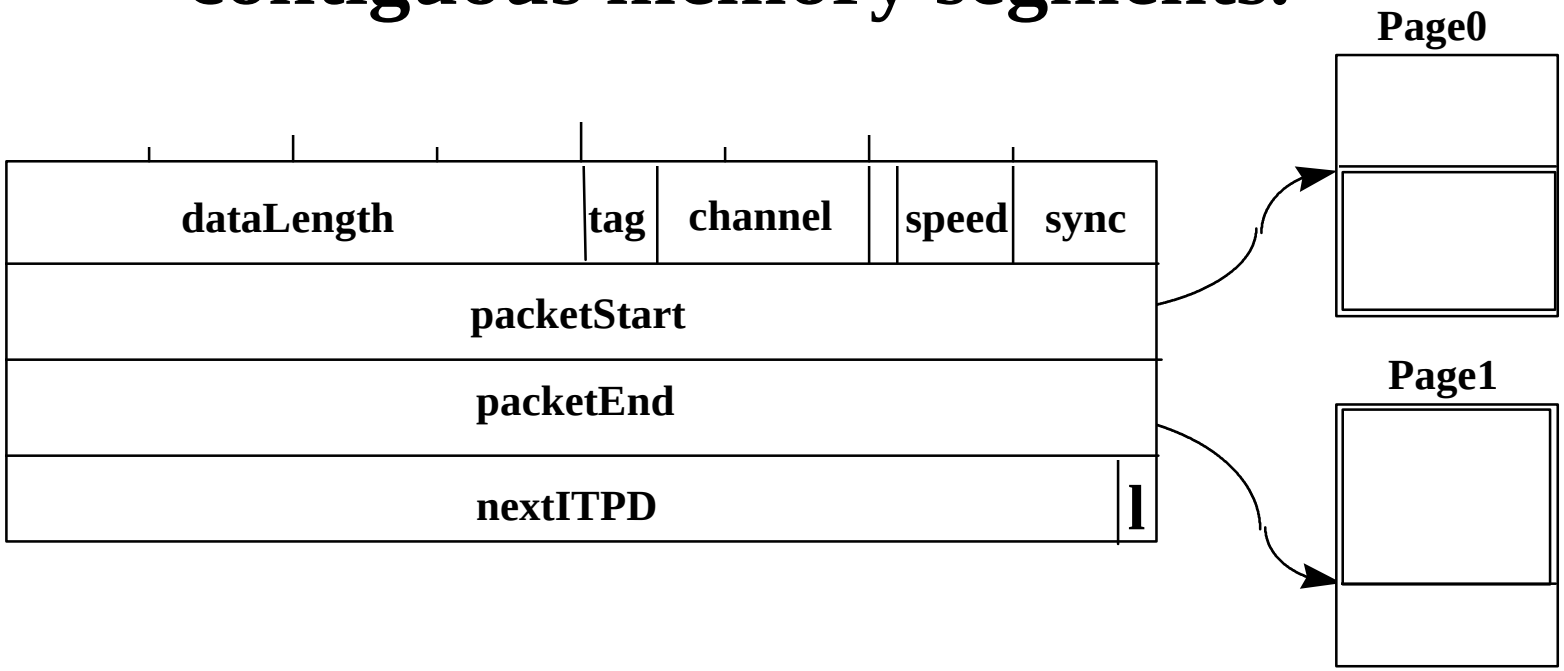
Isochronous Transmit Array

- Each array element points to a list of data buffers to be transmitted during a cycle.



Isochronous Transmit Packet Descriptor

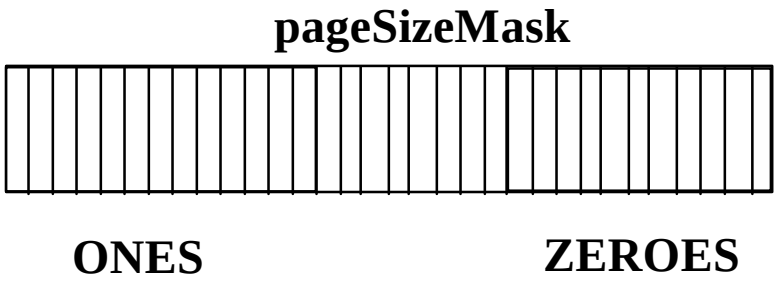
- The ITPD can specify a <u>virtually contiguous</u> buffer consisting of 2 contiguous memory segments.



Page Size

- **The page size register is used with the ITPD packetStart and packetEnd fields to determine the size of the memory segment within each page.**

Isochronous Transmit Page Size register



Isochronous Transmit