1394 OpenHCI DB DMA Part I

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Background
(What is DBDMA?)

- Scatter/Gather DMA System
- Based on buffer descriptor* lists resident in memory
- Linked lists can be created too.

*For this presentation, “descriptor” and “command” are synonymous

DB DMA Descriptor Format

<table>
<tr><td>4</td><td>1</td><td>3</td><td>2</td><td>2</td><td>2</td><td>2</td><td>16</td></tr>
<tr><td>cmd</td><td>s</td><td>key</td><td>r</td><td>i</td><td>b</td><td>w</td><td>reqCount</td></tr>
<tr><td colspan="8">address</td></tr>
<tr><td colspan="8">Immediate data OR Branch Address</td></tr>
<tr><td colspan="7">xferStatus</td><td>resCount</td></tr>
</table>

- **4-bit “Cmd” field**
- **“No Status” (s) bit**
- **Data “key” stream field**
- **Condition fields**
- **Requested Count field**
- **Source/Destination address**
- **Immediate data OR Branch address field**
- **Status result of descriptor**
- **Residual count field**

DBDMA “Cmd” Field

- **Command field encodings:**

value	name	description
0	OUTPUT_MORE	transfer more memory-to-stream
1	OUTPUT_LAST	transfer last memory-to-stream
2	INPUT_MORE	transfer more stream-to-memory
3	INPUT_LAST	transfer last stream-to-memory
4	STORE_QUAD	store immediate 4-byte value
5	LOAD_QUAD	load immediate 4-byte value
6	NOP	no data transfer
7	STOP	suspend command processing
8-15	-	reserved

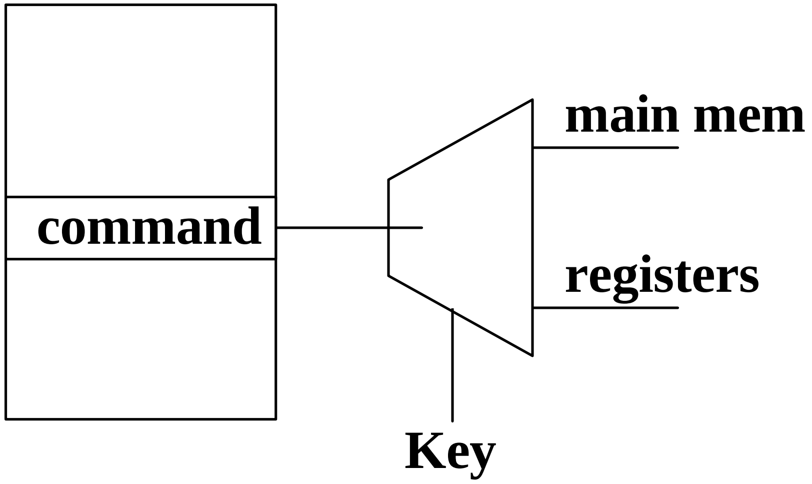
“No Status” Field

- Set to a ‘1’ indicates that the xferStatus and resCount fields should NOT be updated at the completion of the command
- Setting to ‘0’ allows the post-completion parsing of the entire Command List (CL)
- ‘1’ saves memory transactions and possibly unnecessary status updates (like NOPs without branches, and initial Load/Store command status)

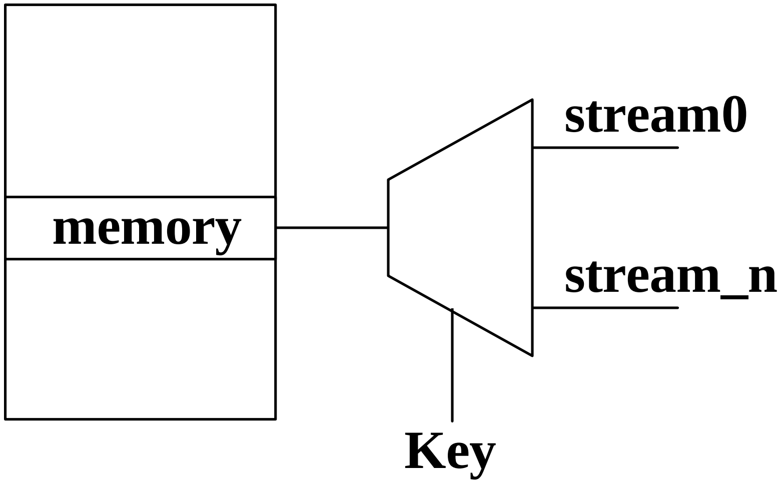
Data “key” Stream Field

- Data router picks source of data for Load and Input commands
- Picks destination of data for Store command

Load and Store “streams”



Input & Output streams



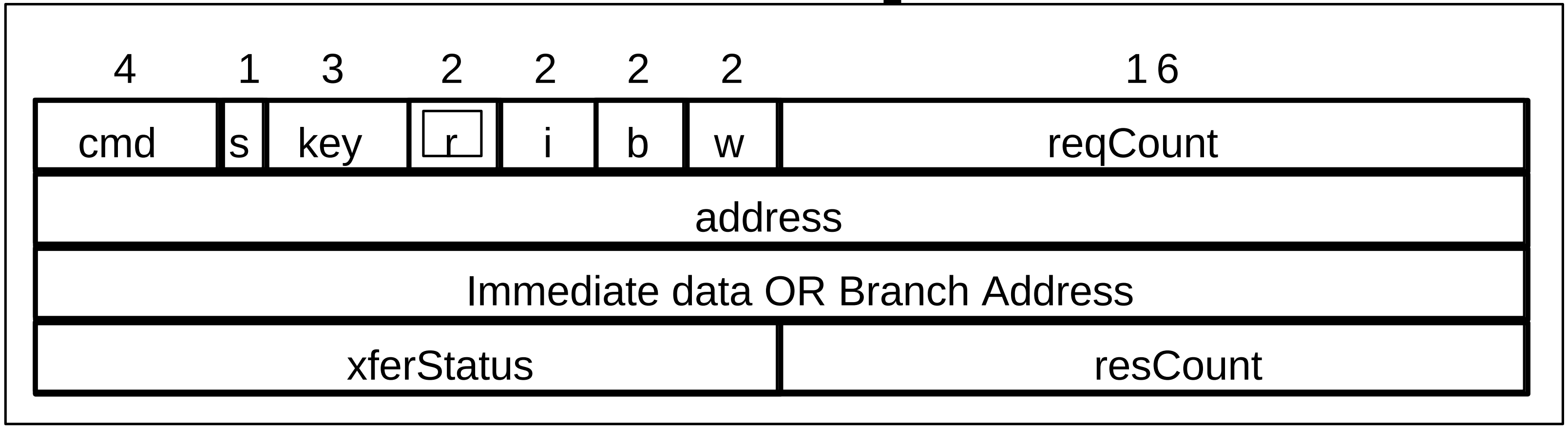
Interrupt, Branch, Wait Fields

- **Encodings:**

Command.i	**condition**
0	never True
1	*True if condition bit is ‘1’*
2	*True if condition bit is ‘0’*
3	always True

c = ((ChannelStatus.s7..s0 & ConditionSelect.mask) = = (ConditionSelect.value & ConditionSelect.mask))

DB DMA Descriptor Format



4	1	3	2	2	2	2	16
cmd	s	key	r	i	b	w	reqCount
address							
Immediate data OR Branch Address							
xferStatus							resCount

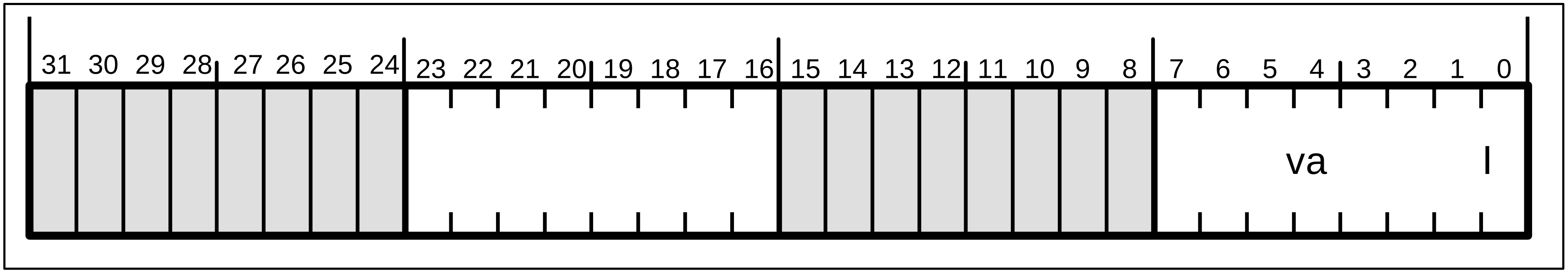
- 4-bit “Cmd” field
- “No Status” (s) bit
- Data “key” stream field
- Condition fields
- Requested Count field
- Source/Destination address
- Immediate data OR Branch address field
- Status result of descriptor
- Residual count field

More on Int, Br, and Wait

- **First, the command finishes the requested transfer OR the command ends prematurely.**
- **Then, the Wait condition is evaluated, and if necessary, command execution waits.**
- **After the Wait condition is satisfied, the Interrupt and Branch conditions are checked and issued accordingly.**
- **At this point any Status writeback would occur if the S bit was 0.**

Condition Select and Mask Registers

- Mask register indicates which bits are to be checked.
- Select register selects the actual value that the masked bit should compared to.



Requested Count Field

- **Contains a value from 0 to 65,535.**
- **Input and Output commands complete "successfully" when this count is met.**

Source/Destination Data Address

- This is the memory location where Input commands will send the data to.
- This is the memory location where Output commands will get the data from.
- For Load and Store commands this field may represent a register address (depending on the keyStream value).

Immediate Data OR Branch Address Field

- **For Input, Output, and NOP commands this field is the conditional Branch address.**
- **For Store commands this field is 32-bit data to be written to the address specified in the Address field.**
- **For Load commands this field is the 32-bit location for data FROM the address pointed to by the Address field.**

Transfer Status Field

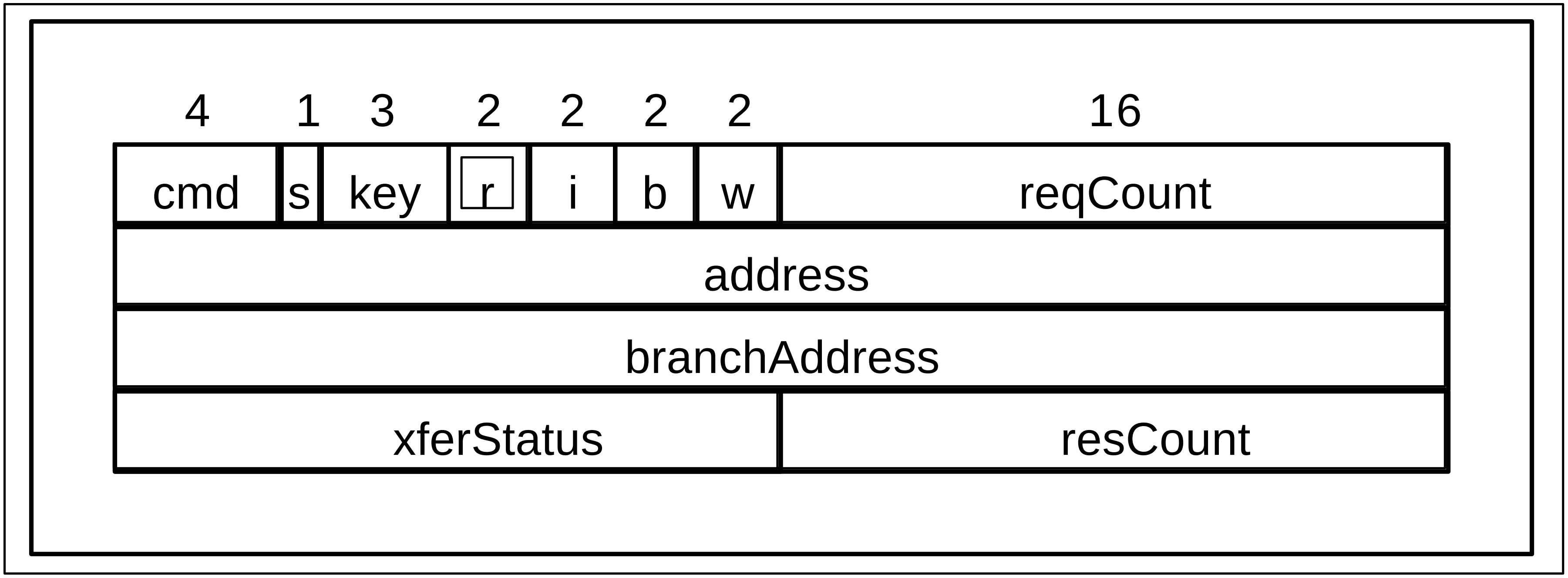
- Upon conclusion of the command, and if the S bit in the command is 0, this field is written with the lower 16 bits of the Status register.

Residual Count Field

- **Upon execution of the command, and if the S bit in the command is 0, this field is written with the difference between the number of bytes which were transferred and the original amount in the reqCount field.**
- **resCount = reqCount - ActualXfer.**

Input & Output Commands

- **THE DMA data-mover instructions**



4	1	3	2	2	2	2	16
cmd	s	key	r	i	b	w	reqCount
address							
branchAddress							
xferStatus							resCount

Input & Output, con’t

- _More option
  - Scatter/gather pieces of a larger transfer
- _Last option
  - Expected to be the last bytes of a packet

Load & Store Commands

- **Used for moving “immediate” data - mainly for reading/writing registers**

4	1	3	2	2	2	2	16
cmd	s	key	r	i	r	w	reserved
Source/Dest address							
“immediate” data32							
xferStatus							reserved

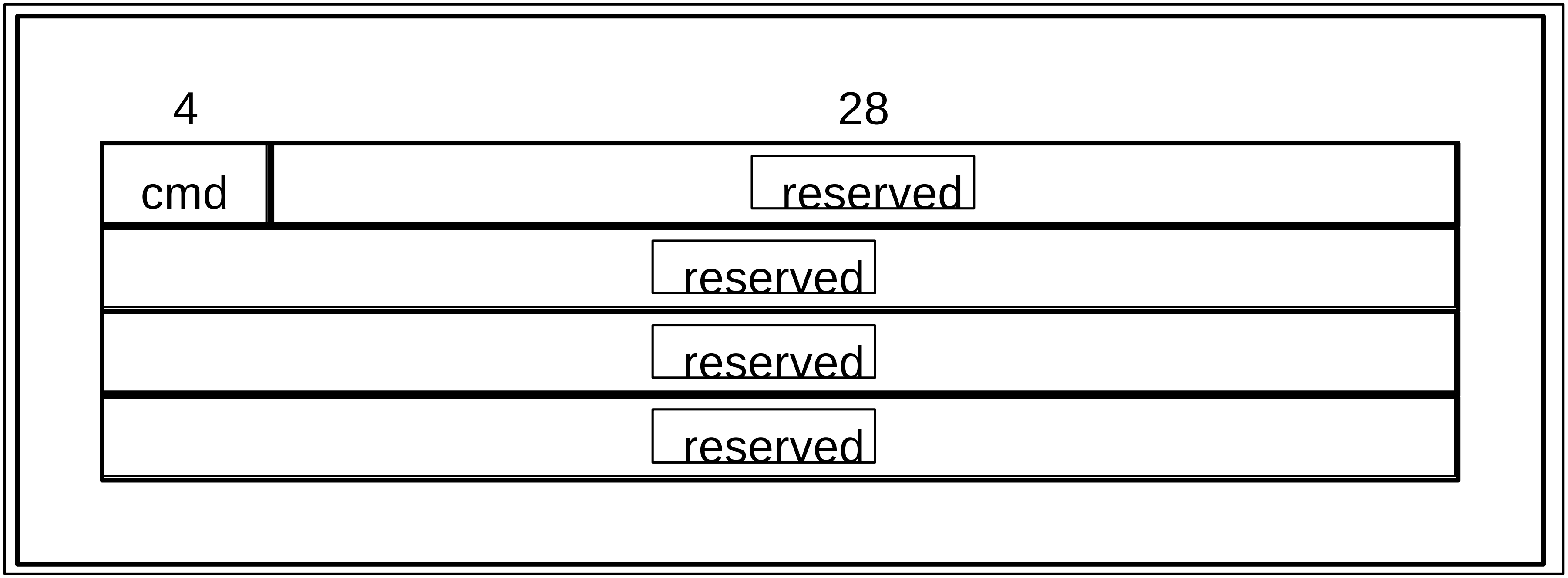
NOP Command

- **Useful for condition-testing as well as nullifying descriptors**

<table>
<tr><th>4</th><th>1</th><th>5</th><th>2</th><th>2</th><th>2</th><th>16</th></tr>
<tr><td>cmd</td><td>s</td><td>reserved</td><td>i</td><td>b</td><td>w</td><td>reserved</td></tr>
<tr><td colspan="7">reserved</td></tr>
<tr><td colspan="7">branchAddress</td></tr>
<tr><td colspan="6">xferStatus</td><td>reserved</td></tr>
</table>

Stop Command

- Last descriptor in the command list
- No Interrupt, Branch or Wait conditions
- CommandPtr left pointing to this location



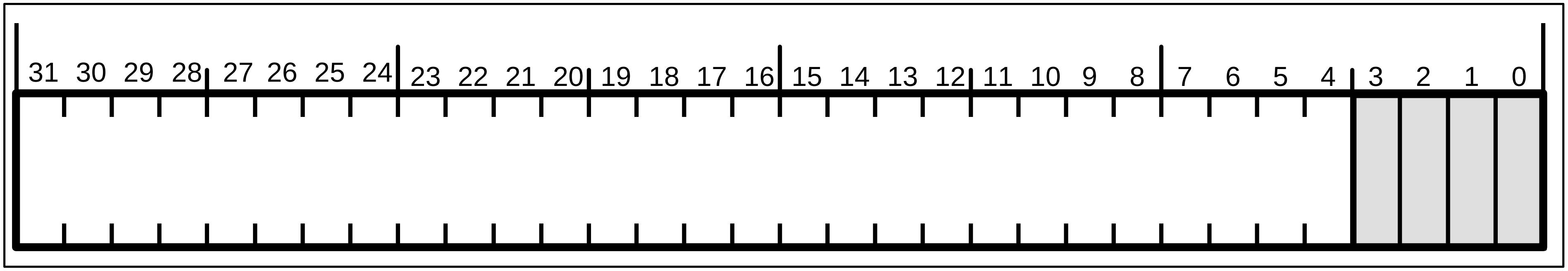
<table>
<tr><th>4</th><th>28</th></tr>
<tr><td>cmd</td><td>reserved</td></tr>
<tr><td colspan="2">reserved</td></tr>
<tr><td colspan="2">reserved</td></tr>
<tr><td colspan="2">reserved</td></tr>
</table>

Building Command Lists

- Write contiguous command list, zeroing xferStatus and resCount fields for later viewing.
- Always end with a STOP command

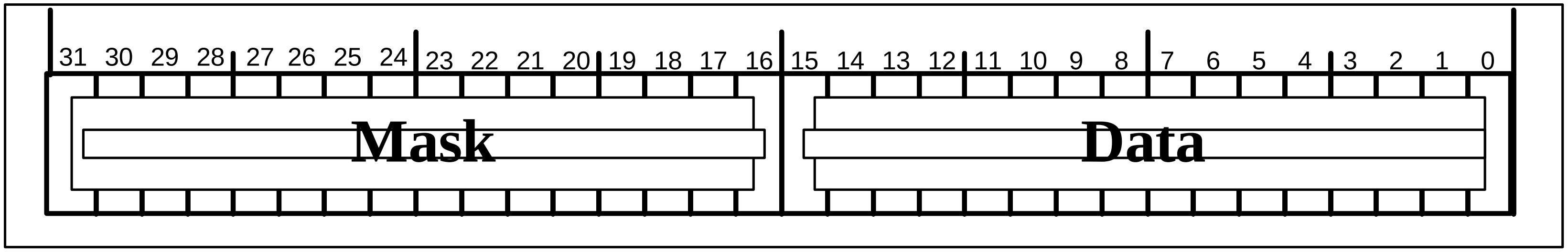
CommandPtr register

- Points to current CL location (beginning)
- 16-byte aligned
- Remains pointing at STOP command after STOP completes

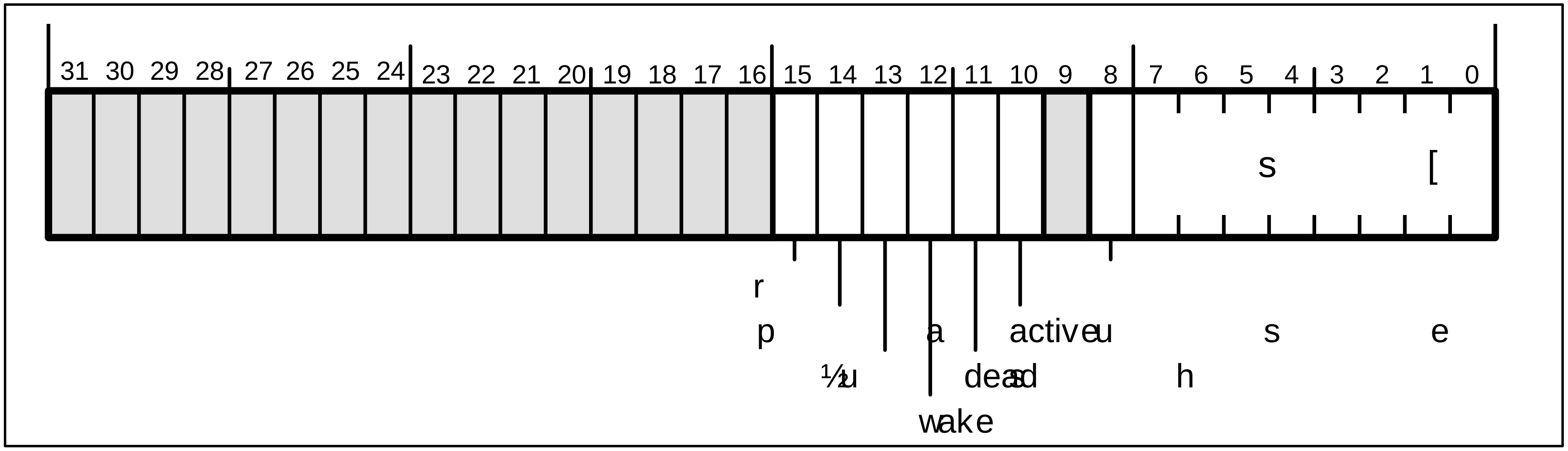


Channel Status and Control regs

- ## ChannelControl register



- ## ChannelStatus register



Writing the ChannelControl Register

- Put ‘1’s in Mask bits which correspond to bits to be written.
- Put the value of the bits to be written in the Value bits.
- Do this all as an autonomous 4-byte write.

ChannelStatus Details

- <u>Control bits</u>: set and cleared by software
  - Run enables CL execution
  - Pause, well, it pauses!!
- <u>Command bits</u>: set by software, cleared by hardware
  - Flush bit is used in conjunction with Pause to clear out all internal buffers/FIFOs.
  - Wake bit cause DBDMA state machines to refetch current command.
- <u>Status bits</u>: set by hardware, cleared by hardware
  - Dead indicates an internal error
  - Active is set when Run bit is true. Cleared when Pause or Dead are set, or when STOP encountered

Starting the Command List

- **Write the CommandPtr register with the address of the CL.**
- **Set up any conditions necessary for the CL (like an interrupt on the last command).**
- **Write the ChannelControl register with the Run bit set and the Pause bit cleared.**

Re-starting the Command List

- Start by setting up new CL in memory, then
  - Method 1:
    - Change the CommandPtr to point to new CL
  - Method 2:
    - Change STOP command to Branch command which has a pointer to new CL.
- Finally: Set the Wake bit.

Command List Example

	cmd	key	i	b	w	reqCount	address
0	OUTPUT_MORE	STREAM0	NEVER	NEVER	NEVER	100	&Hdr1
1	OUTPUT_LAST	STREAM0	NEVER	NEVER	NEVER		&Buf1
2		STREAM1		NEVER	NEVER	4	
3	OUTPUT_MORE	STREAM0	NEVER	NEVER	NEVER	100	&Hdr2
4	OUTPUT_LAST	STREAM0	NEVER	NEVER	NEVER		&Buf2
5	INPUT_LAST	STREAM1	ALWAYS	NEVER	NEVER	4	&Status2
6	STOP->NOP	NA	NA	NA	NA	NA	NA
7	OUTPUT_MORE	STREAM0	NEVER	NEVER	NEVER	100	&Hdr2
8	OUTPUT_LAST	STREAM0	NEVER	NEVER	NEVER		&Buf2
9		STREAM1		NEVER	NEVER	4	
				NA			
	-	-	-	-	-	-	-

Any Questions?