Software Considerations

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OpenHCI

An overview of the design from the driver writer's point of view

Agenda

- **What is OpenHCI?**
- **Initialization**
- **Asynchronous Transmit Example**
- **Asynchronous Receive**

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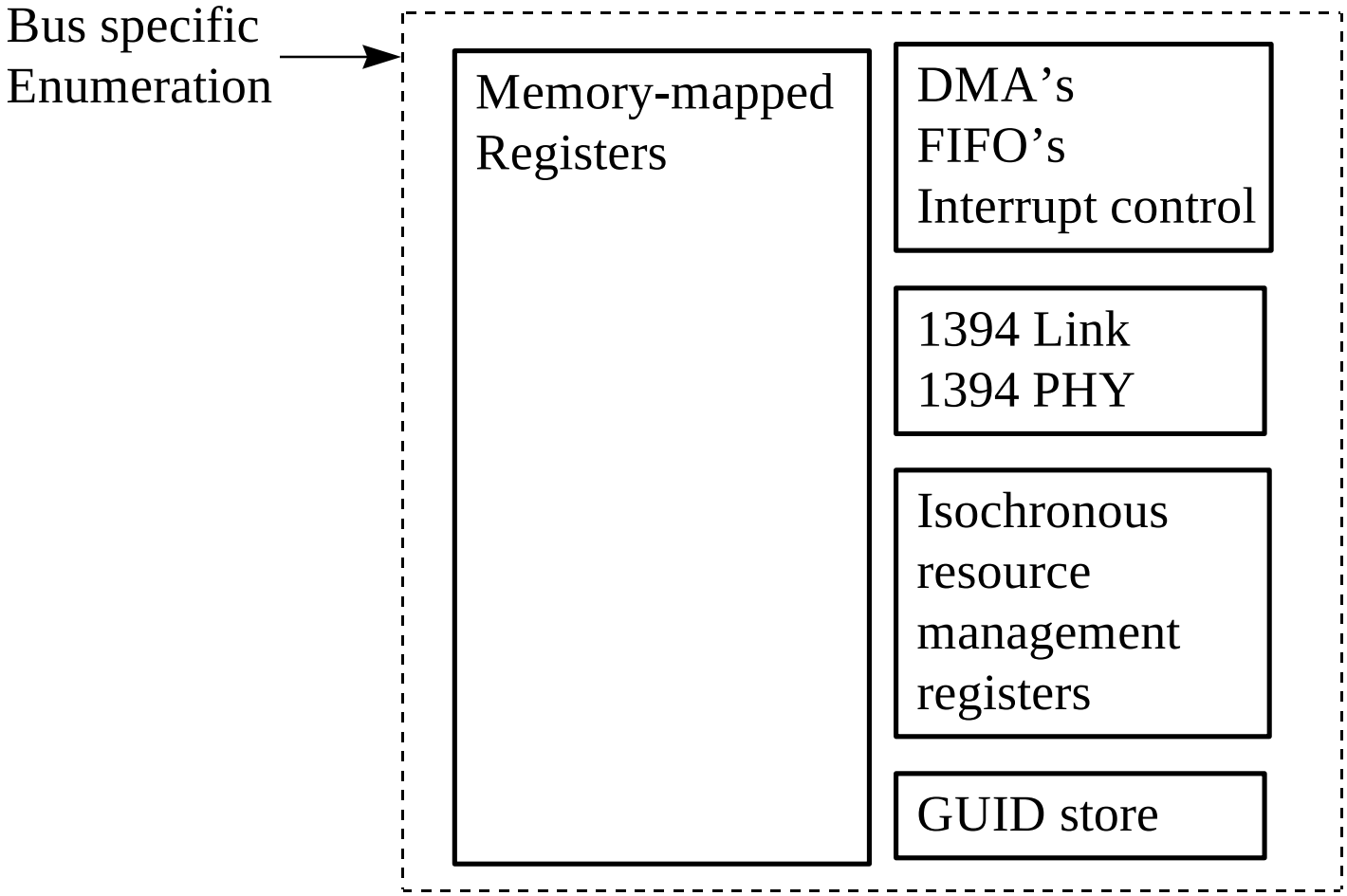
What's in OpenHCI?



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PCI Specific Parts

BAR0
Base Class
Sub Class
Programming Interface
Global Swap

Initialization

Initialization -- part 1

- Enumeration finds Host Controller
- Examine Version Register
- Issue softReset
- Find number of Iso Tx/Rx contexts
- Read HC's GUID
- Create Config ROM image and set Configuration ROM mapping register

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Initialization -- part 2

- **Initialize more registers:**
  - **Config ROM header & Bus Options**
  - **ATRetries**
  - **LinkControl**
  - **IntEvent, isoXmitIntEvent, & isoRecvIntEvent (clear all)**
  - **IntMask, isoXmitIntMask, & isoRecvIntMask (clear all)**
  - **SelfID Buffer Pointer (if desired)**

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Initialization -- part 3

- Create Asynchronous Receive context programs and set run bits
- Initialize s/w Async Tx queues
- Clear IR Channel Mask
- Set desired IntMask
- Set HCControl.linkEnable
- Tell PHY to send a bus reset

Asynchronous Transmit Example

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Async Rq Tx -- part 1

- **Client must provide:**
  - **Destination node**
  - **Destination offset**
  - **Data length**
  - **Request type (read, write, lock)**
  - **Data (for write or lock)**
  - **Buffer (for read or lock)**

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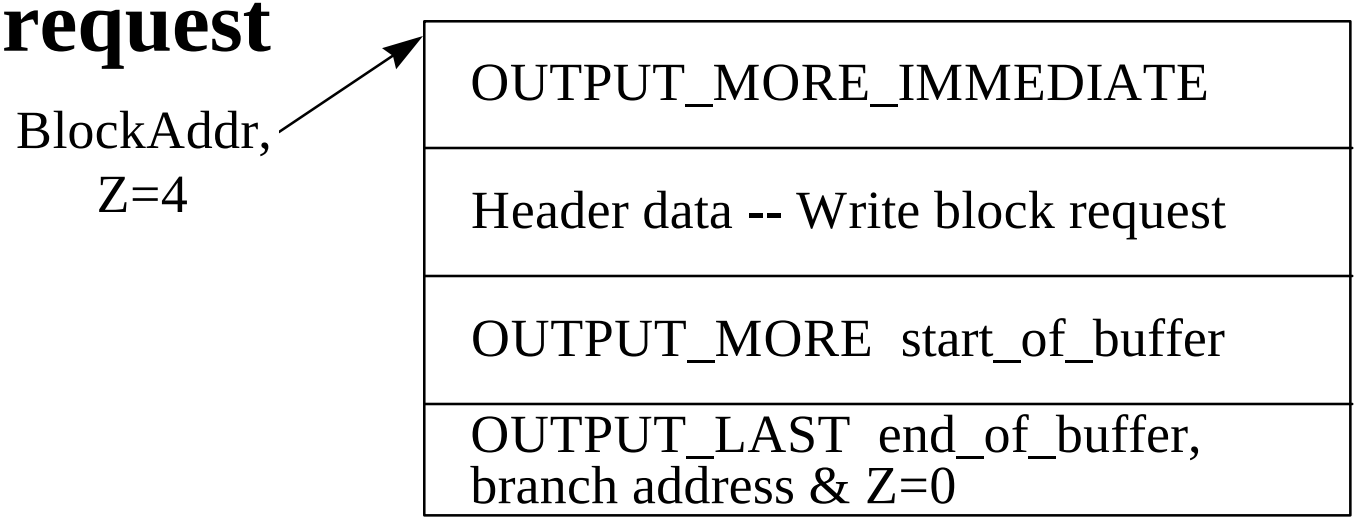
Async Rq Tx -- part 2

- **Driver must assign a tLabel for request**
- **Driver builds a Z-block to describe request**



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Async Rq Tx -- part 3

- **Append Z-block to h/w Tx queue:**

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Asynchronous Receive

1394 Node Offset Map

CSR area, Writes give ACK_PENDING
Upper address space, Writes give ACK_PENDING (use for protocols that don't tolerate lost packets)
Middle address space, Writes give ACK_COMPLETE but errors may cause packets to be lost (use for protocols like TCP/IP that tolerate lost packets).
Low address space, Writes may give either ACK_COMPLETE or ACK_PENDING depending on FIFO/error conditions (use for direct memory accesses)

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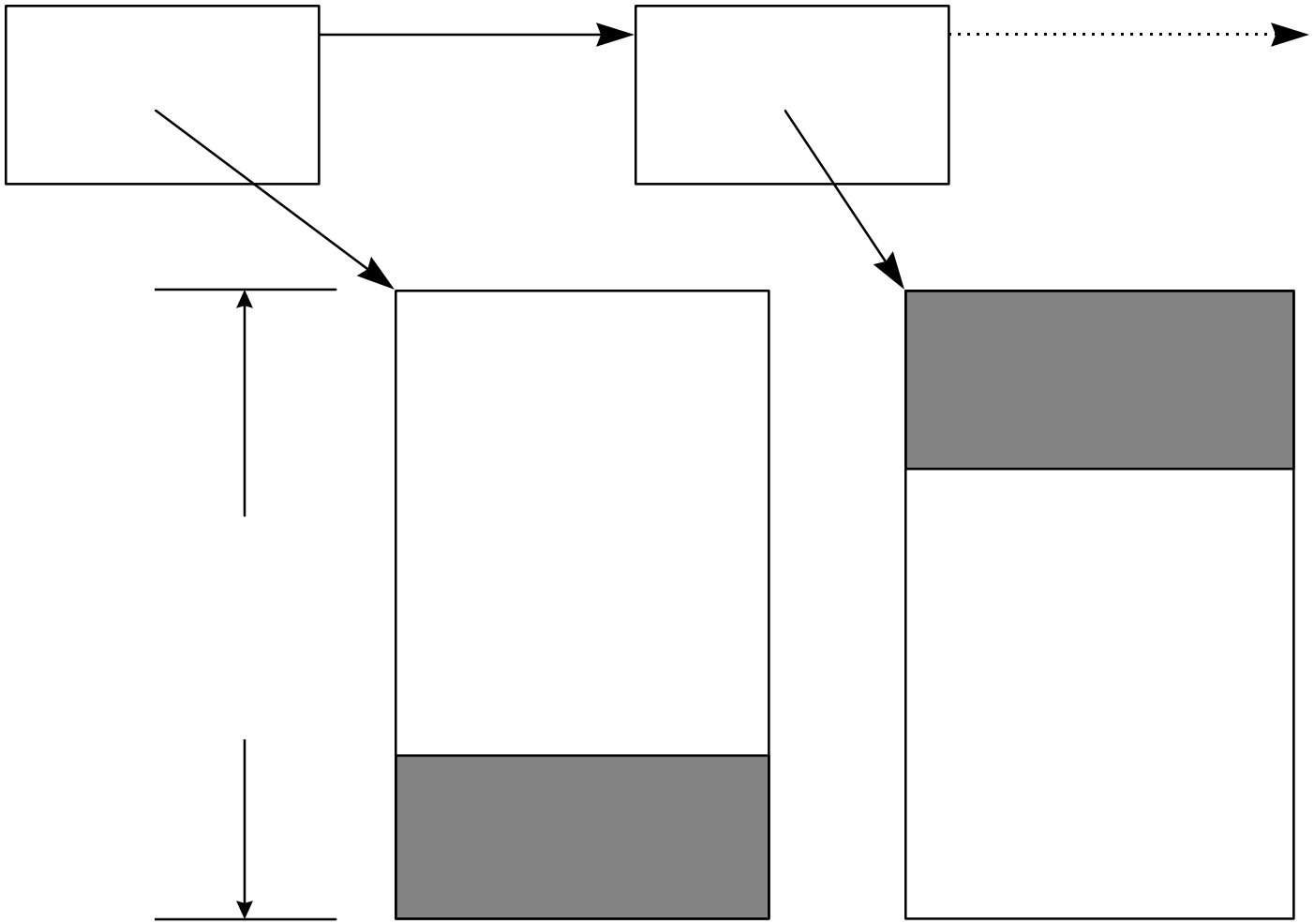
Async Receive



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Async Receive Queuing

- Append buffers to receive queue in same manner as for Async Tx
- Separate queues for Requests and Responses

Async Receive Filtering

- **Two stage filtering:**
  - **AsyncRequestFilter specifies which nodes are allowed to make requests**
  - **PhysicalRequestFilter specifies which of these nodes may directly access memory (when addressing low address space)**
- **Responses are not filtered**

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Async Tx/Rx restriction

- **Before transmitting an Async request software must ensure that space is allocated in Async Receive Response queue to receive the response**

Isochronous Operation

How Many Contexts?

- **Do during initialization:**

Questions?