



**PEN**

**1394**

# **Open Host Controller Interface**

## **Section 7**

# **Asynchronous Transmit DMA**

by

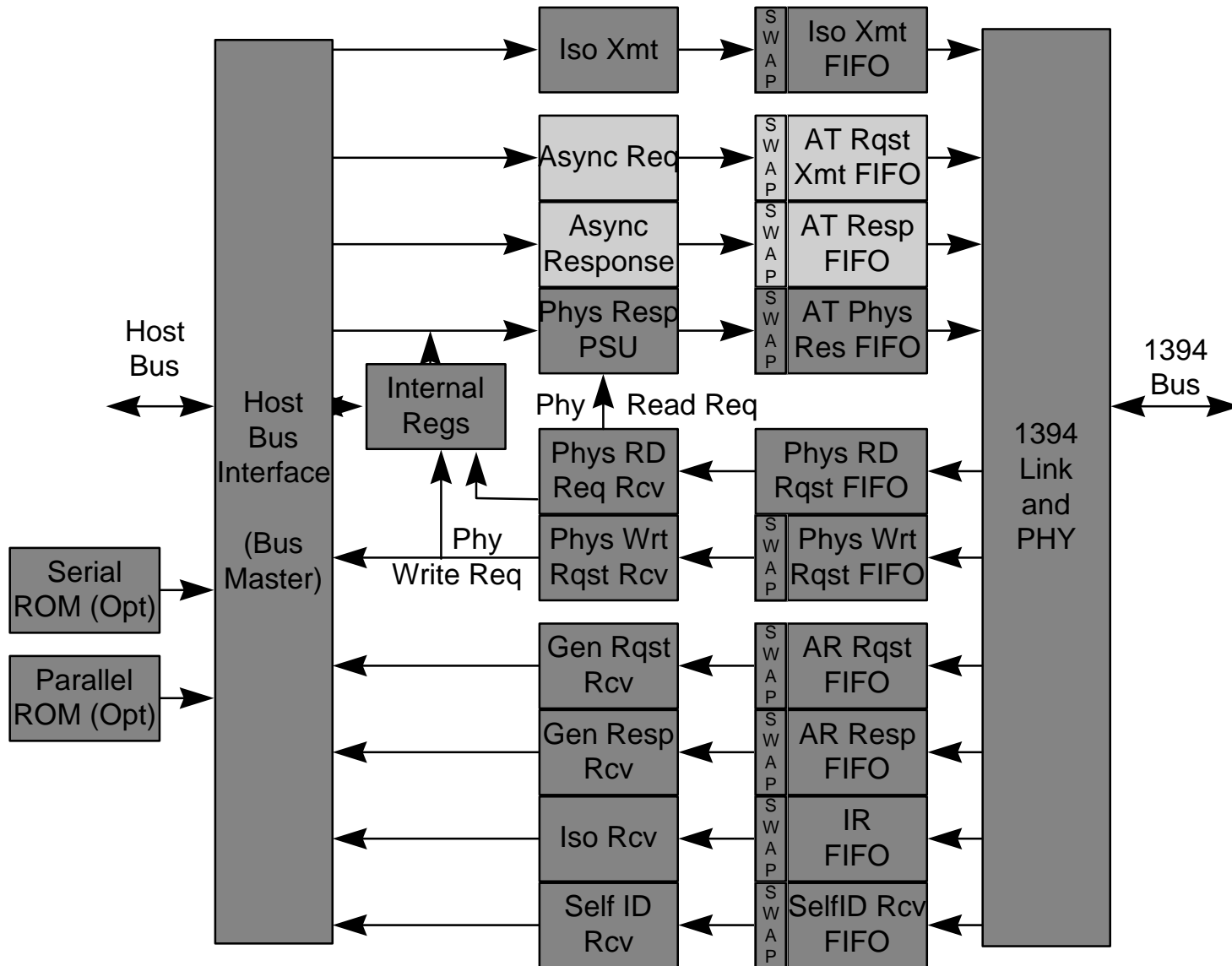
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Solectron Texas  
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# Asynchronous Transmit DMA

- ◆ **Request DMA programs**
  - **Read, Write, Lock Request**
- ◆ **Response DMA programs**
  - **Read, Write, Lock Response**
- ◆ **Physical Transmit Requests**
  - **covered in Section 12**

# OHCI Diagram





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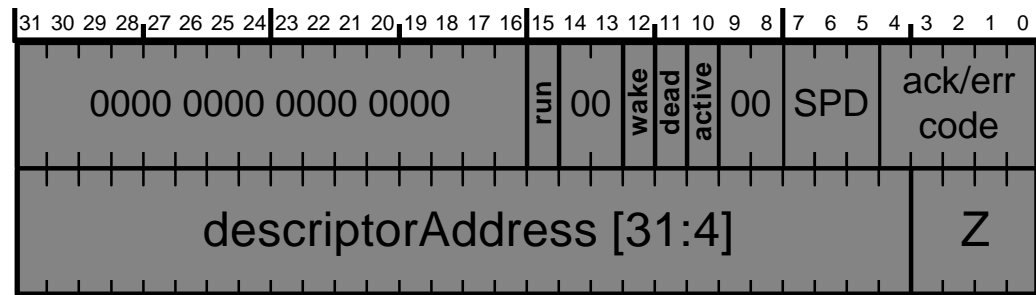
# Context Registers

## OHCI Register Address Space

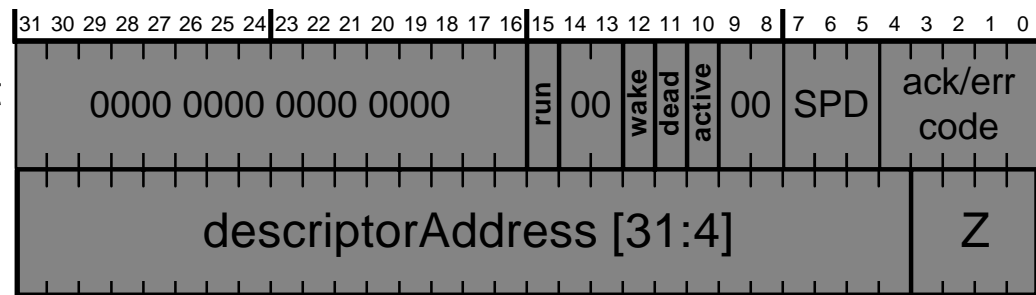
- 11'h180 ContextControlSet
- 11'h184 ContextControlClr
- 11'h188 reserved
- 11'h18C CommandPtr
  
- 11'h190 reserved
- 11'h194 reserved
- 11'h198 reserved
- 11'h19C reserved

- 11'h1A0 ContextControlSet
- 11'h1A4 ContextControlClr
- 11'h1A8 reserved
- 11'h1AC CommandPtr
  
- 11'h1B0 reserved
- 11'h1B4 reserved
- 11'h1B8 reserved
- 11'h1BC reserved

## Asynchronous Request Transmit



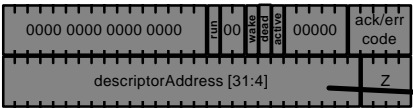
## Asynchronous Response Transmit



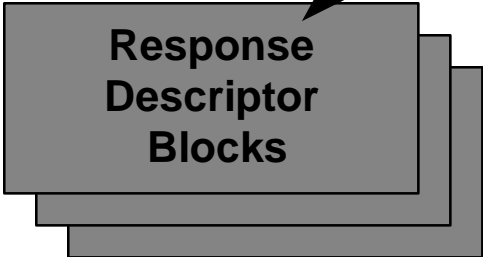
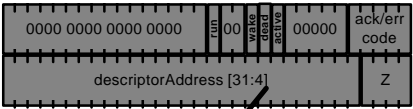
# Write Request Block

OHCI Register Space

Async Request Transmit

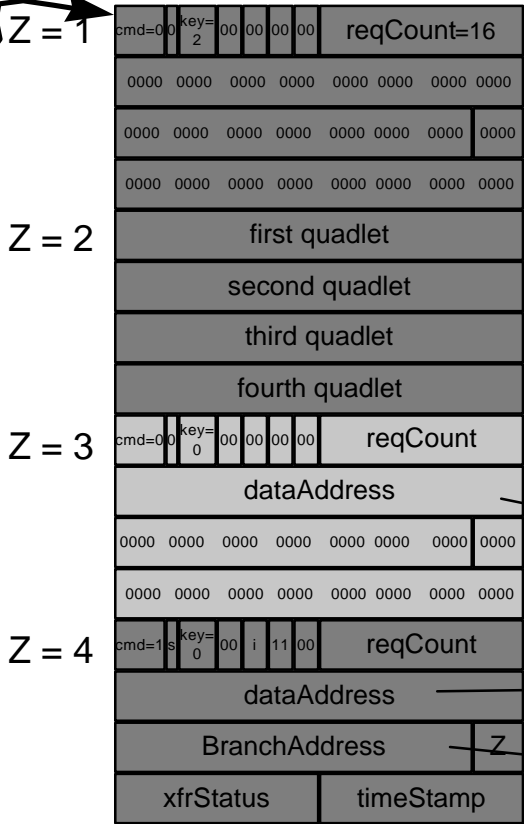


Async Response Transmit



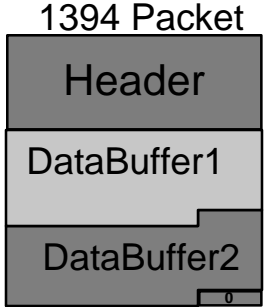
Host Memory Space

Descriptor Block



first command MUST be an output\*\_immediate

Output\_More\_Immediate



Output\_More

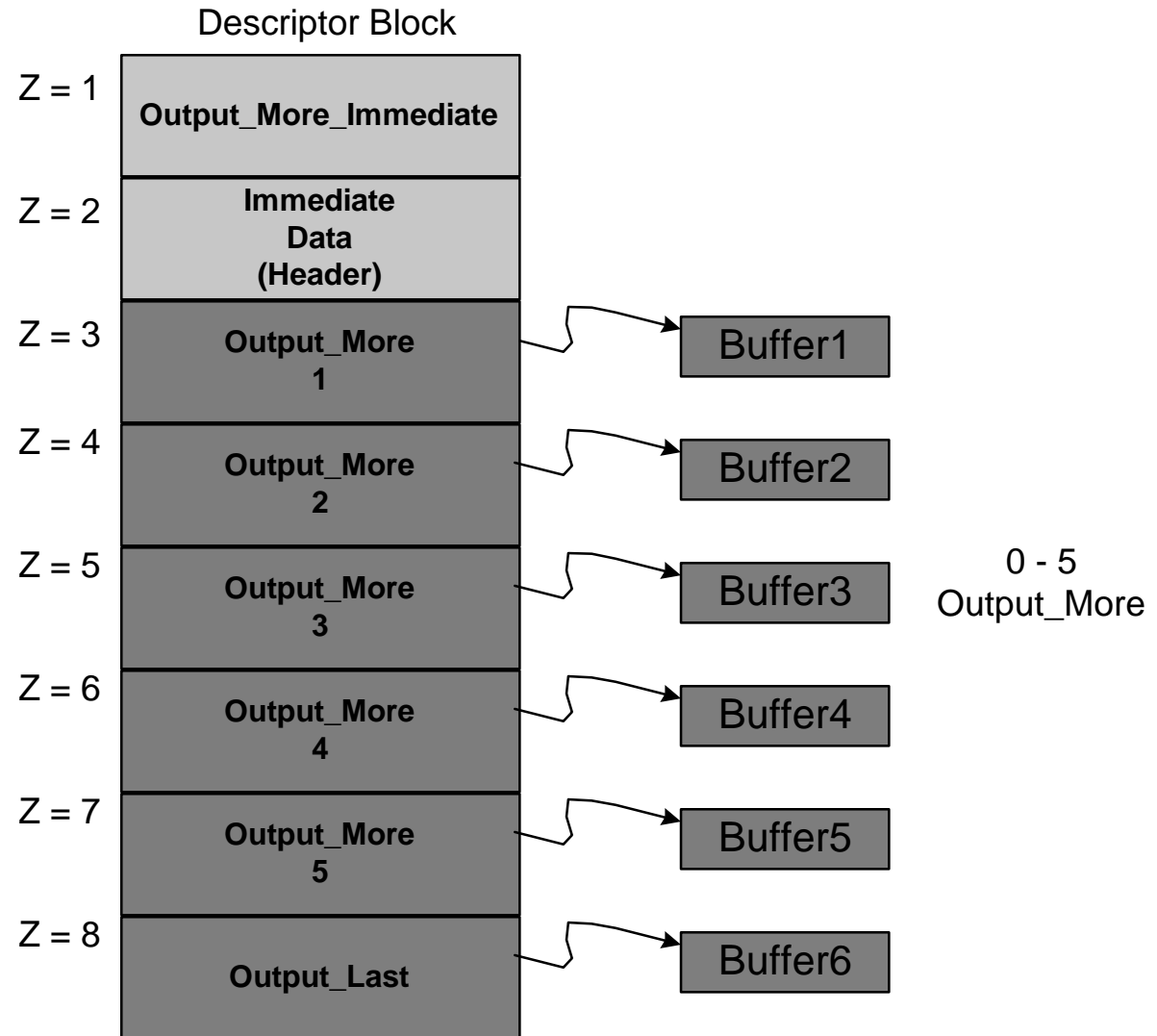


Output\_Last



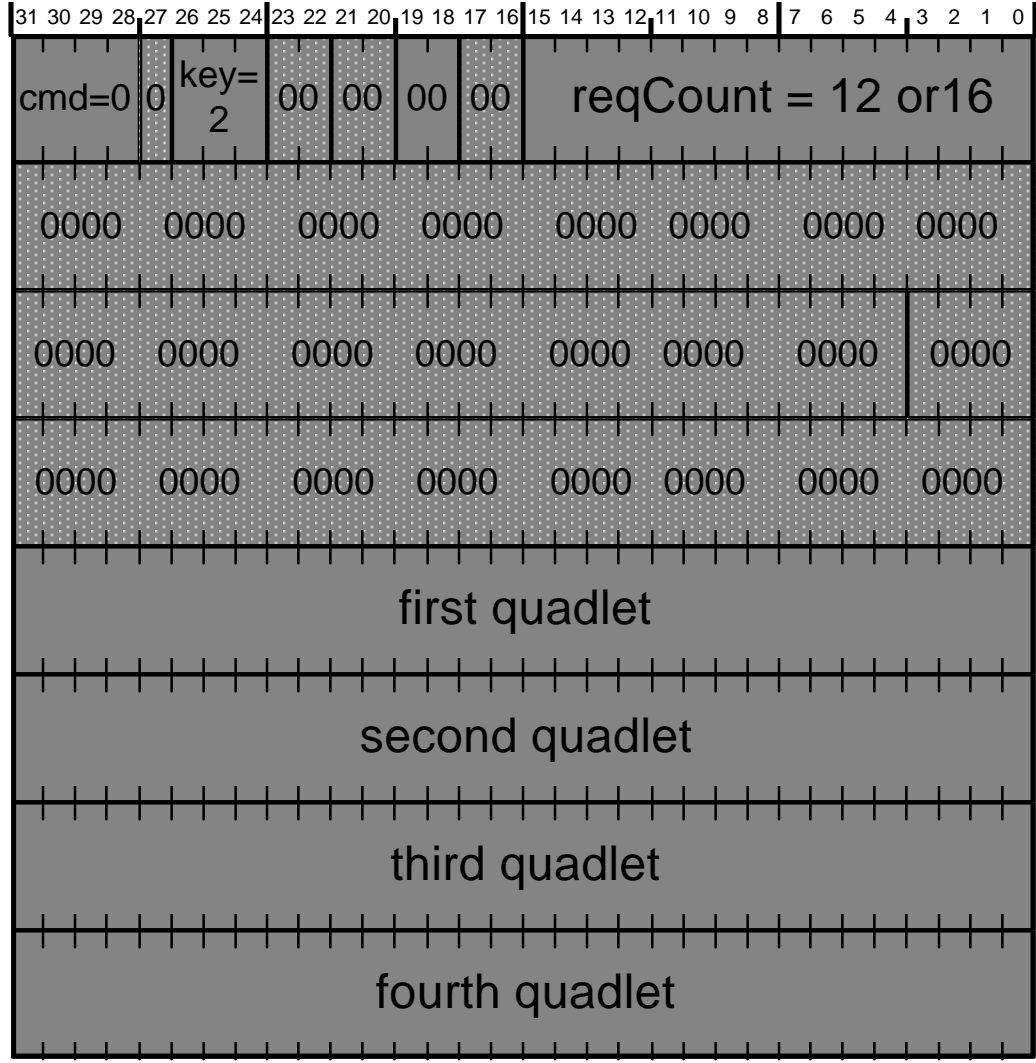
Next Descriptor Block (Z != 0)

# Descriptor Blocks



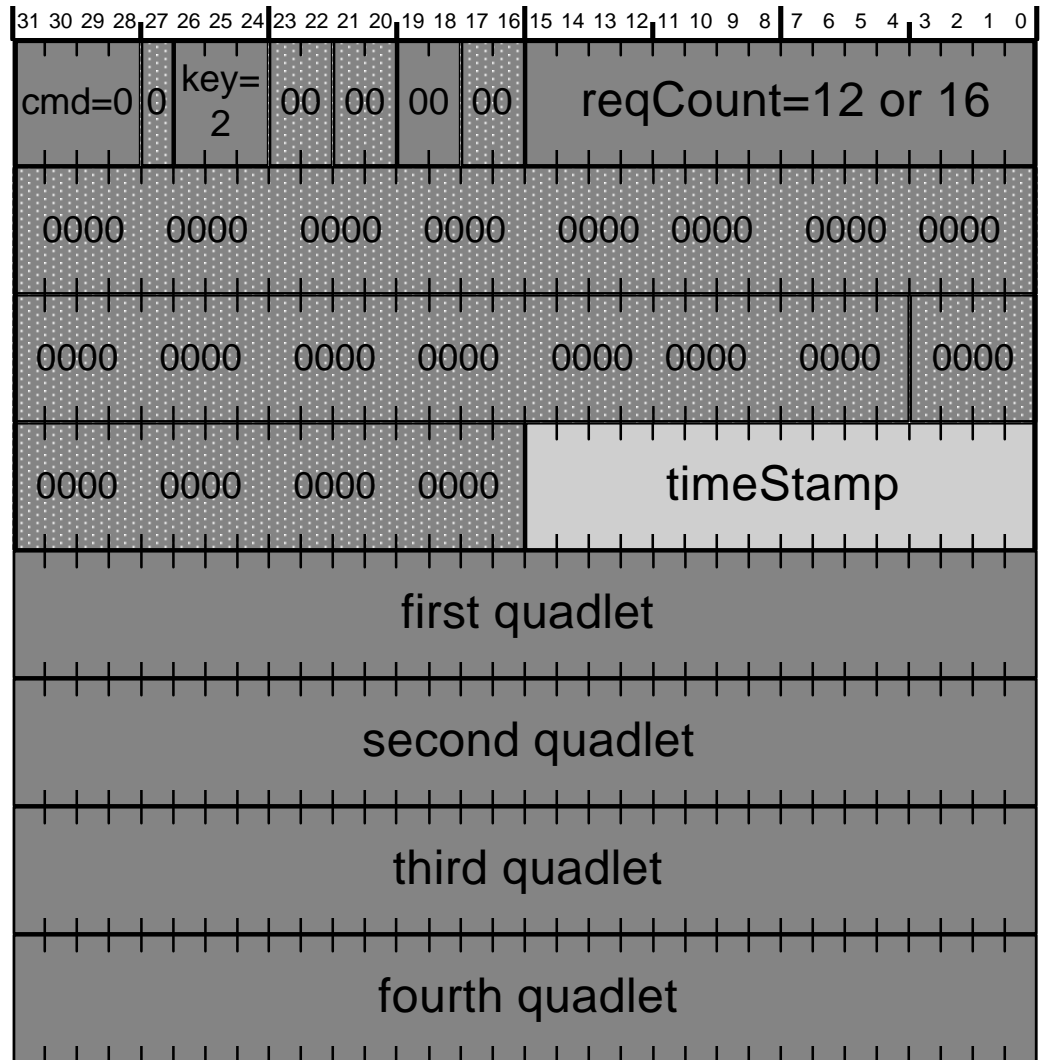


# OUTPUT\_MORE\_Immediate Request



**Header Only**

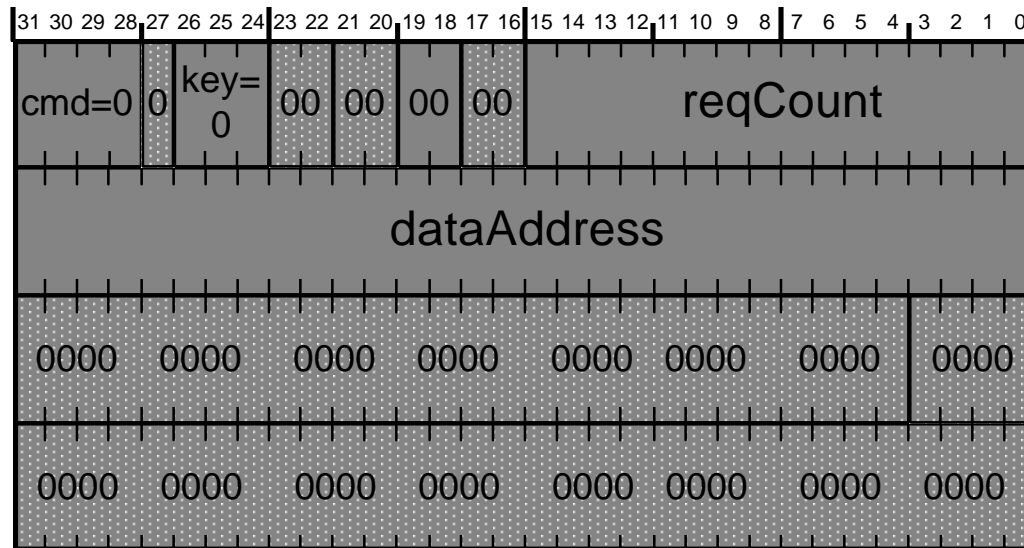
# OUTPUT\_MORE\_Immediate Response



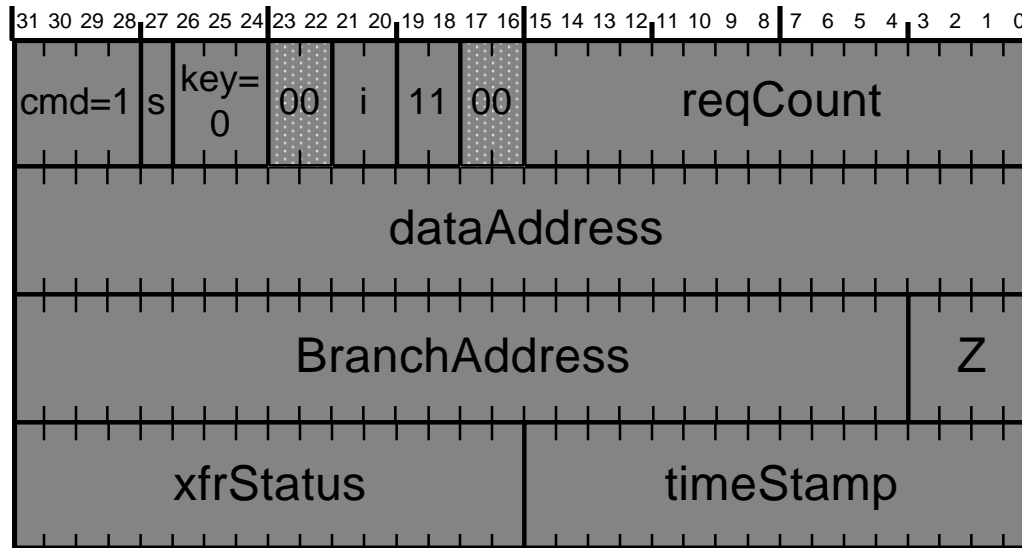
**Header Only**



# OUTPUT\_MORE

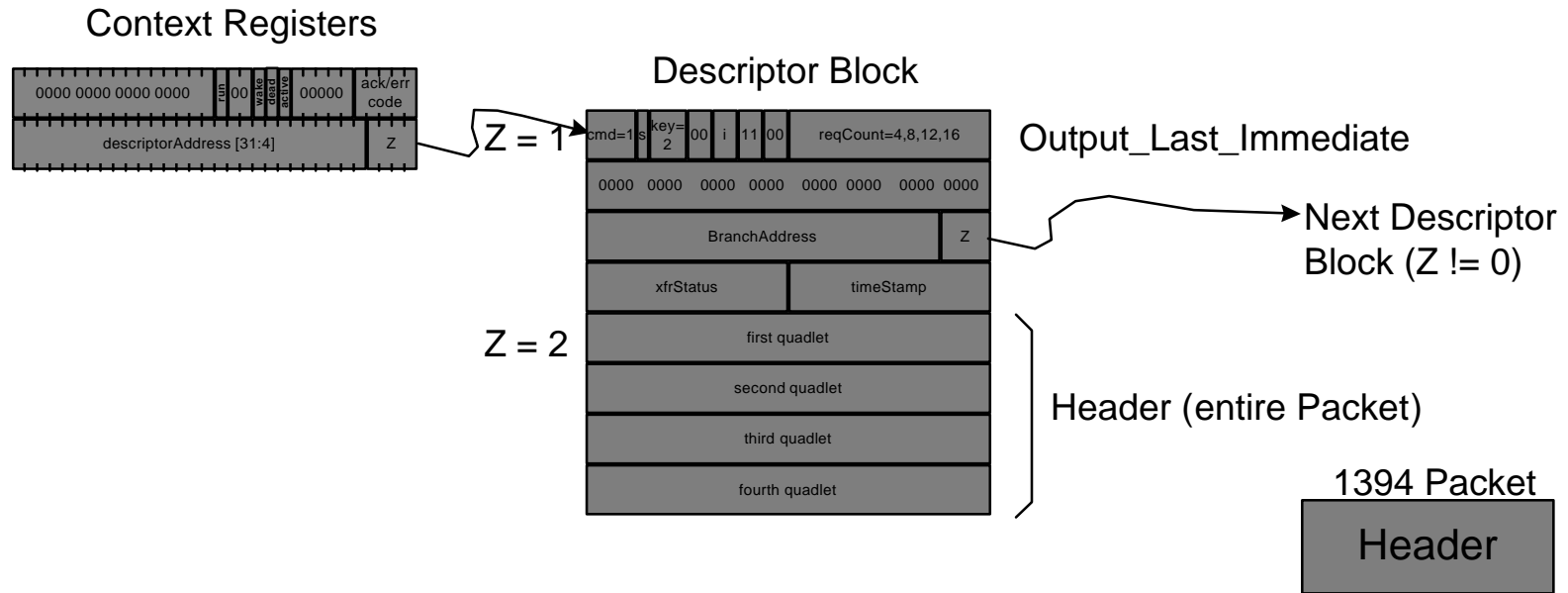


# OUTPUT\_LAST

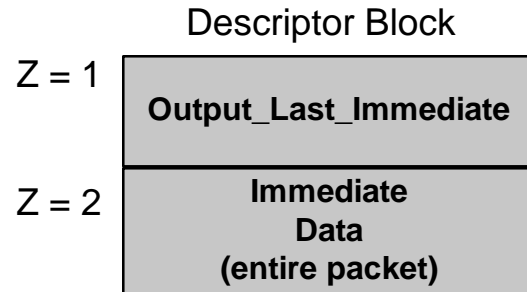




# Read Request

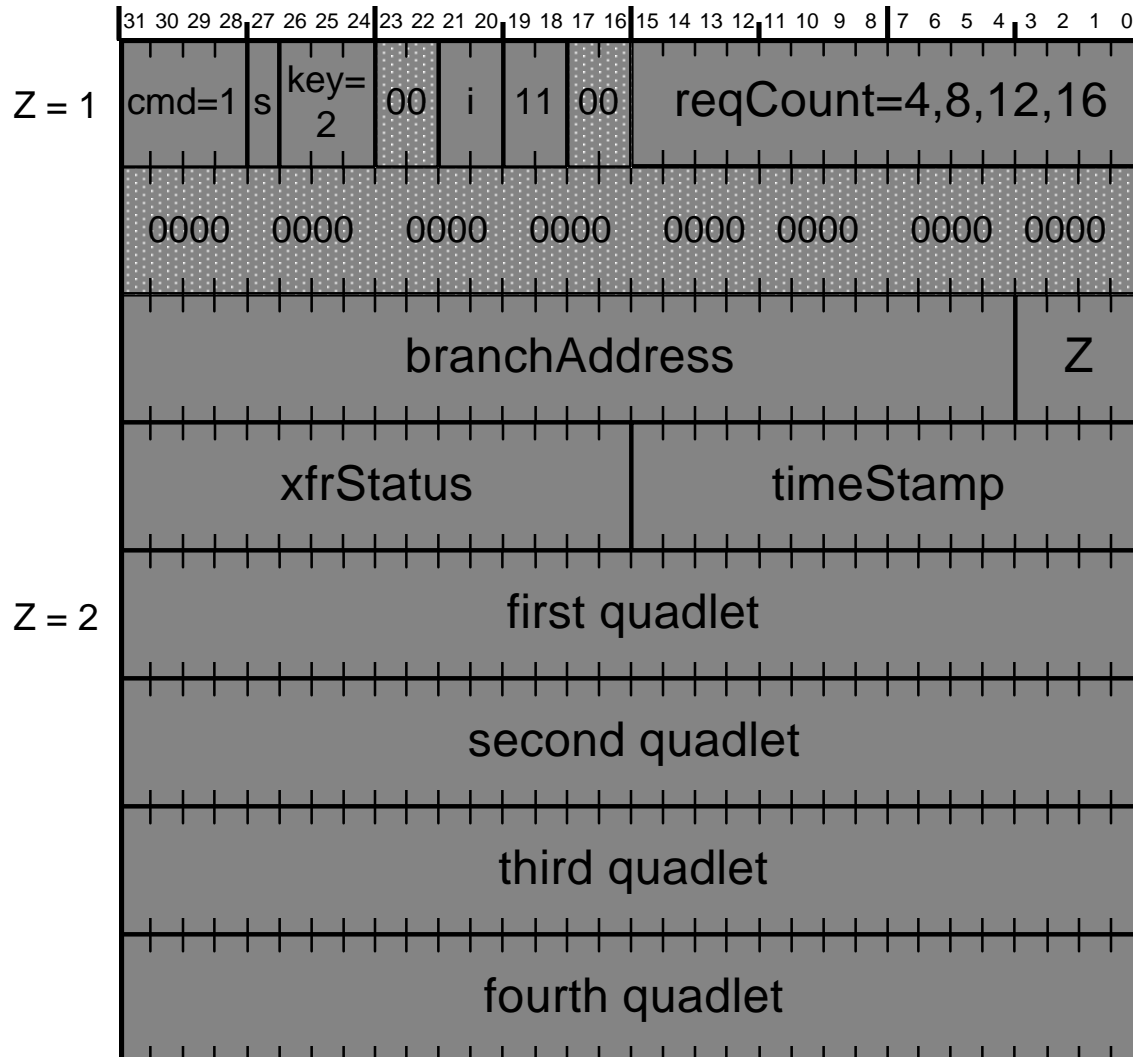


# Descriptor Blocks





# OUTPUT\_LAST\_Immediate





# Split Transaction

## ◆ Split Transaction

- responder releases bus after receiving the request
- responder ACKs the request pending
- later the responder sends the response subaction
- if fast enough, the responder may “concatenate” the response with the request
- write requests may be ACK'ed complete for a “Unified” transaction



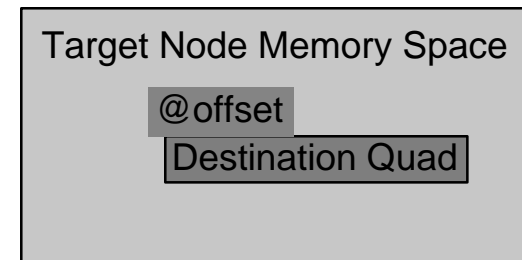
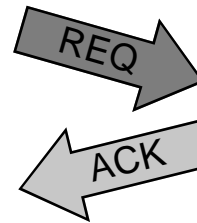
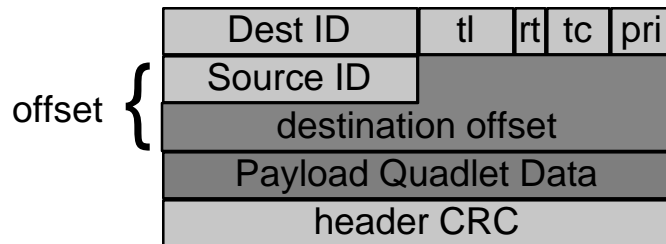
# Split Transaction Timeout

- ◆ **Both requestor and responder must keep track of how long the transaction is outstanding**
- ◆ **split transaction timeout value in 1394 CSR registers**
- ◆ **When timeout value is exceeded, both requestor and responder must terminate the transaction**

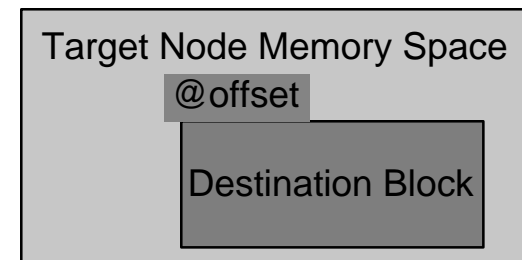
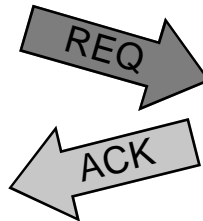
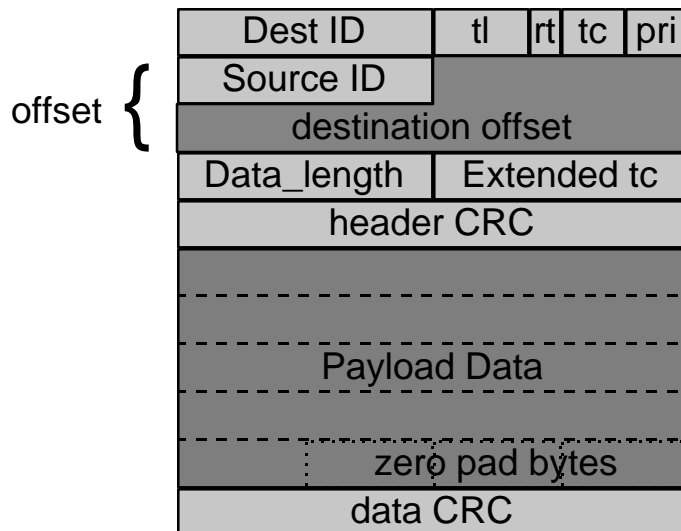
# Write Request Packets w/ ACK

(Not a split transaction)

Write Request Quadlet

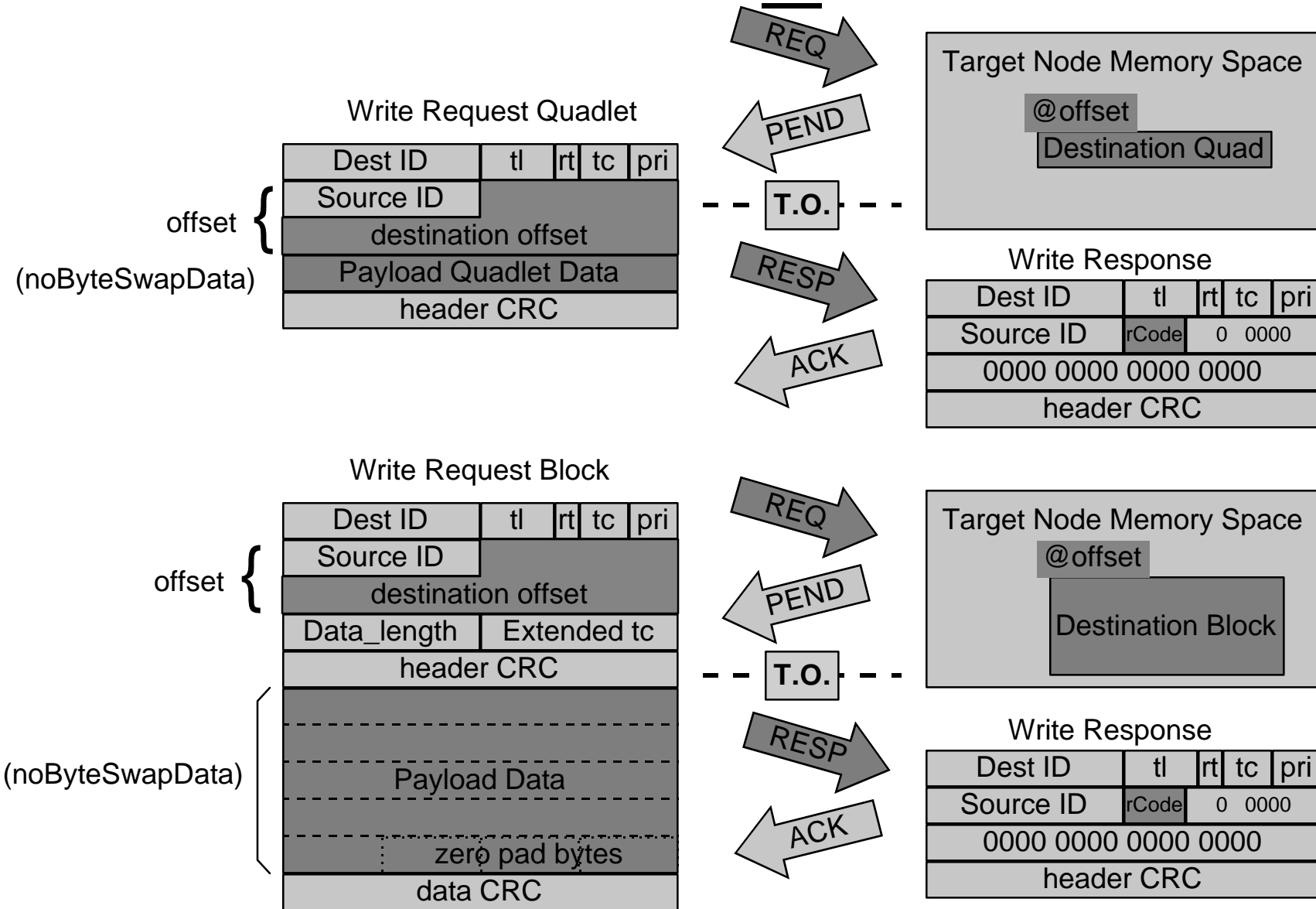


Write Request Block

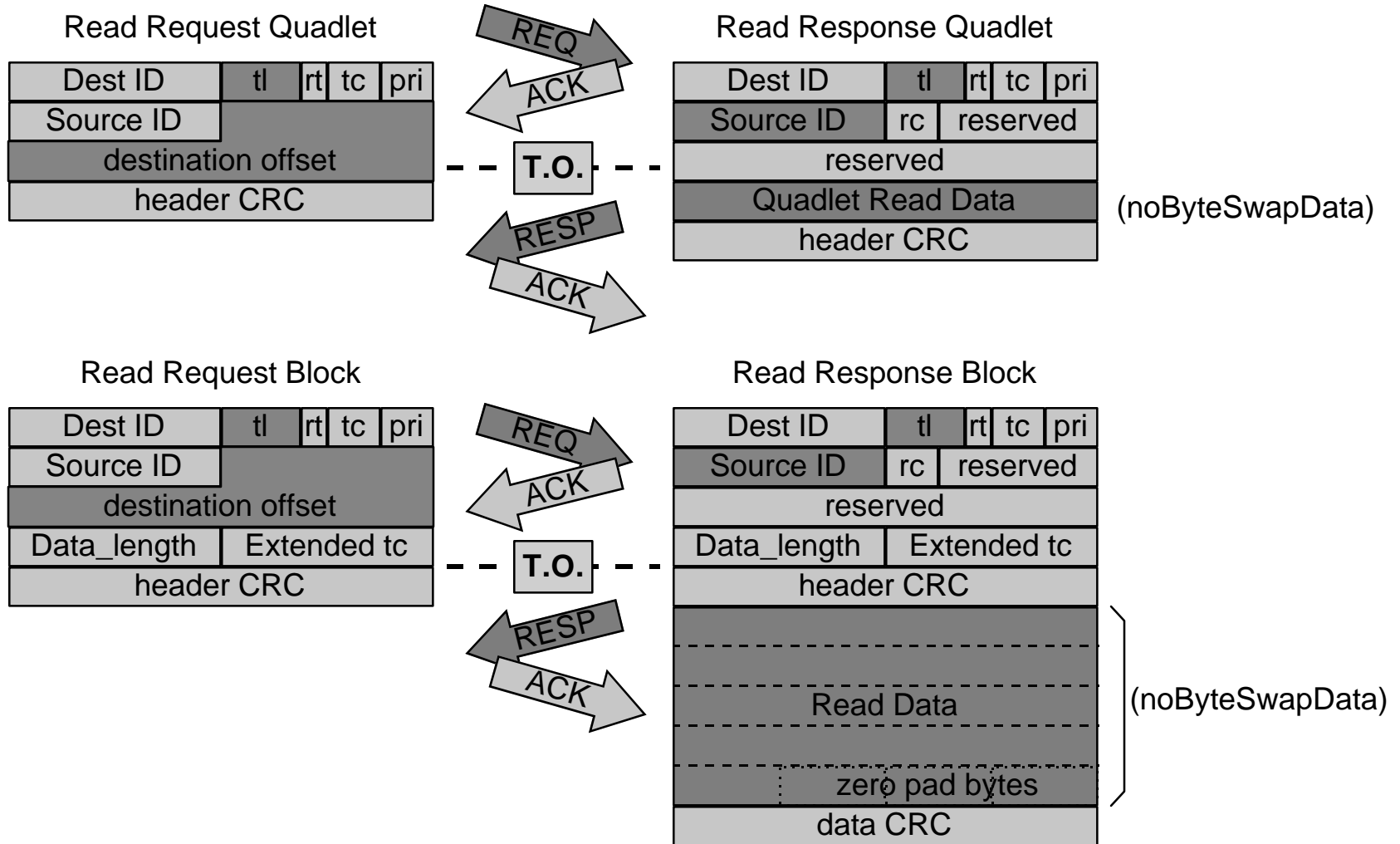




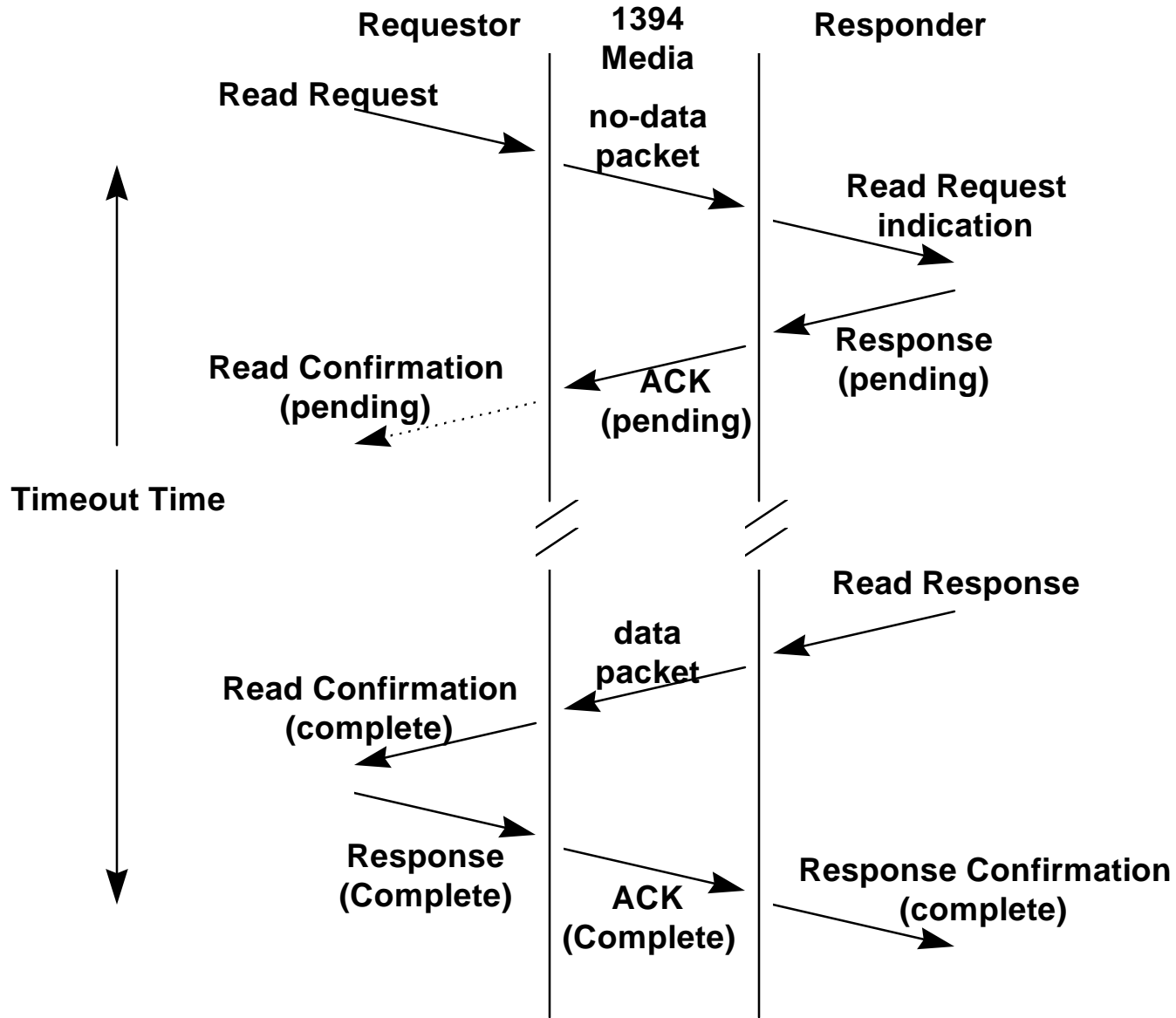
# Write Packets w/ ACK\_PENDING



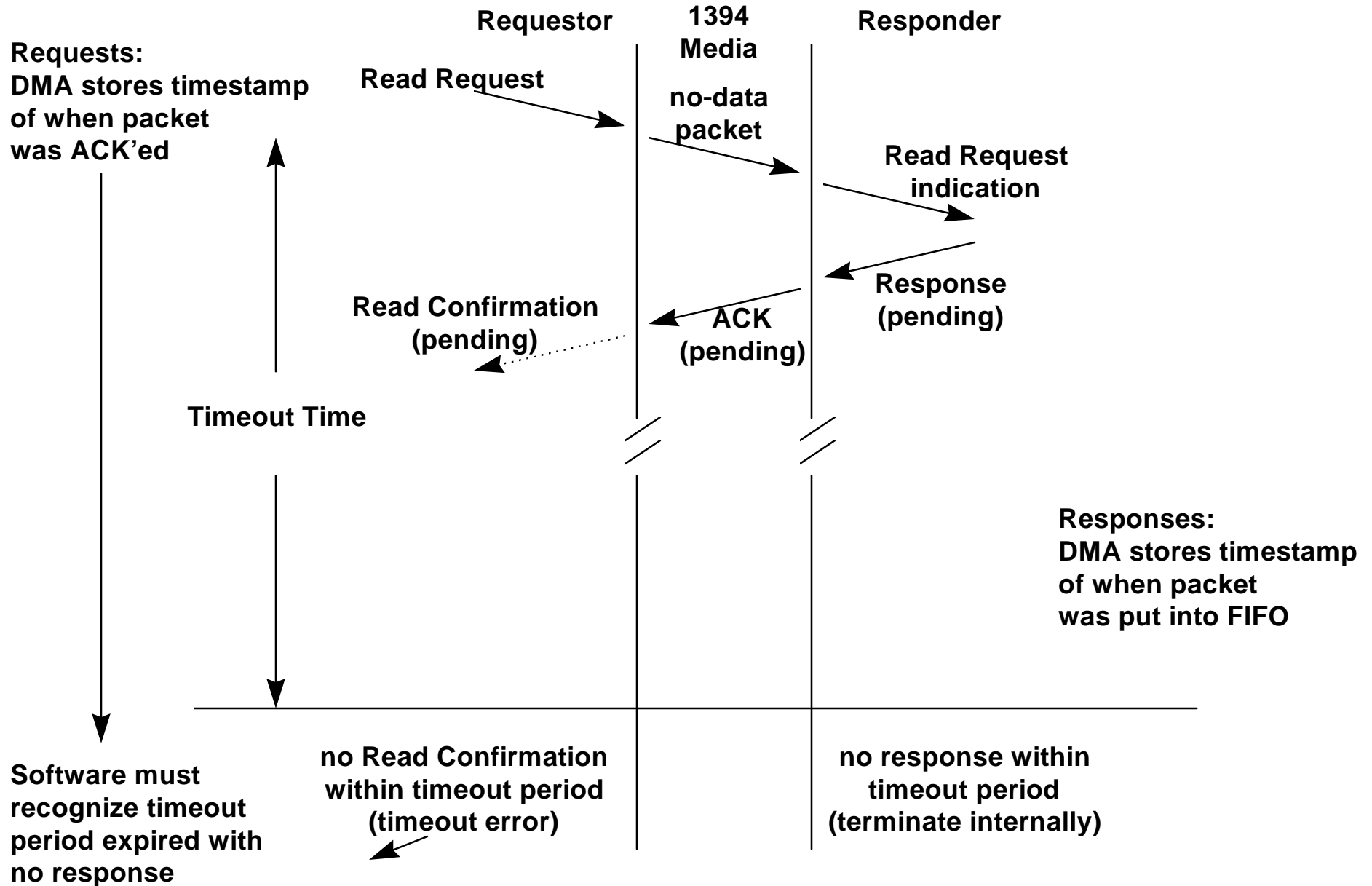
# Read Request / Response



# Split Transaction

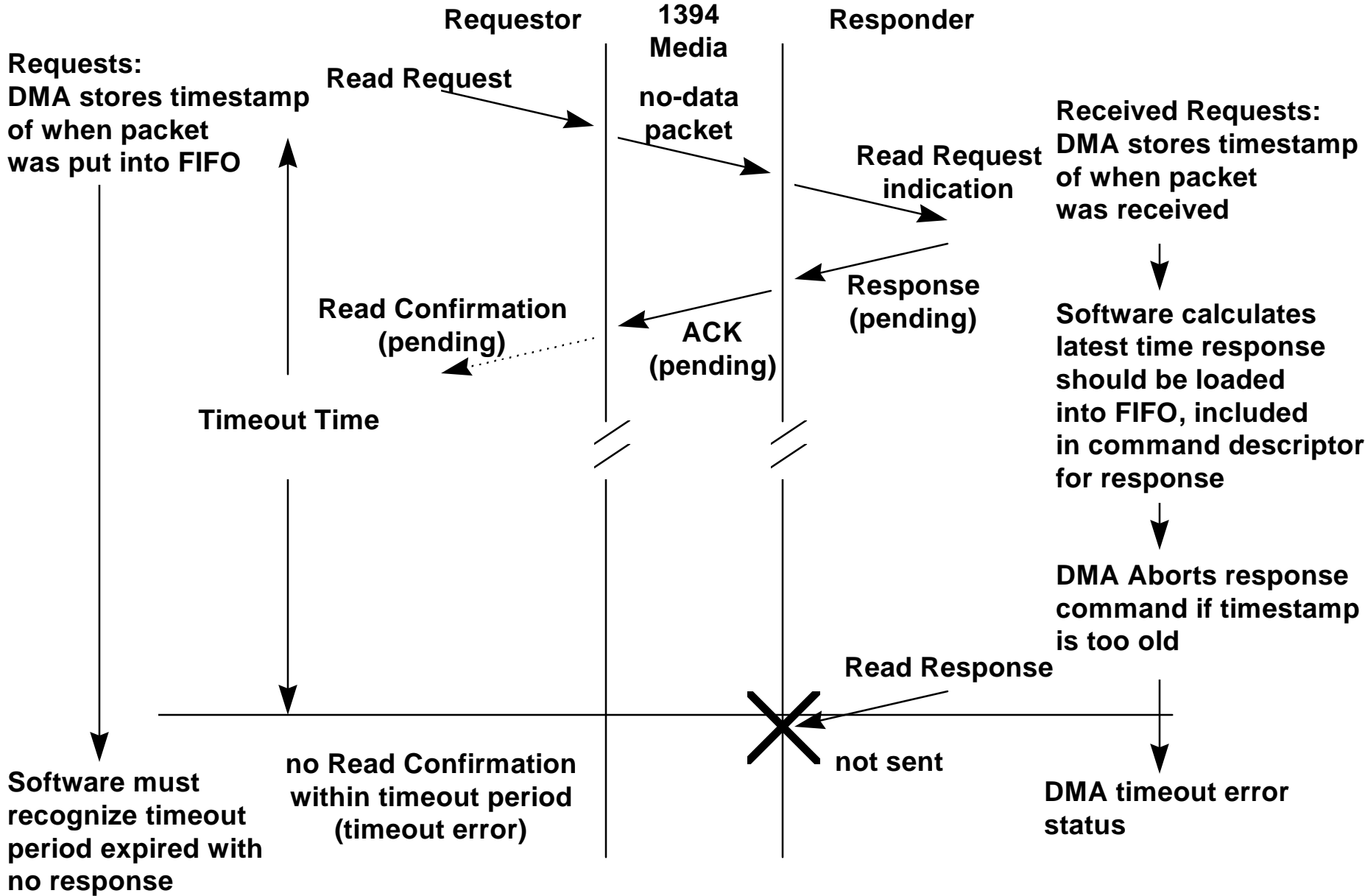


# Timeout





# Timeout

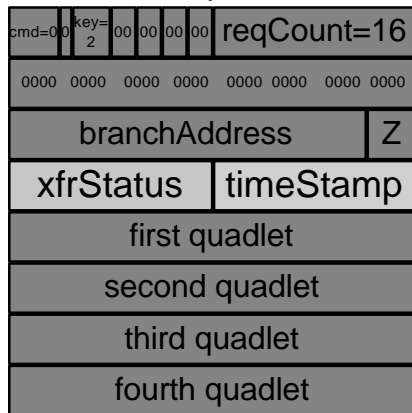




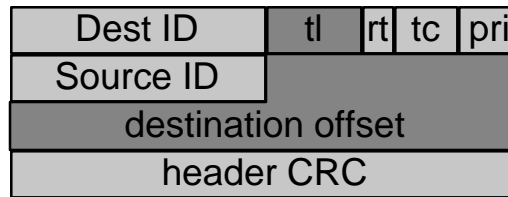
**PEN**

# OHCI Requests

OUTPUT\_LAST\_Immediate Request



Read Request Quadlet

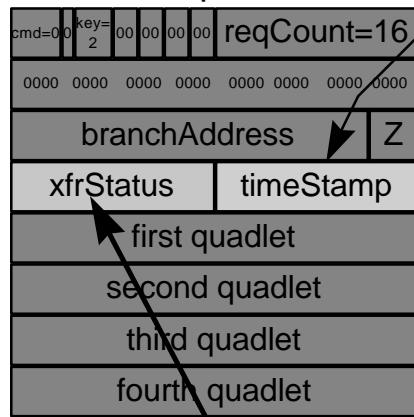


Time request packet was put into FIFO returned with status

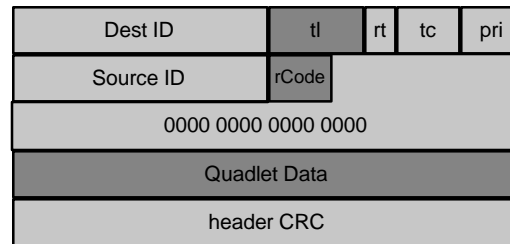
# OHCI Responses

Software specifies latest time to transmit packet in descriptor block

OUTPUT\_LAST\_Immediate Response



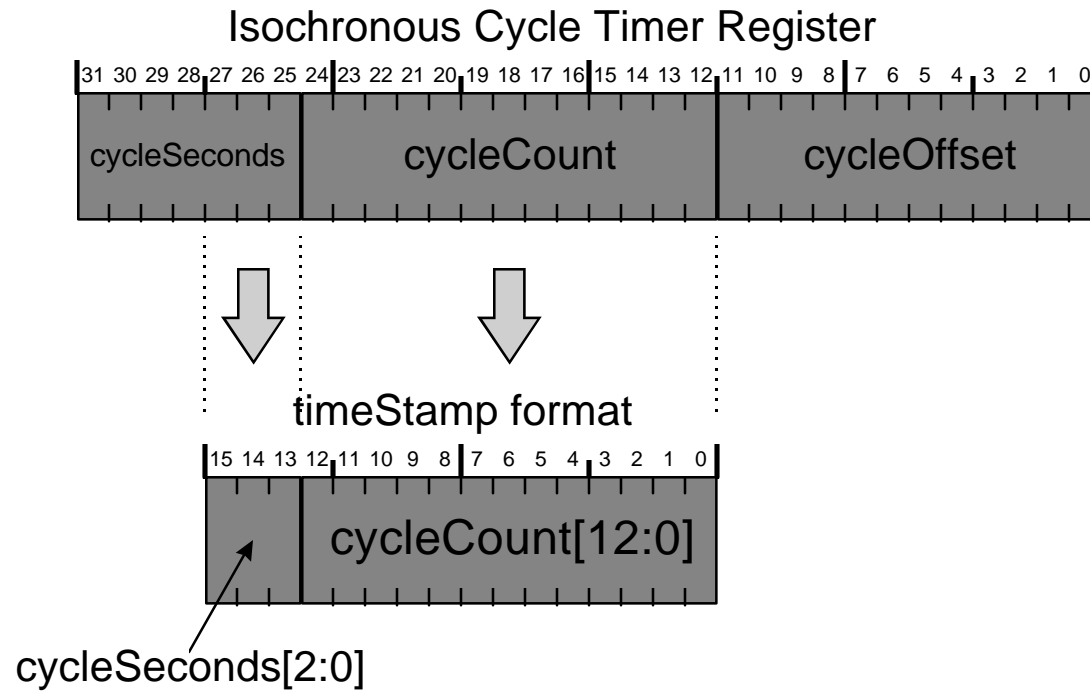
Read Response Quadlet



DMA checks time before putting in transmit FIFO

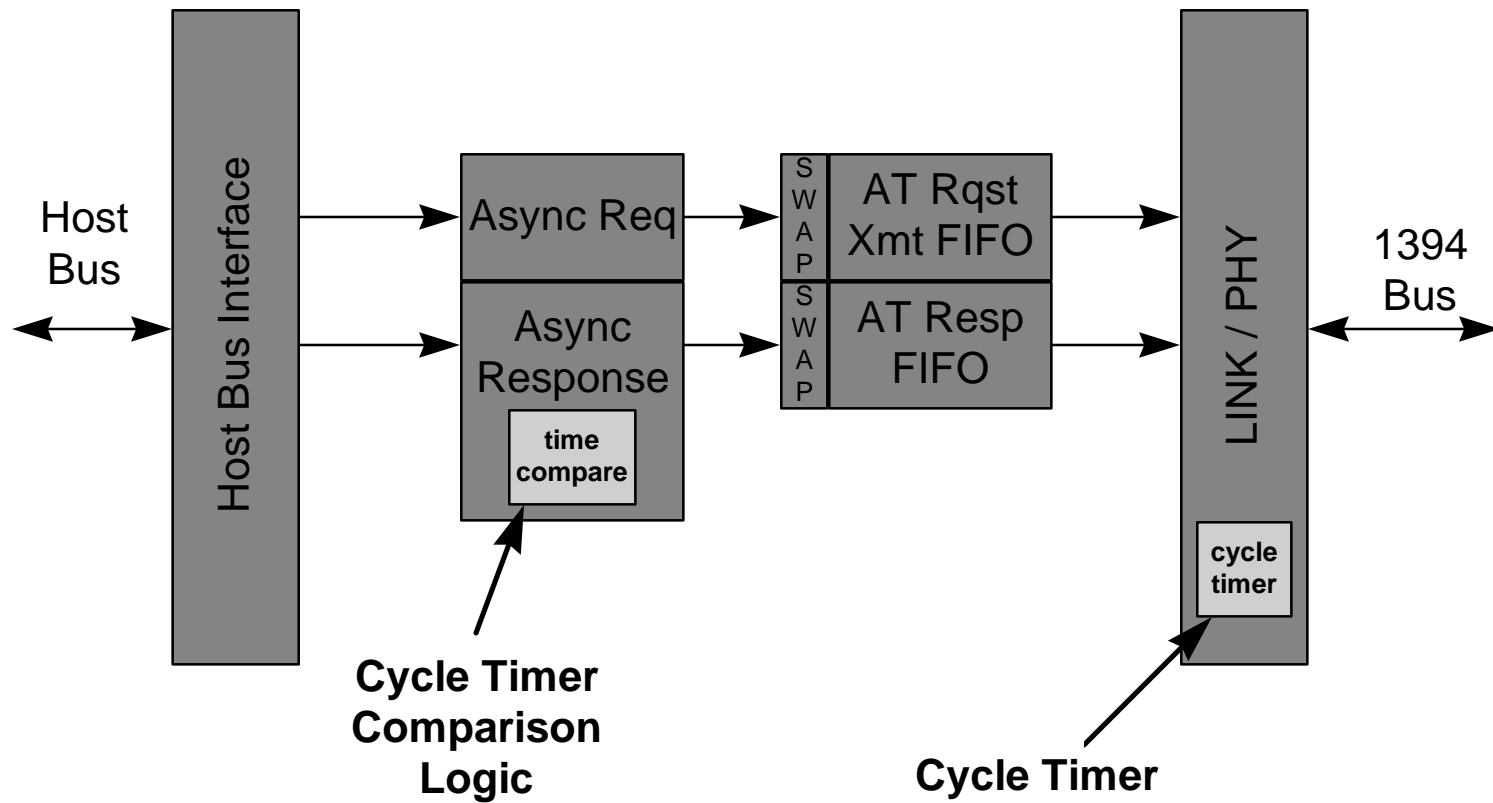
if timestamp is old, don't send packet, return error status

# timeStamp Format





# OHCI Response Transmit Diagram

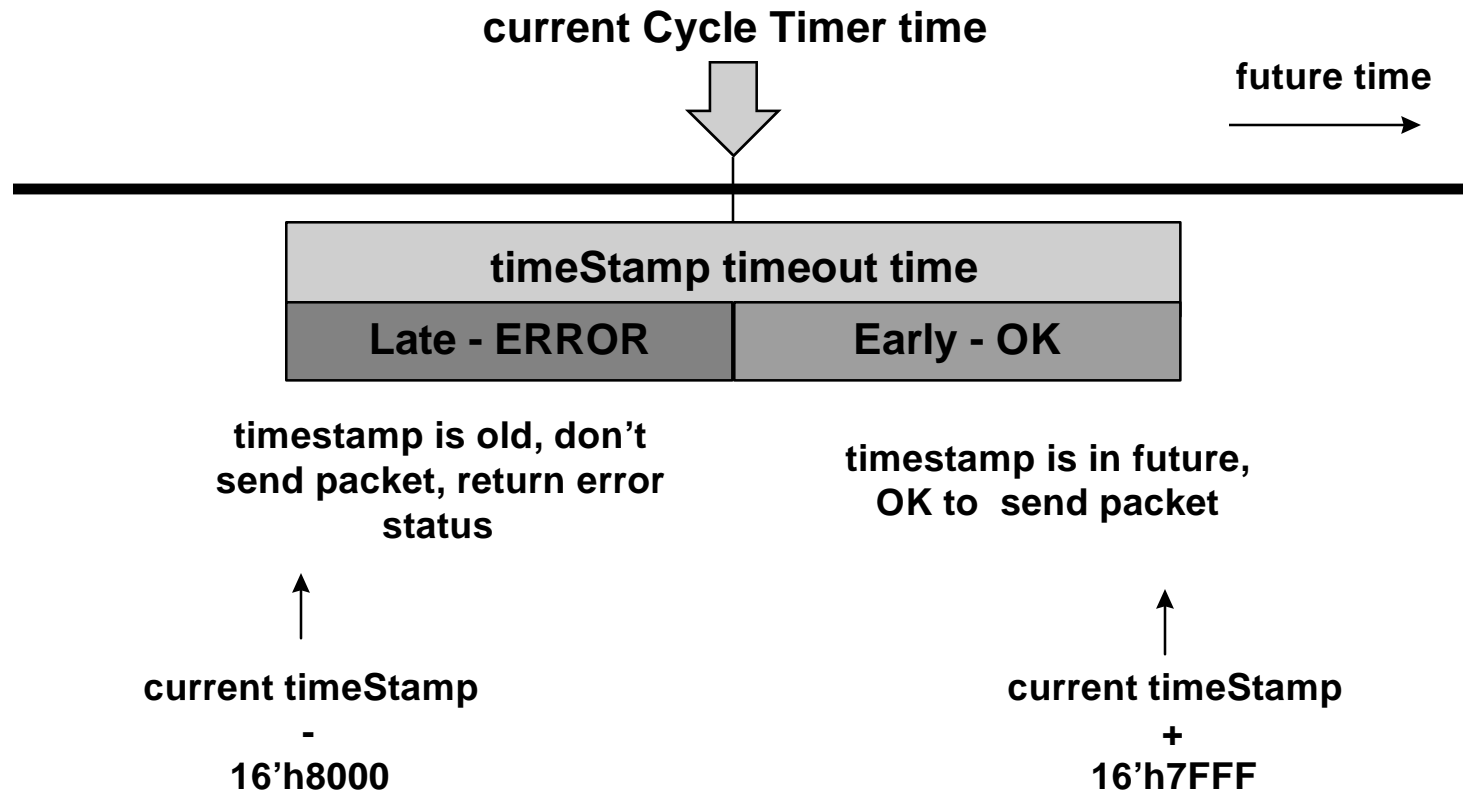




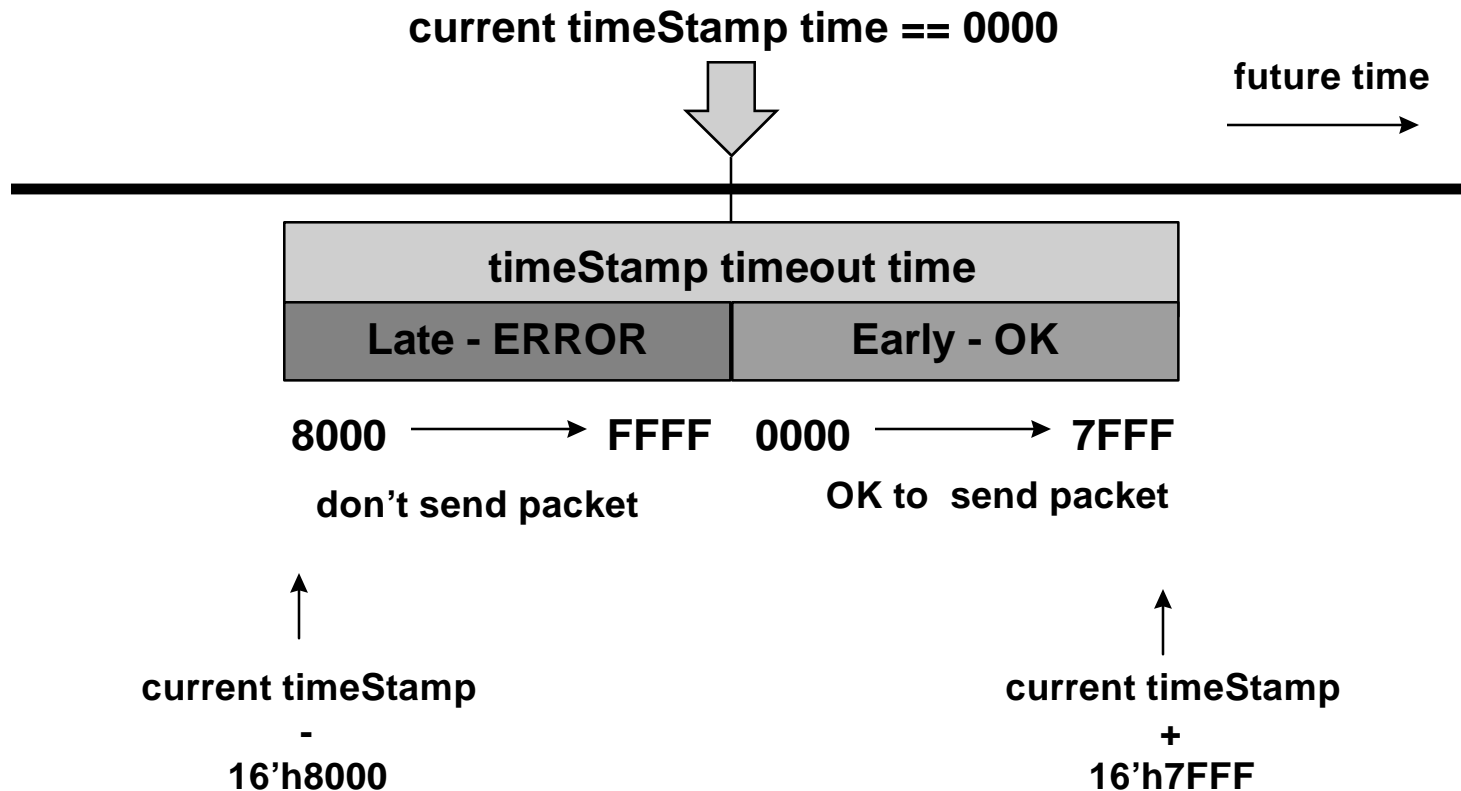
# Split Transaction Response Timeout

- ◆ **timeStamp represents a “Timeout” time**
- ◆ **Response can be transmitted if Current time is before timeStamp**
- ◆ **Otherwise, transmit is aborted**

# Response timeout comparison



# Response timeout example





# 1394 Bus Reset

- ◆ while busReset interrupt is active, flush async transmit
- ◆ wait for both async transmit `contextControl.active == 0`
- ◆ clear busReset interrupt
- ◆ re-build transmit commands

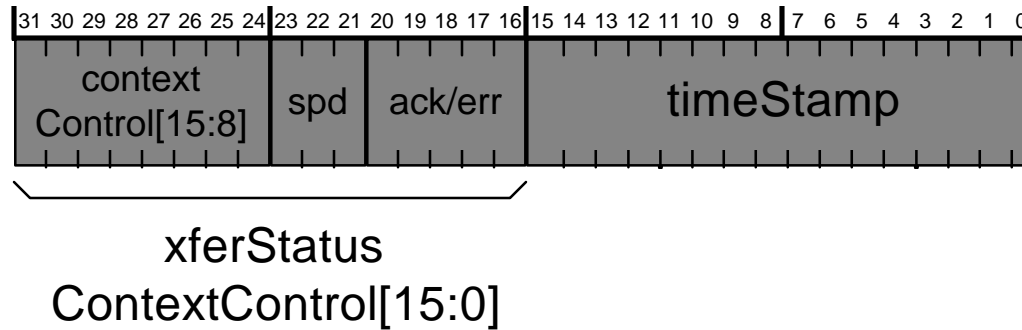


# Completion Status

- ◆ **written if “s” bit is 1**
- ◆ **written to OUTPUT\_LAST\*  
descriptor in block**

# Completion Status

## Status





# Retries

- ◆ **busied requests retried by DMA up to `ATRetries.maxATReqRetries` times**
- ◆ **busied responses retried by DMA up to `ATRetries.maxATRespRetries` times**
- ◆ **request retries must not block response**





# Interrupts

- ◆ **controlled by “i” bit in \*LAST\***
- ◆ **i = 11, interrupt on completion**
- ◆ **i = 01, interrupt only if didnot complete with ACK\_Complete or ACK\_Pending**
- ◆ **interrupt for each context**
  - **reqTxComplete**
  - **respTxComplete**



# Data Formats

- ◆ **no-data packets**
  - **quadlet read request**
  - **write response**
- ◆ **quadlet packets**
  - **quadlet write request**
  - **quadlet read response**
  - **block read request**



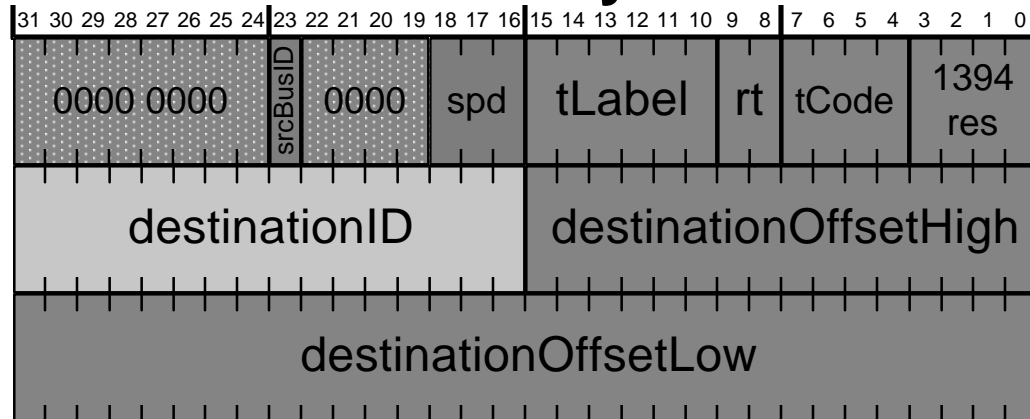
# Data Formats (con't)

- ◆ **block packets**
  - **lock request**
  - **lock response**
  - **block write request**
  - **block read response**
- ◆ **PHY packets**

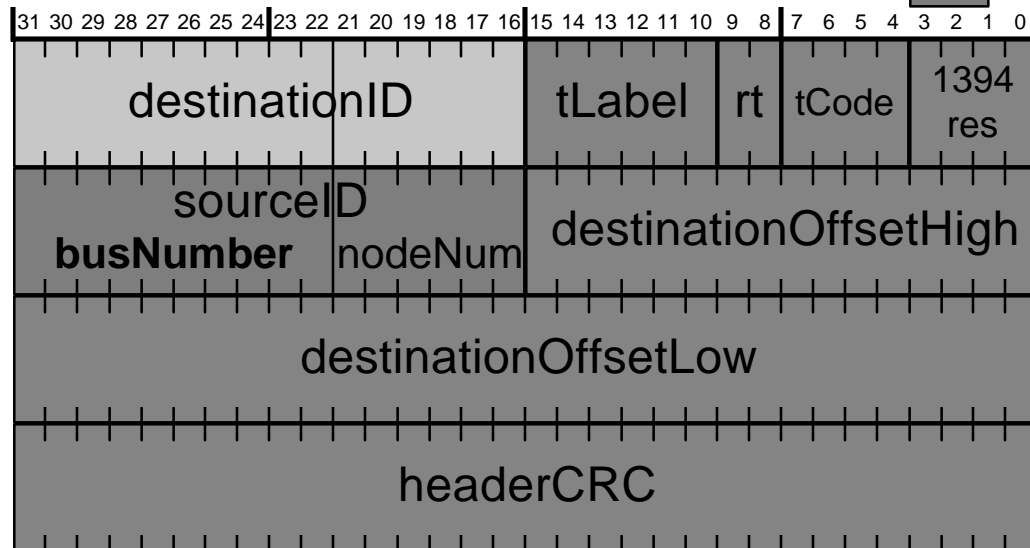
# Transmit Data Formats

## Quadlet Read Request

### Host Memory Format



### Transmitted on 1394 Bus @ spd



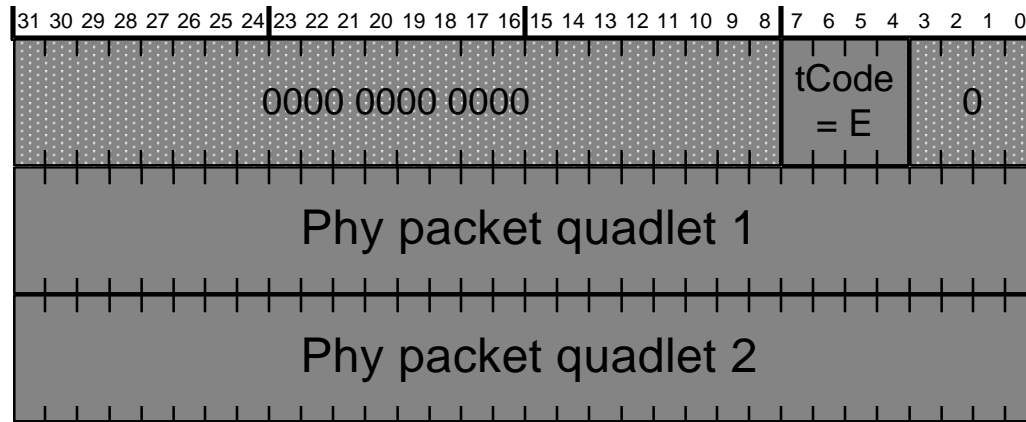
srcBusID	Transmitted busNumber
0	10'h3FF
1	NodeID.BusNumber



# Data Formats

## PHY Packet Transmit

### Host Memory Format



### Transmitted on 1394 Bus @ 100mb/s

