1394 Open HCI
Asynchronous Receive DMA

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Agenda

- AR Context Program
- BufferFill Mode
- AR Command and Control
- Asynchronous Request Filters
- Receive Data Formats

Asynchronous Receive Context Program

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AR Descriptor

- **Only one descriptor to choose from**
  - **INPUT_MORE**
- **Z field of Zero or One allowed**
- **Unconditional update of status after each packet is received (S = 1)**

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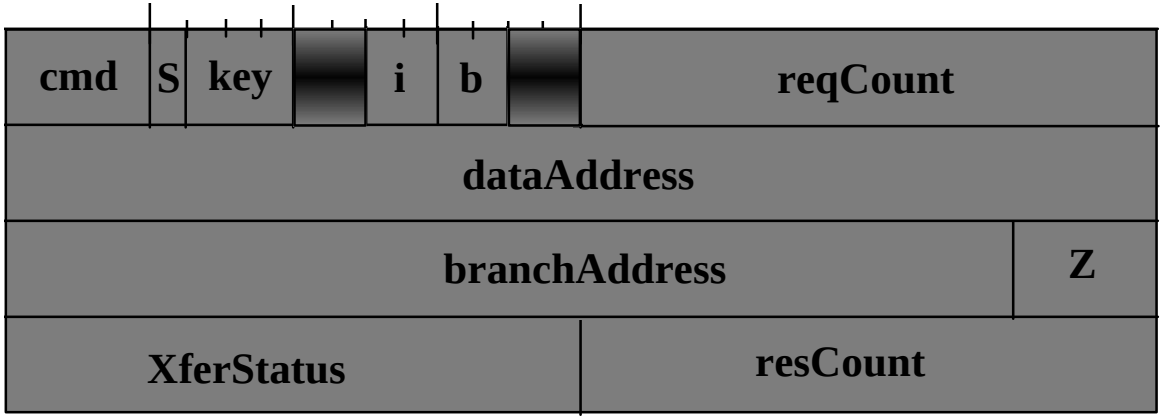
AR Descriptor Usage

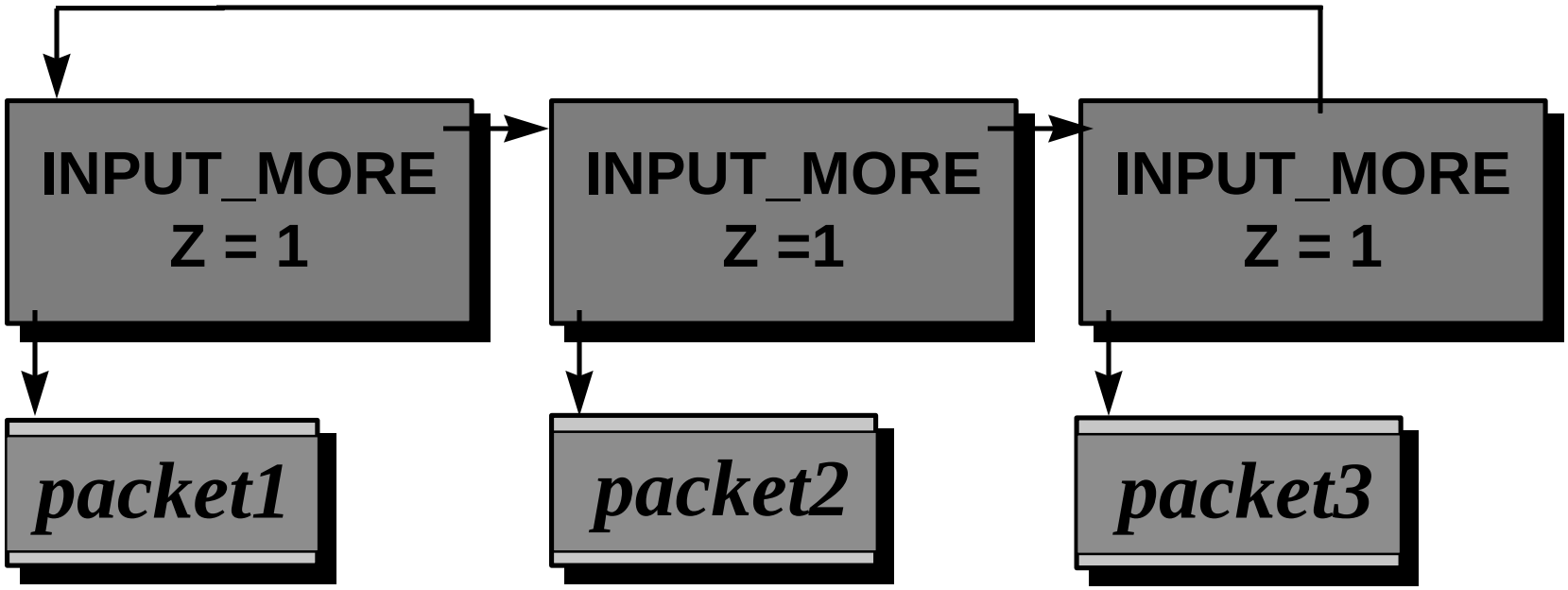
- INPUT_MORE to describe one or more packets
- Unconditional branch (Z = 1) to next INPUT_MORE descriptor
- Easy stop mechanism (Z = 0)
- Update of status (S =1)

INPUT_MORE Descriptor



- Cmd = 4'h2 (INPUT_MORE)
- Key = 3'b0
- Z = 0 or 1
- S = 1

Using AR Cmd Descriptors



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BufferFill Mode

- Data buffers can be upto 64 K
- Receive packets can cross multiple buffer descriptors or be contained in one descriptor
- No buffer descriptors will result in receive packets to be dropped
- Insufficient buffer space will result in rest of packet to be dropped
- Do not have to support posted writes, can send ack_pending

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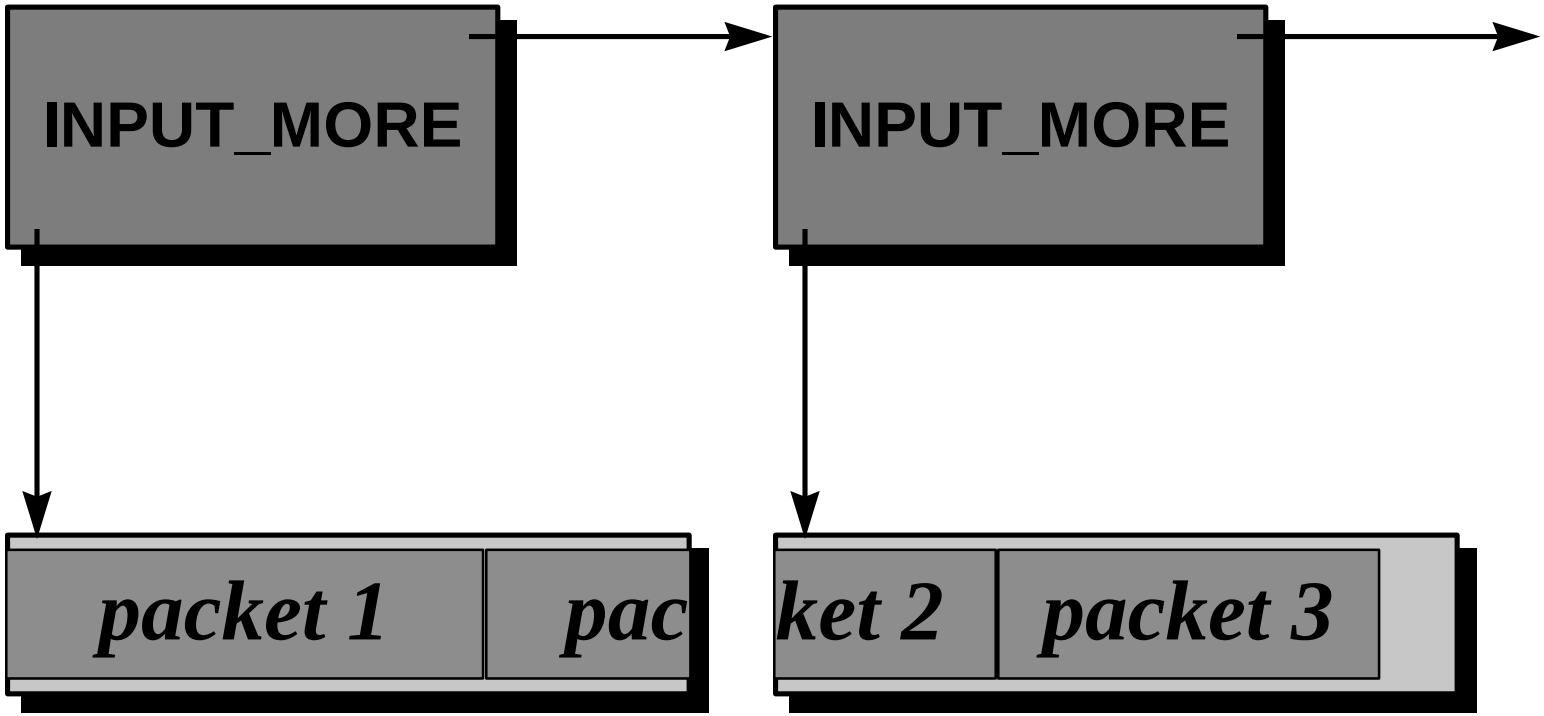
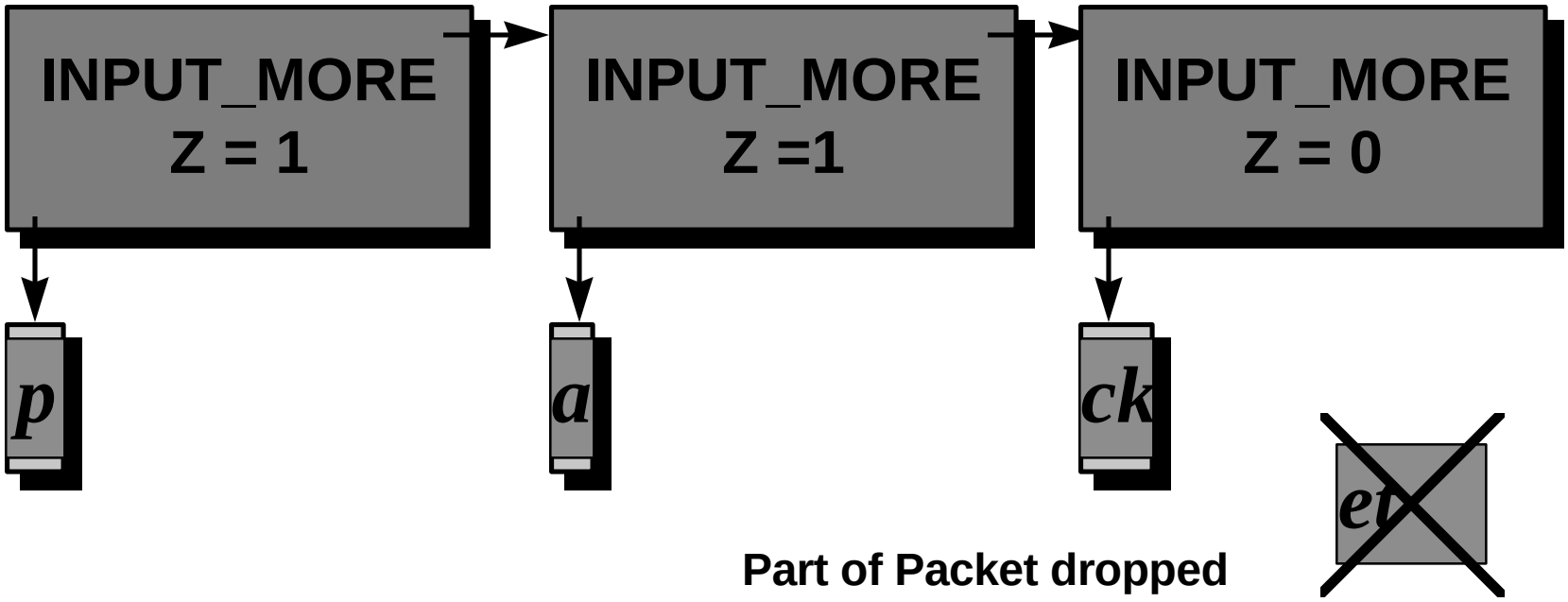
BufferFill Mode (2)



BufferFill Mode (3) insufficient descriptors



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Asynchronous Context Command & Control

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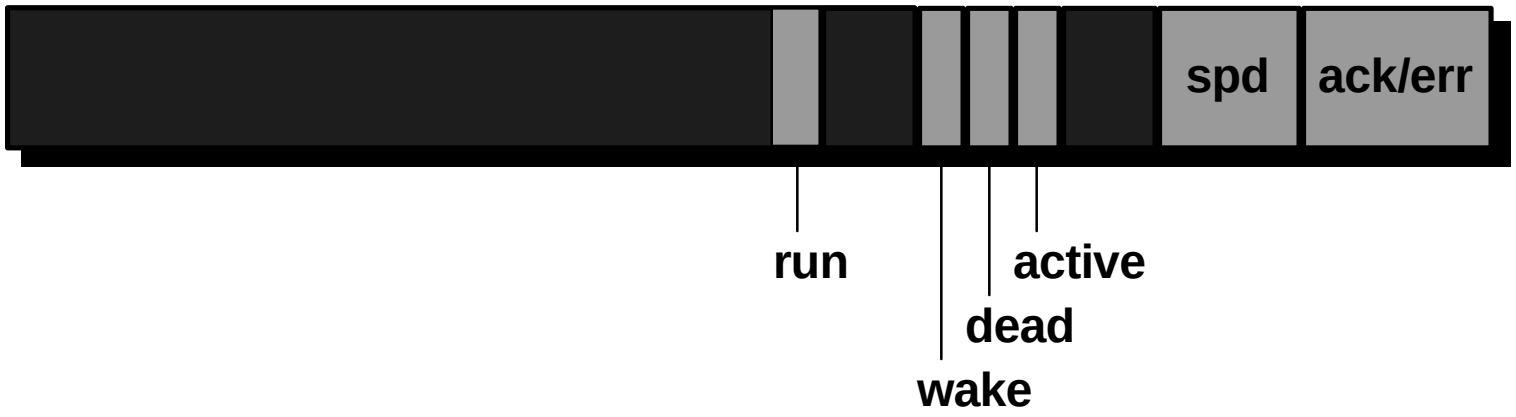
Command Pointer

- To start the asynchronous receive context
  - Load CommandPtr with descriptor address
  - Set run bit in Context Control register
- ARDMA stops (active = 0)
  - when Z = 0 or run is deasserted
- CommandPtr can only be written when DMA has stopped (active = 0)

Context Control



- Set run to start DMA
- Wake mechanism can be used to append descriptors
- Speed & ack/err codes reported

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Two Contexts

- **Request context**
- **Response context**

Interrupts (IntEvent)

- Two interrupts for each context
- Async Response
  - Responses (RsPkt) per packet
  - DMA buffer completion (i = 2'b11, ARRS is set in IntEvent)
- Async Request
  - Requests (RqPkt) per packet
  - DMA buffer completion (i = 2'b11, ARRQ is set in IntEvent)

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Asynchronous Request Filters

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Request Filters

- Selective access to host memory provided by two sets of 64-bit set-clear registers
  - PhysRequestFilter & AsynchRequestFilter
- Request Filter not applied to quadlet reads to Config ROM
- No effect on Response packets
- Request offsets above 48'h0000_FFFF_FFFF are always sent to the Async Request DMA
- Request offsets below 48'h0001_0000_0000 can be processed by PhysicalRequestFilter (if enabled)
- if Async/Phys ReqResourceAll bit is set, then request from any other bus (bus other than 10'h3FF and busID) will be accepted

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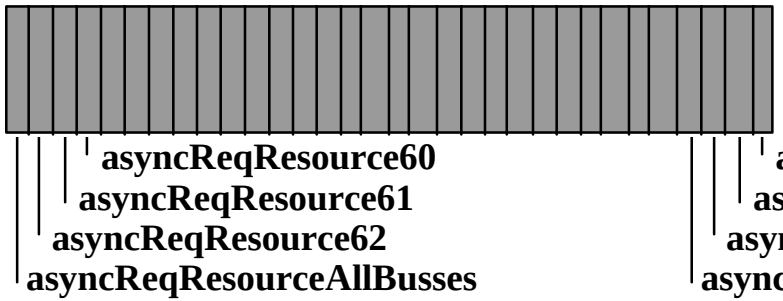
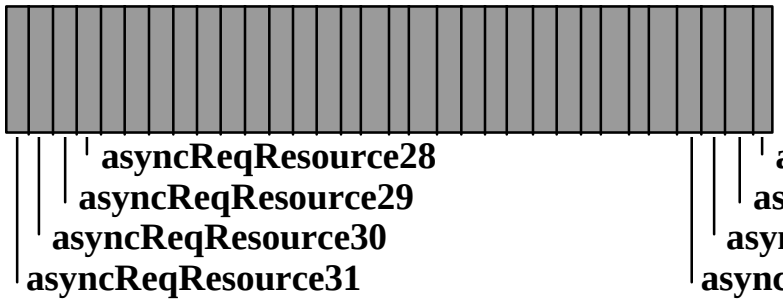
AsyncRequestFilter

RequestFilterHi register

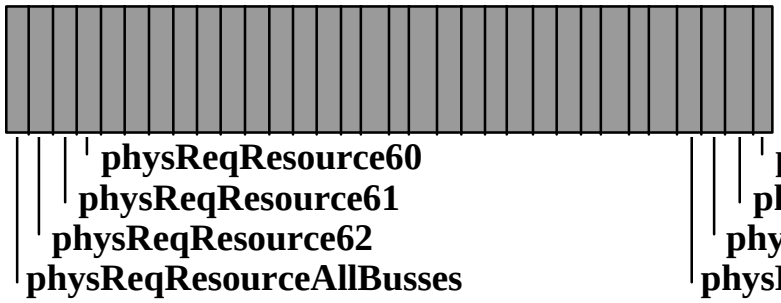


RequestFilterLo register

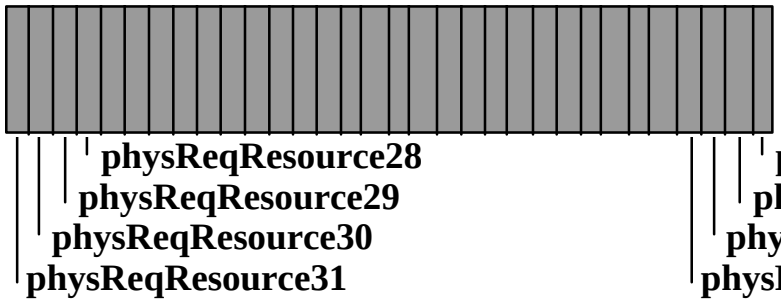


PhysRequestFilter

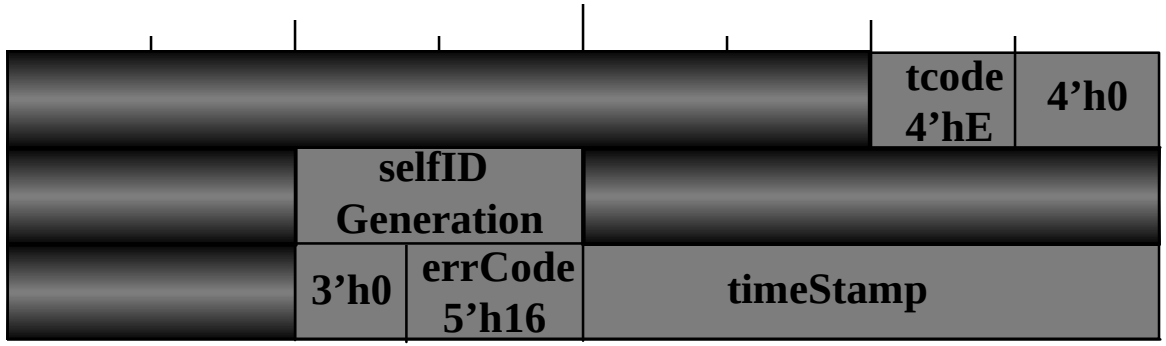
RequestFilterHi register



RequestFilterLo register



Bus Reset Packet



AR Request Context Bus Reset packet format

- **errCode = 5'h16 indicates this is a bus reset packet**
- **Inserts a synthesized bus reset packet into the AR DMA Request Context Buffer as soon as a bus reset is detected**
- **selfIDGeneration corresponds to previous bus reset**
- **If the fifo is full, the AR Request controller will insert the bus reset packet the moment the fifo has space available**

Receive Data Formats

Four basic types of Receive Packets

- **No-data Packets**
  - **Quadlet Read Request & All Write Responses**
- **Quadlet Packets**
  - **Quadlet Write Requests**
  - **Quadlet & Block Read Responses**
- **Block Packets**
  - **Lock Request & Responses**
  - **Block Write Request & Read Responses**
- **PHY Packets**

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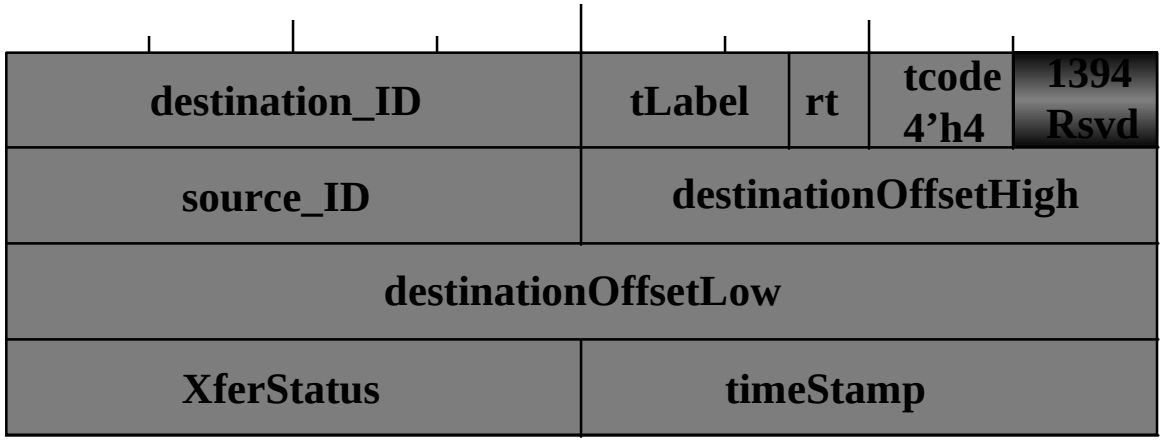
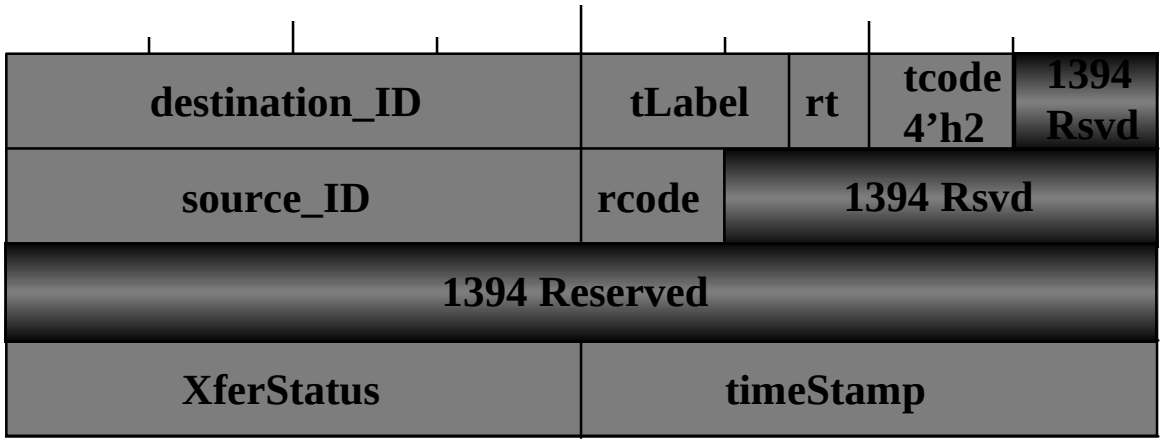
No-data Receive



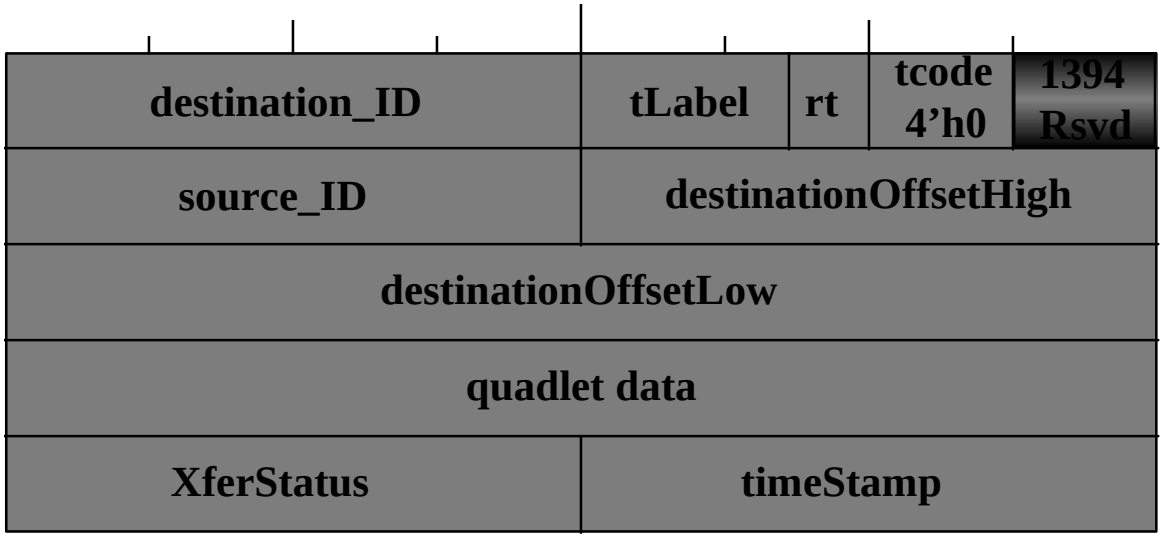
Quadlet read request receive format

No-data Receive (2)



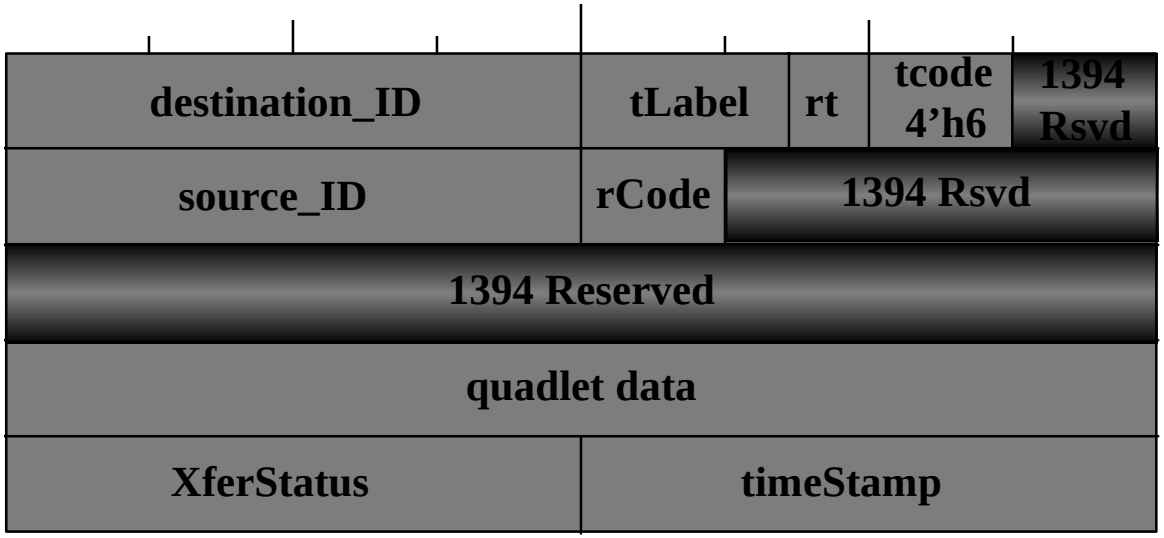
Write response receive format

Quadlet Packets



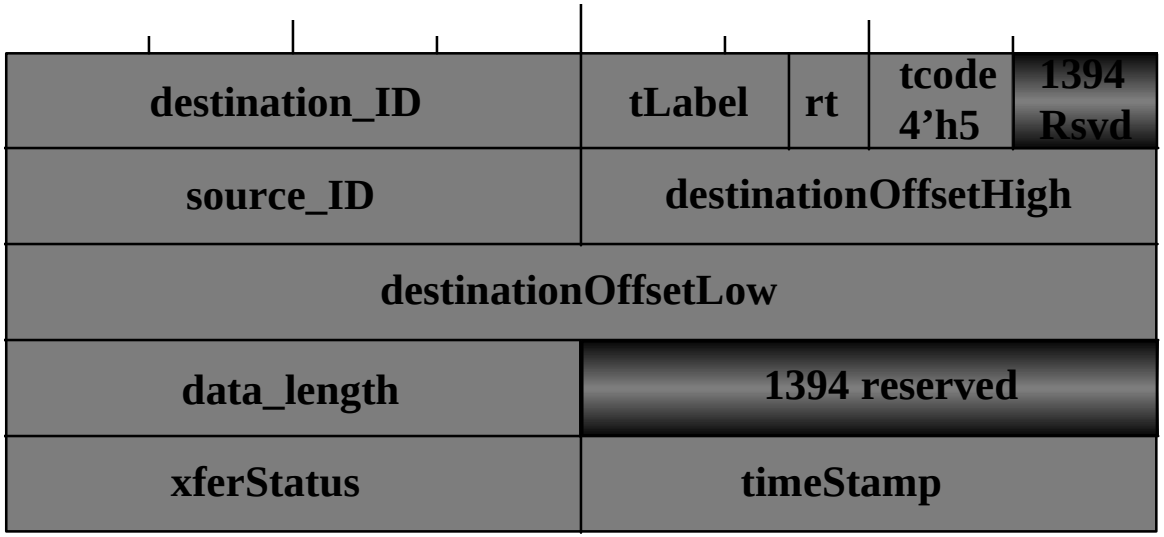
Quadlet write request receive format

Quadlet Packets (2)



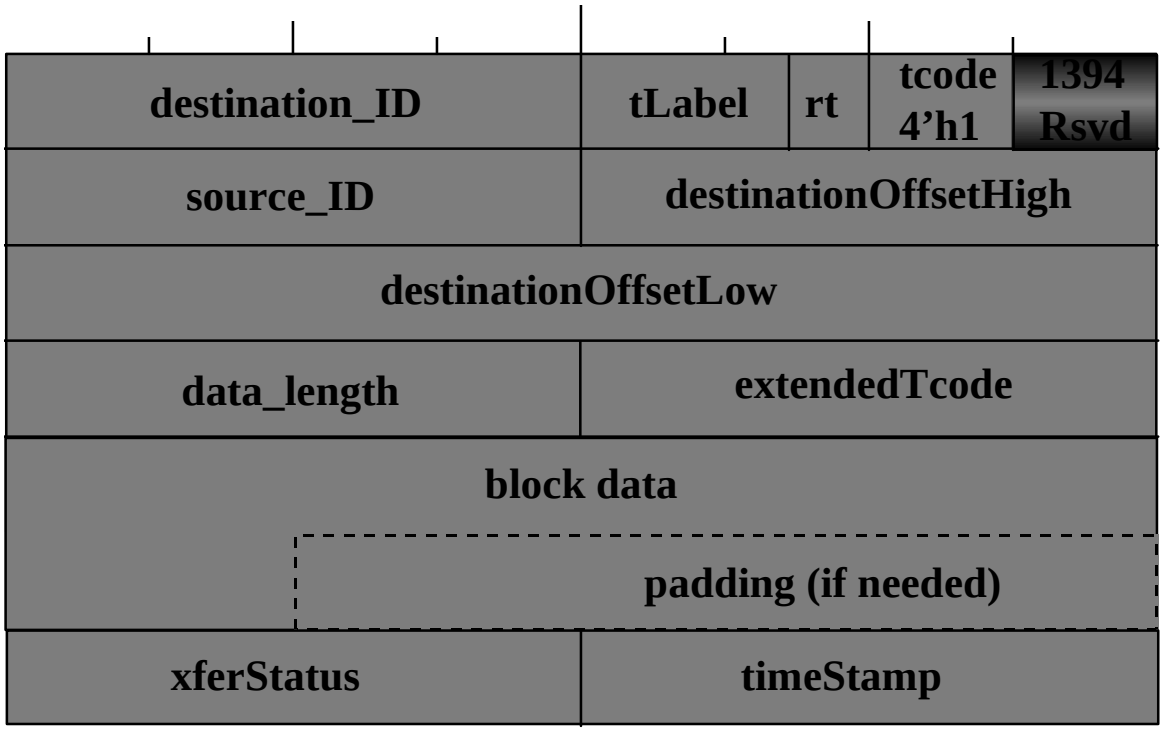
Quadlet read response receive format

Quadlet Packets (3)



Block read request receive format

Block Packets



Block write request receive format

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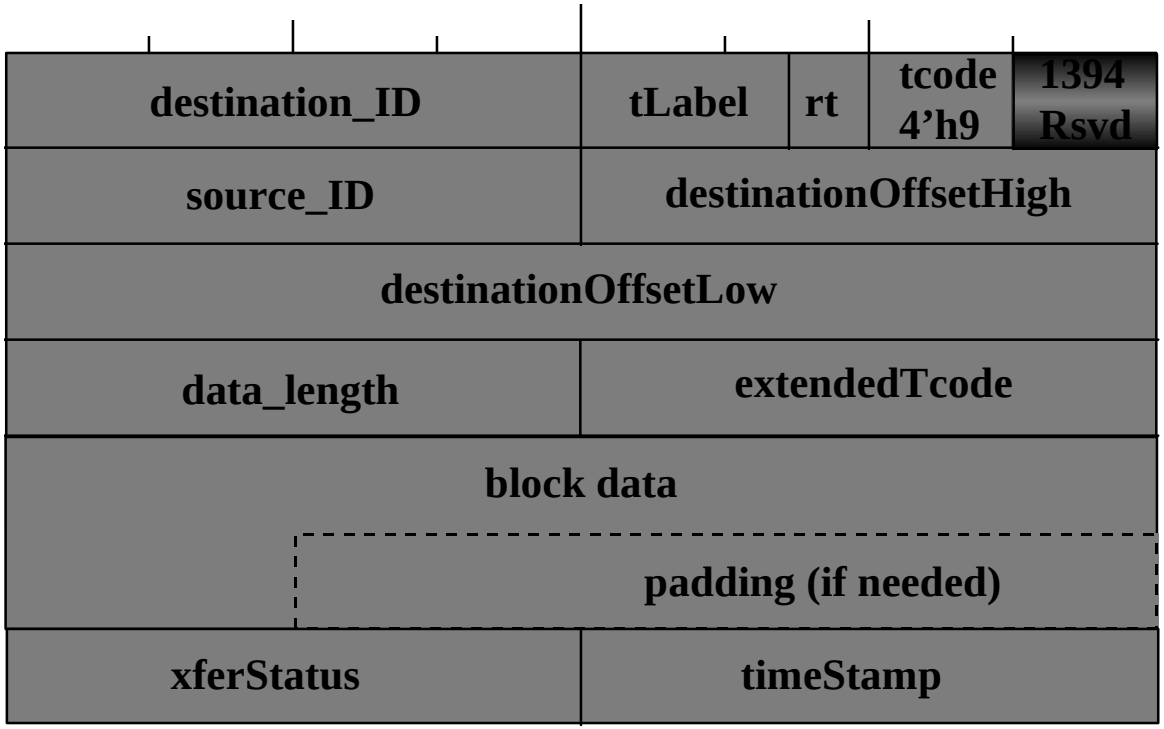
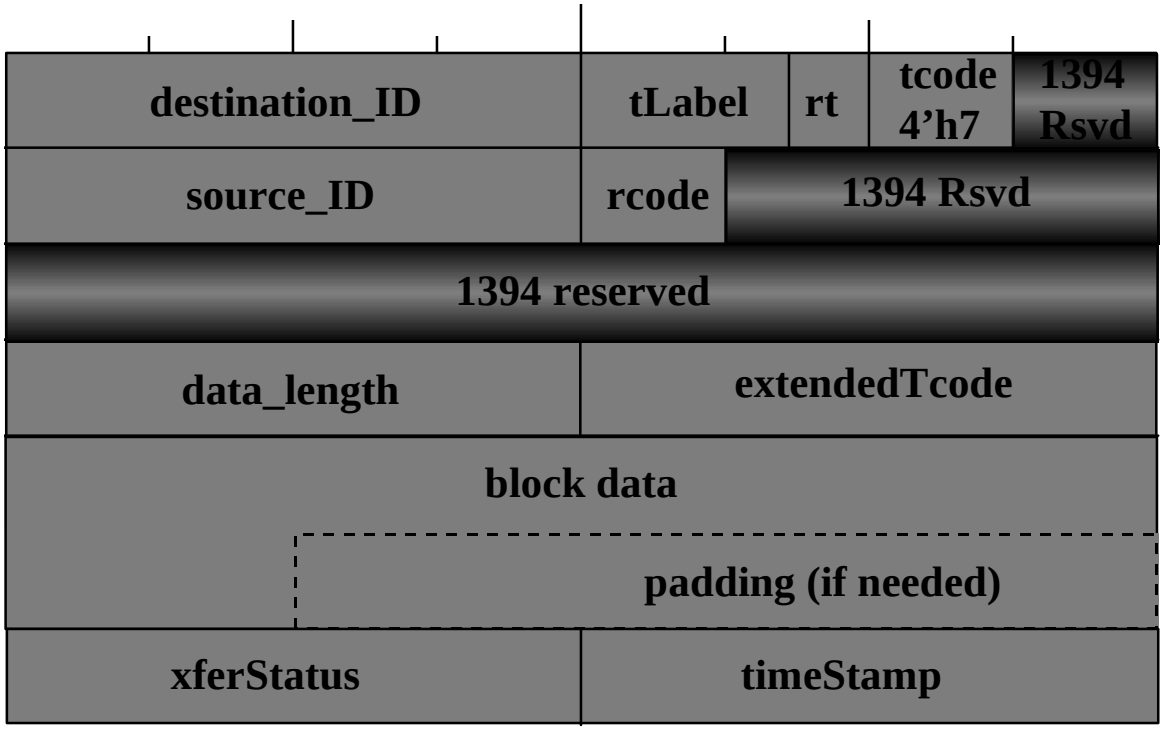
Block Packets (2)



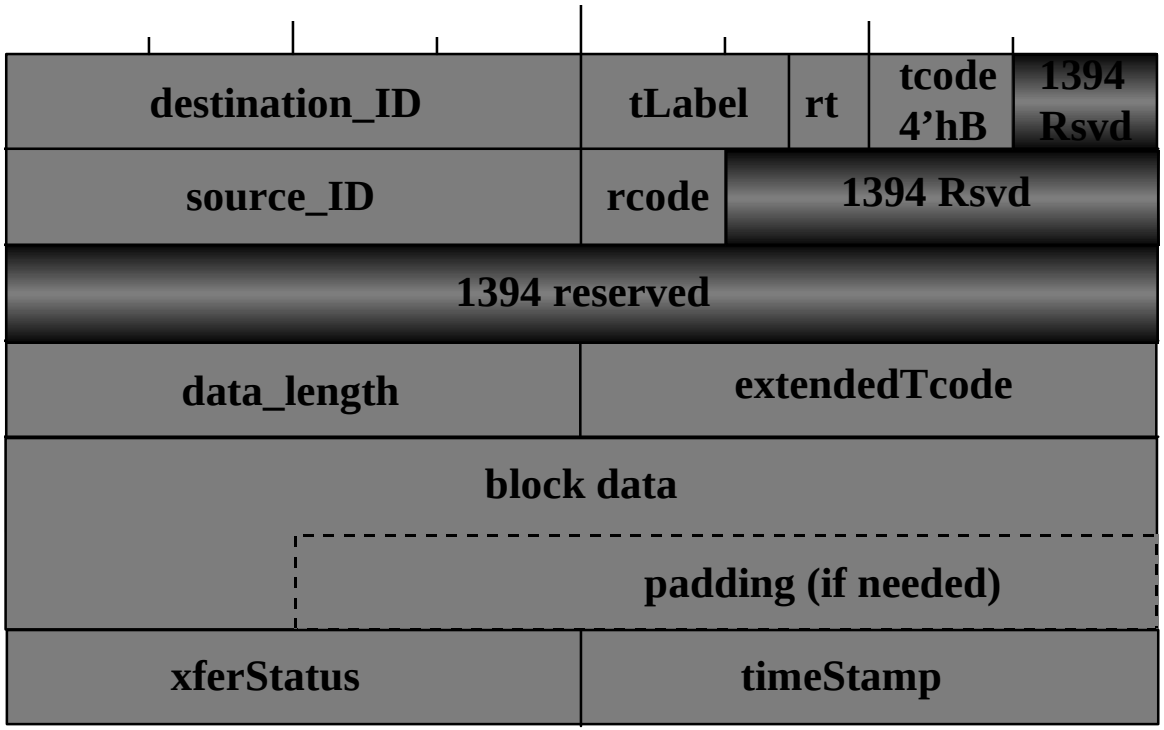
Lock request receive format

Block Packets (3)



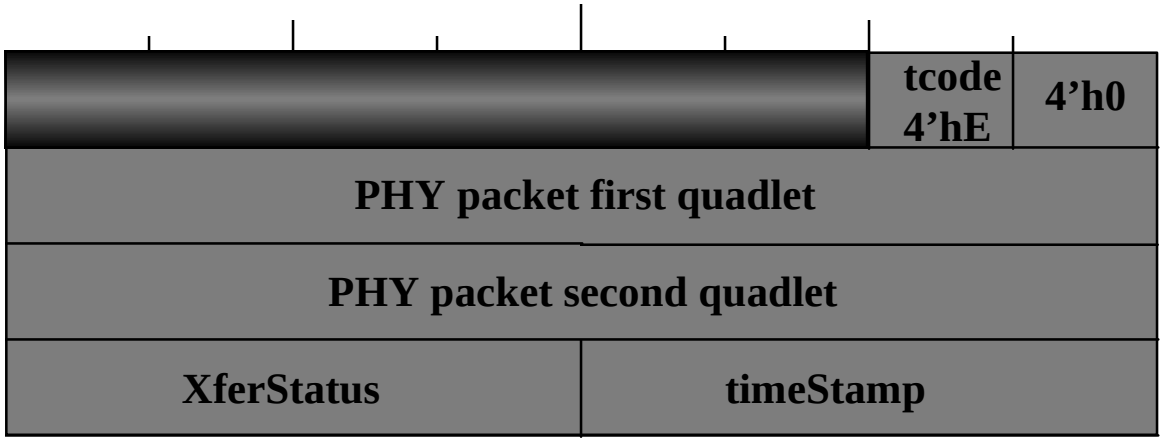
Block read response receive format

Block Packets (4)



Lock response receive format

PHY Packets



PHY packet receive format

- **First word contains a synthesized tCode of 4'hE**
- **Only PHY packet first quadlet is stored, second quadlet is verified and stripped**
- **SelfID packets not arriving during the bus initialization phase are received as PHY Packets**

End