PowerPC™

PowerPC™ 604 SMP Reference Design Errata Summary Revision 1.0

This document details reference design and Technical Specification errata that were discovered after the initial printing of release 1.0 of the Technical Specification. Workarounds and corrections are described.

Document Number:
MPRZAPESU-01
December 1995

IBM ®

PowerPC™ 604 SMP Reference Design Errata Summary, Revision 1.0

December 1995

This document describes PowerPC 604 SMP Reference Design Release 1.0 errata which were identified after the initial printing of the technical specification. Board errata 1:8, which were discovered prior to that date, are listed in Section 12 of the technical specification (*PowerPC 604 SMP Reference Design Technical Specification Release 1.0*, MPRZAPTSU-01). Also described are upgrades that will enhance the performance of a release 1.0 reference design for compatibility with release 3.0 of the reference design. Release 1.0 Technical Specification corrections are also included.

Reference Design Errata

These errata concern release 1.0 of the PowerPC 604 SMP Reference Design, which corresponds to pass 2 of the reference board.

Errata 9 . . . . . . Ethernet Interrupt Pullup Resistor

Date 10/23/95

Functional . . . . . . The pullup resistor was left off of the Ethernet interrupt net, which is driven by an open collector output in the Ethernet controller.

Work Around . . . Install an 8.2kΩ resistor from INT_ETHNT* (U2 pin 117) to a convenient +5v.

Errata 10 . . . . L2_PD[0:1] Pullups

Date 11/07/95

Functional . . . . . . The pullup resistors were incorrectly omitted from the L2_PD_CPU[0:1] nets for both CPU slots.

Work Around . . . Add a 10k Ω resistor to +3.3v to the following nets:

Net	Board Reference
CPU Slot 1: L2_PD0	J8 pin 241
CPU Slot 1: L2_PD1	J8 pin 244
CPU Slot 2: L2_PD0	J9 pin 241
CPU Slot 2: L2_PD1	J9 pin 244

Errata 11 . . . . . ZC3 Update

Date 11/07/95

Functional . . . . . . The ZC3 PAL has been updated to ZC3B. It is necessary to reprogram the ZC3 PAL to the latest code level.

Work Around . . . In the PAL design file, change the pin 15 output (MASK_PCI_GNT) from combinatorial to registered. The new line should read:

```
PIN 15     MASK_PCI_GNT    REG     ;Registered    to ZP
```

Reference Design Upgrades

The following upgrades will enhance the performance of a release 1.0 reference design for compatibility with release 3.0 of the reference design.

Upgrade 1 . . . Upgrade From MPIC-2 to MPIC-2A

Functional . . . . . . MPIC-2 is no longer generally available. MPIC-2A offers enhanced features.

Details . . . .

Item	IBM p/n	Toshiba p/n	package
MPIC-2	11H9484	TC160G54HS-1230	
MPIC-2A	39H9930	TC160G54AF-1414	plastic
MPIC-2A	39H9930	TC160G54ES-1414	ceramic

Installation of MPIC-2A also requires upgrading the ROM code to version 2.0.

Upgrade 2 . . . Upgrade ROM Code From Version 1.x to Version 2.0

Functional . . . . . . Upgrade the version 1.x ROM code associated with release 1.0 of the reference design to release 2.0 ROM code to enhance the firmware function for compatibility with release 3.0 of the reference design. Contact your IBM technical representative for details.

Upgrade 3 . . . Upgrade System EPLD

Functional . . . . . . The ability to reset the system via a software command was added.

Work Around . . . The EXTHRST# output was added to the system EPLD. EXTHRST# acts in parallel with the reset pushbutton. See Figure 1 below.

Details . . . .
1. Change C350 from .1uf to .01uf.
2. Remove R884.
3. Connect R844 pad1 to a convenient via connected to C350 pin1.
4. These changes require upgrading the ROM code to version 2.0**.**
5. Reprogram the system EPLD with the code shown in the Revision 3.0 *PowerPC 604 SMP Reference Design Technical Specification*.

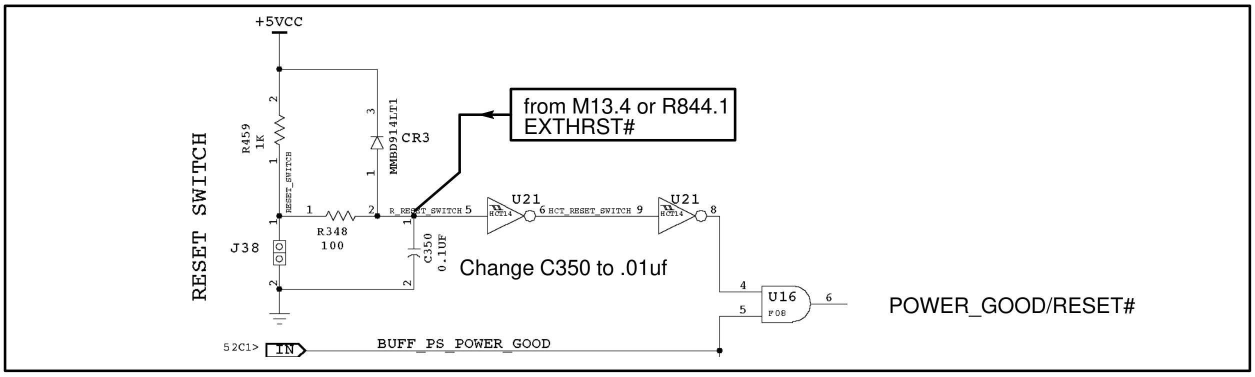

Figure 1. Generic Implementation PAL Installation

Upgrade 4 . . . Upgrade to Release 3.0 Technical Specification

Various improvements (in addition to the changes shown herein) have been made to release 3.0 of the technical specification. Contact your IBM representative for availability information.

Technical Specification Errata

This section corrects errors which were found in the *PowerPC 604 SMP Reference Design Technical Specification Release 1.0*.

Section 1.1	**Page 23**	IBM will not offer PowerPC 604 SMP Reference Boards or Systems for sale. Instead, IBM has enabled other vendors to design and manufacture boards and systems based on the reference design. Contact your IMD Field Marketing Representative for further information.
Section 2.7.1	**Page 48**	In the L2_BR# entry of Table 4, change column 2 from O to I.
Section 2.7.1	**Page 48**	In the L2_BG# entry of Table 4, change column 2 from I to O.
Section 2.7.6	**Page 60**	In Table 8, change pin 108 from L2_AACK_EN to L2_AACK_EN#.
Section 2.7.7	**Page 63**	In Table 9, change pin 5 from HALT_B/QREQ_B# to HALT_B/QREQ_B.
Section 2.8.2	**Page 67**	In the A[1:28] entry of Table 12, change column 1 from A[1:28] to A[0:28]. Also make this change in column 5.
Section 2.8.8	**Page 76**	In Table 16, change pin 100 from SRAMWE3# to SRAM_WE3#.
Section 4.1.3	**Page 102**	In column 2 of Table 30, change the pin 1 entry from BR# to SYS_BR#. In column 2 of Table 30, change the pin 11 entry from INTA# to INT_A#.
Section 4.2.2	**Page 104**	The CPU power supply pinout that is implemented by the 2.5v power supply circuit may not be valid for future processors. See the individual processor hardware specification for that information.
Section 2.5.1	**Page 109**	In Table 35, change pin 108 from L2_AACK_EN to L2_AACK_EN#.
Section 6.2	**Page 122**	A new section on SMP reset considerations has been added to release 3.0 of the reference design technical specification.
Section 6.2.1	**Page 122**	The four items in the reset list have been reordered for release 3.0, but changes have been made only to the CPU Enable Register section (was #4) as follows: CPU Enable Register. As detailed in Section 10, a CPU-specific hard reset or system reset is generated by using the system EPLD CPU Enable Register (Port 871) and the HRESET PAL.

Section 6.2.1.1	**Page 123**	Figure 39 has been changed (see Figure 2 below) to show the EXTHRST# signal output from the system EPLD to the reset logic (shown as an AND gate).

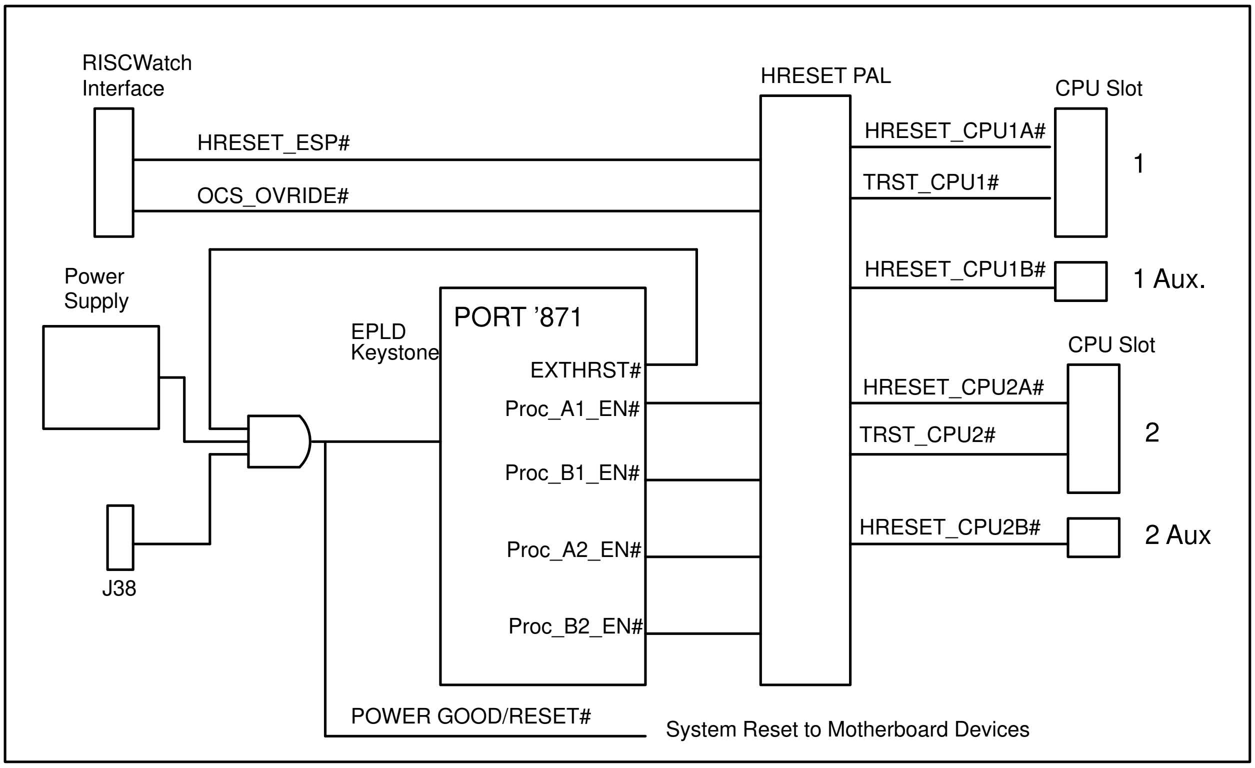

Figure 2. HRESET# Signal Circuit

Section 7.3.1	**Page 140**	The following was added to the second bullet: This mode has not been tested, and is not recommended.
Section 7.5	**Page 140**	In Table 41, the frequency of the Reference crystal for power management controller was changed from 1.8432 MHz to 16 MHz.
Section 10	**Page 165**	There are many changes to this section. Please see release 3.0 of the reference design technical specification for more information.
Section 10.2.11	**Page 177**	There are many changes to this page. The new external hardware reset pulse output EXTHRST# is controlled via this (CPU Enable) register.
Section 10.3	**Page 178**	In Table 57; 1) On p178, change RTC_ALE to RTC_ALE#. 2) On p179, change the pin order assignment of ECS[2:0] from 21, 22, 59 to 59, 22 21. 3) On p179, change the pin order assignment of XD[7:0] from 73, 74, 92, 95, 96, 97, 98, 99 to 73, 92, 95, 96, 97, 74, 98, 99. 4) On p181, change SER_CLKEN# to SER_CLKEN. 5) On p182, change RSVD_IN1 to EXTHRST# (an Output. Also see section 10.2.11). 6) On p182, change RSVD_IN2 to RSVD_IN.
Section 10.4	**Page 183**	The entire EPLD Design Files section has been replaced by the new EPLD design file.

Section 10.3 **Page 199** In Table 58, change:
pin 4 from RSVD_IN1 to EXTHRST#;
pin 15 from IRQ15 to IRQ12;
pin 21 from ECS[2] to ECS [0];
pin 29 from SER_CLKEN# to SER_CLKEN;
pin 41 from RSVD_IN2 to RSVD_IN;
pin 59 from ECS [0] to ECS[2].

Section 12.1.5 **Page 223** In the Workaround section, change 0Ω resistor (R429) to 510Ω resistor.

Section 12.1.8 **Page 224** Under Component Changes, change R768 to R678 and change R769 to R679.

Section 12.1.8 **Page 225** There are two changes to Figure 53. First, the name of the ZC3B PAL changes to ZC3B (and new equations are required – see errata 11). Second, the 100Ω pulldown resistor R894 is incorrectly shown as connecting to both pin 9 and pin 11 of ZC3B. It correctly connects only to pin 11.

Section 12.2.3 **Page 229** There is an error in the ZC3 PAL design file (see Errata 11). Change the name of the PAL from ZC3 to ZC3B (three places). Change the pin definition of pin 15 from:
PIN 15 MASK_PCI_GNT COMB ;COMBINATORIAL to ZP
to:
PIN 15 MASK_PCI_GNT REG ;Registered to ZP

Section 14.5.4 **Page 276** Several of the values in Table 75 will change when upgrading from version 1.x to version 2.0 of the ROM. See release 3.0 of the reference design technical specification for more information.

Section 18.2.2 **Page 329** The section title and the title of Figure 74 change from CPU Card Power Cable to Riser Power Cable. In Figure 74, change:
P2 – Mates with CPU card.
to:
P2 – Mates with Riser.

Section 18.2.30 **Page 346** Change the section title from 3.3v Power Connector J50 to Riser 3.3v Power Connector J50.

Section 20 **Page 380** Make the following changes to the CPU BOM shown inTable 117:

Table 117. Cheetah0 (CPU Card) Bill of Materials

	No	Part Name	Part Number	Ref Des	Qty	Manufacturer Name	Manufacturer Part Number	JEDEC TYPE	Part Description
incorrect	1	604BGANH-SIOC	A123_XX	U1	1	IBM	03H4964-DD1_66MHZ	SBC-256NH	604_DD1_66 MHZ IN BGA
correct	1	604BGANH	64G 4738	U1	1	IBM	IBM25PPC604-BE-133-2	SBC-256NH	PowerPC 604 CPU
incorrect	10	CPUHEATSINK-SIOC		M1	1	SANYO DENKI	REMP5412 H2026	CPUHEATSINK	HEATSINK
correct	10	CPUHEATSINK		M1	1	SANYO DENKI	REMP5412 H2026	CPUHEATSINK	FANSINK
incorrect	20	RESISTOR-33.0,5%	7F7666	R25	1	PANASONIC	ERJ3GSYJ 330V	SMC0603	RESISTOR
correct	20	RESISTOR-33.0,5%	71F7666	R25	1	PANASONIC	ERJ3GSYJ 330V	SMC0603	RESISTOR

The BOMs correspond to the pre–errata PD of the reference design. Changes to the components that are required by the errata in this document and the technical specification are not reflected in the BOMs.

Section 21

No additional errata were found in the schematics.

The schematics correspond to the pre–errata PD of the reference design. Changes to the components and connectivity that are required by the errata in this document and the technical specification are not reflected in the schematics.

Section 22

An updated 604 CPU Hardware Specification and MPIC Data Sheet are included in the release 3.0 Technical Specification.

PowerPC

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Document Number: MPRZAPESU-01