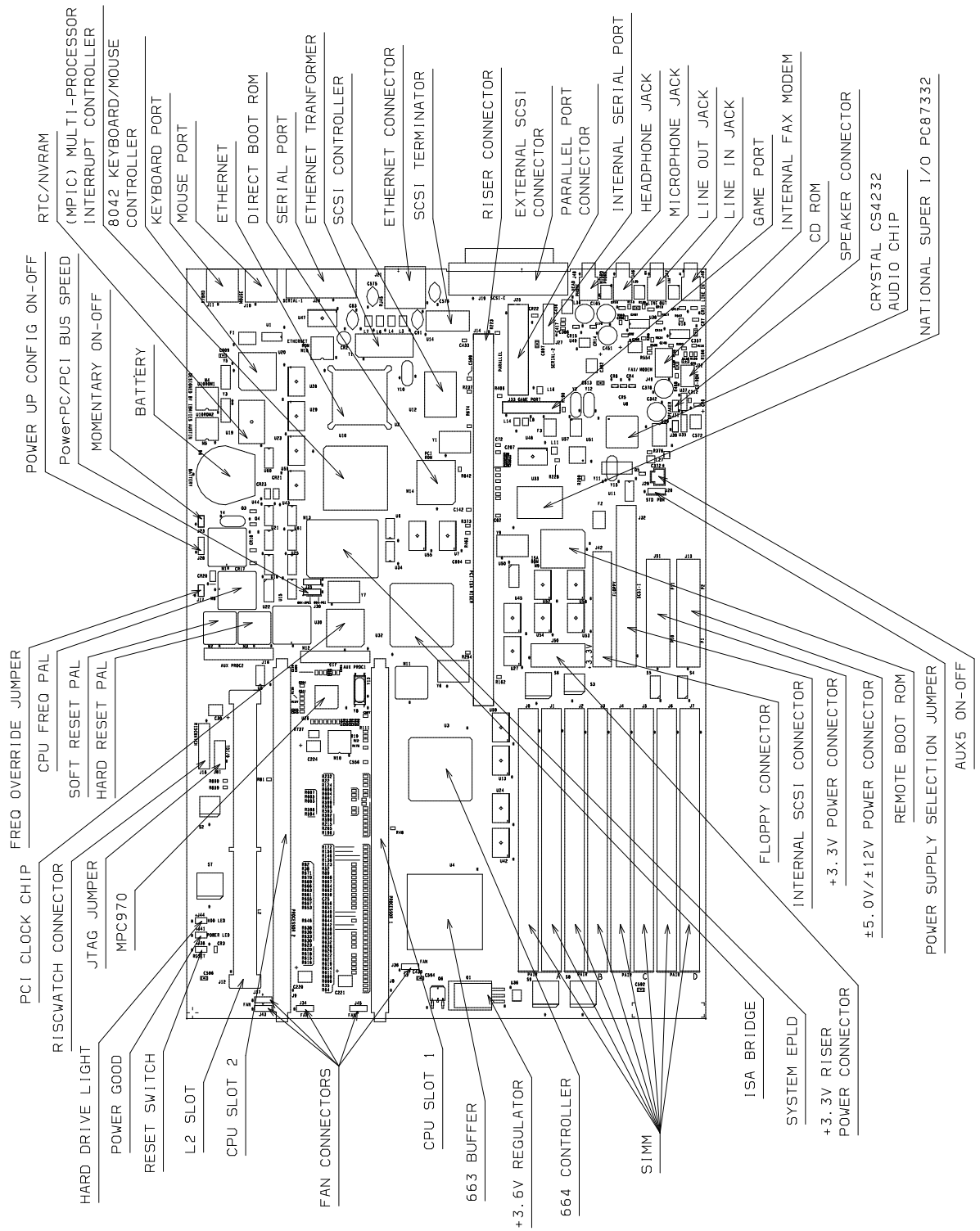
Section 21
Schematics

This section contains the schematics of the reference design and a component placement drawing of the reference board.

The schematics are numbered separately from the rest of the reference design technical specification.

Reference Board Component Placement



PowerPC 604
SMP REFERENCE
BOARD SCHEMATICS

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IBM			
DRAWING DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 1 OF 64

MOTHERBOARD

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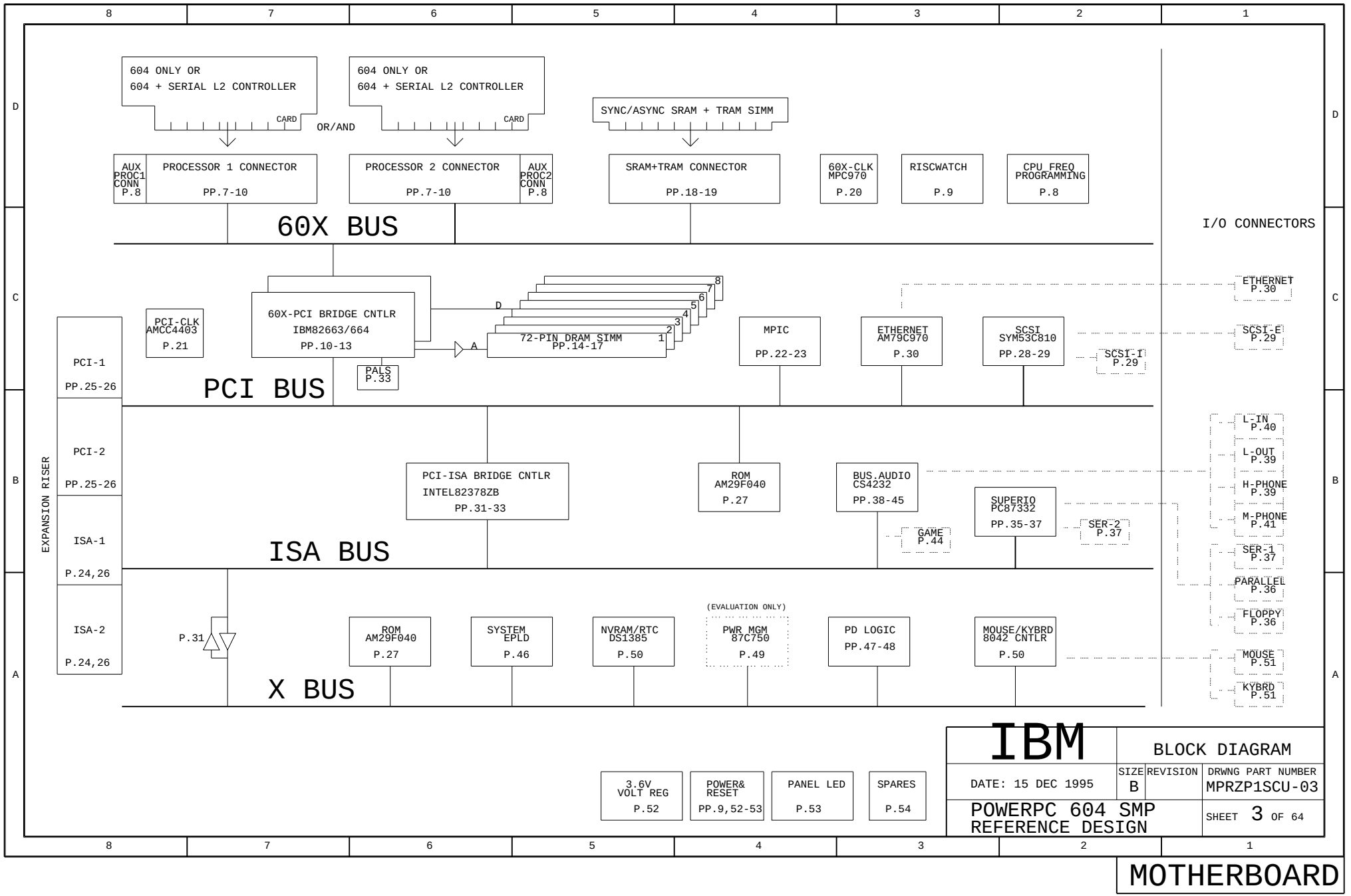
604 ONLY OR
604 + SERIAL L2 CONTROLLER
CARD
OR/AND
604 ONLY OR
604 + SERIAL L2 CONTROLLER
CARD
SYNC/ASYNC SRAM + TRAM SIMM
AUX PROC1 CONN P.8
PROCESSOR 1 CONNECTOR
PP.7-10
PROCESSOR 2 CONNECTOR
PP.7-10
AUX PROC2 CONN P.8
SRAM+TRAM CONNECTOR
PP.18-19
60X-CLK MPC970
P.20
RISCWATCH
P.9
CPU FREQ PROGRAMMING
P.8
60X BUS
I/O CONNECTORS
PCI-CLK AMCC4403
P.21
60X-PCI BRIDGE CNTLR
IBM82663/664
PP.10-13
PALS
P.33
72-PIN DRAM SIMM
PP.14-17
MPIC
PP.22-23
ETHERNET AM79C970
P.30
SCSI SYM53C810
PP.28-29
ETHERNET
P.30
SCSI-E
P.29
SCSI-I
P.29
PCI-1
PP.25-26
PCI-2
PP.25-26
ISA-1
P.24,26
ISA-2
P.24,26
EXPANSION RISER
PCI BUS
PCI-ISA BRIDGE CNTLR
INTEL82378ZB
PP.31-33
ROM
AM29F040
P.27
BUS.AUDIO
CS4232
PP.38-45
SUPERIO
PC87332
PP.35-37
GAME
P.44
SER-2
P.37
L-IN
P.40
L-OUT
P.39
H-PHONE
P.39
M-PHONE
P.41
SER-1
P.37
PARALLEL
P.36
FLOPPY
P.36
ISA BUS
P.31
ROM
AM29F040
P.27
SYSTEM
EPLD
P.46
NVRAM/RTC
DS1385
P.50
(EVALUATION ONLY)
PWR MGM
87C750
P.49
PD LOGIC
PP.47-48
MOUSE/KYBRD
8042 CNTLR
P.50
MOUSE
P.51
KYBRD
P.51
X BUS
3.6V VOLT REG
P.52
POWER& RESET
PP.9,52-53
PANEL LED
P.53
SPARES
P.54
IBM
BLOCK DIAGRAM
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER
MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
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IBM

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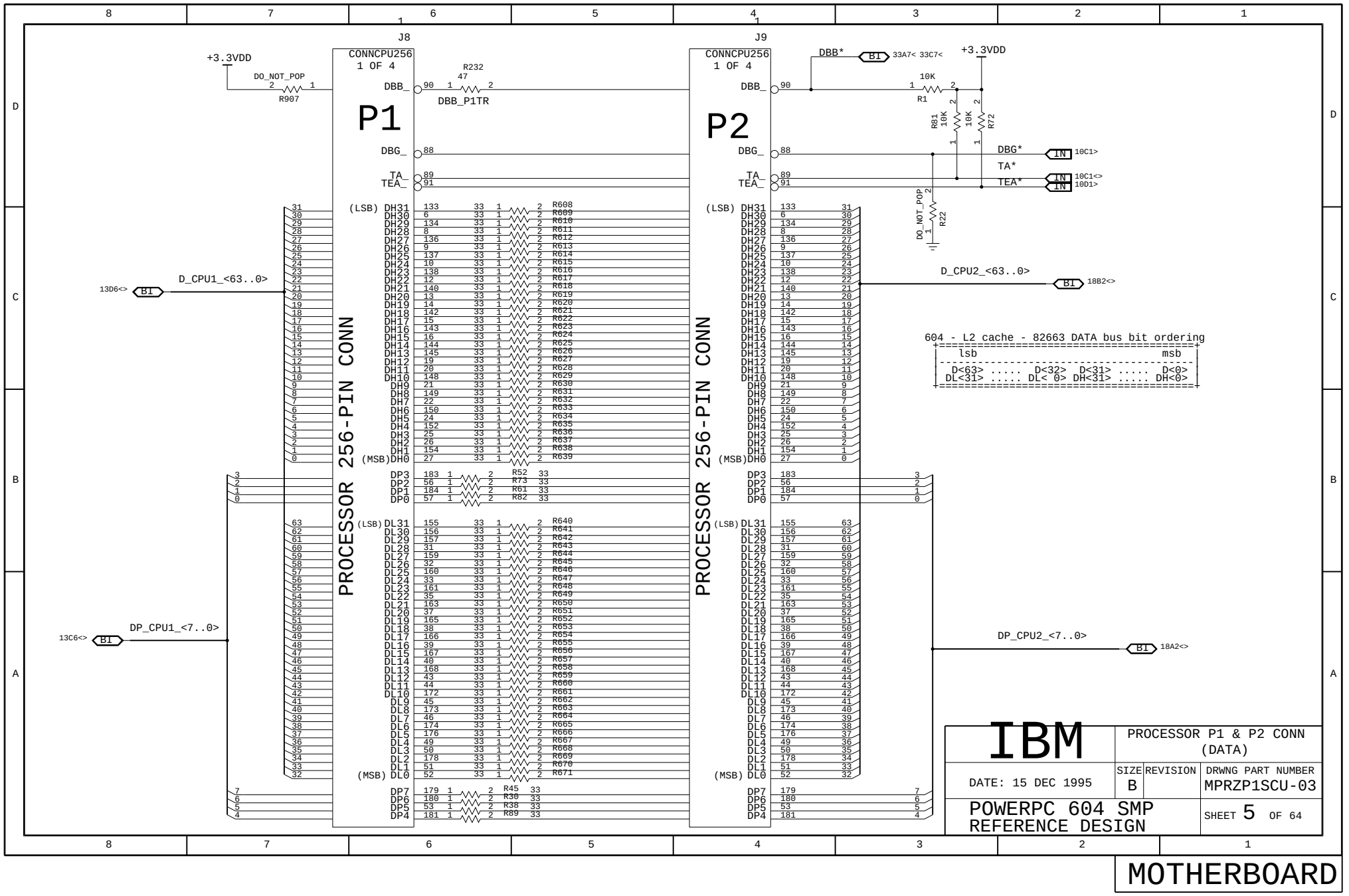
J8
CONNCPU256
1 OF 4
P1
PROCESSOR 256-PIN CONN
J9
CONNCPU256
1 OF 4
P2
PROCESSOR 256-PIN CONN
+3.3VDD
DO_NOT_POP
R907
R232
47
DBB_P1TR
DBB_
DBG_
TA_
TEA_
D_CPU1_<63..0>
13D6<>
B1
DP_CPU1_<7..0>
13C6<>
DBB*
33A7< 33C7<
10K
R1
R81
R72
DBG*
TA*
TEA*
10C1>
10C1<>
10D1>
R22
D_CPU2_<63..0>
18B2<>
DP_CPU2_<7..0>
18A2<>
604 - L2 cache - 82663 DATA bus bit ordering
lsb
msb
D<63> ..... D<32> D<31> ..... D<0>
DL<31> ..... DL< 0> DH<31> ..... DH<0>
IBM
PROCESSOR P1 & P2 CONN
(DATA)
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER
MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 5 OF 64
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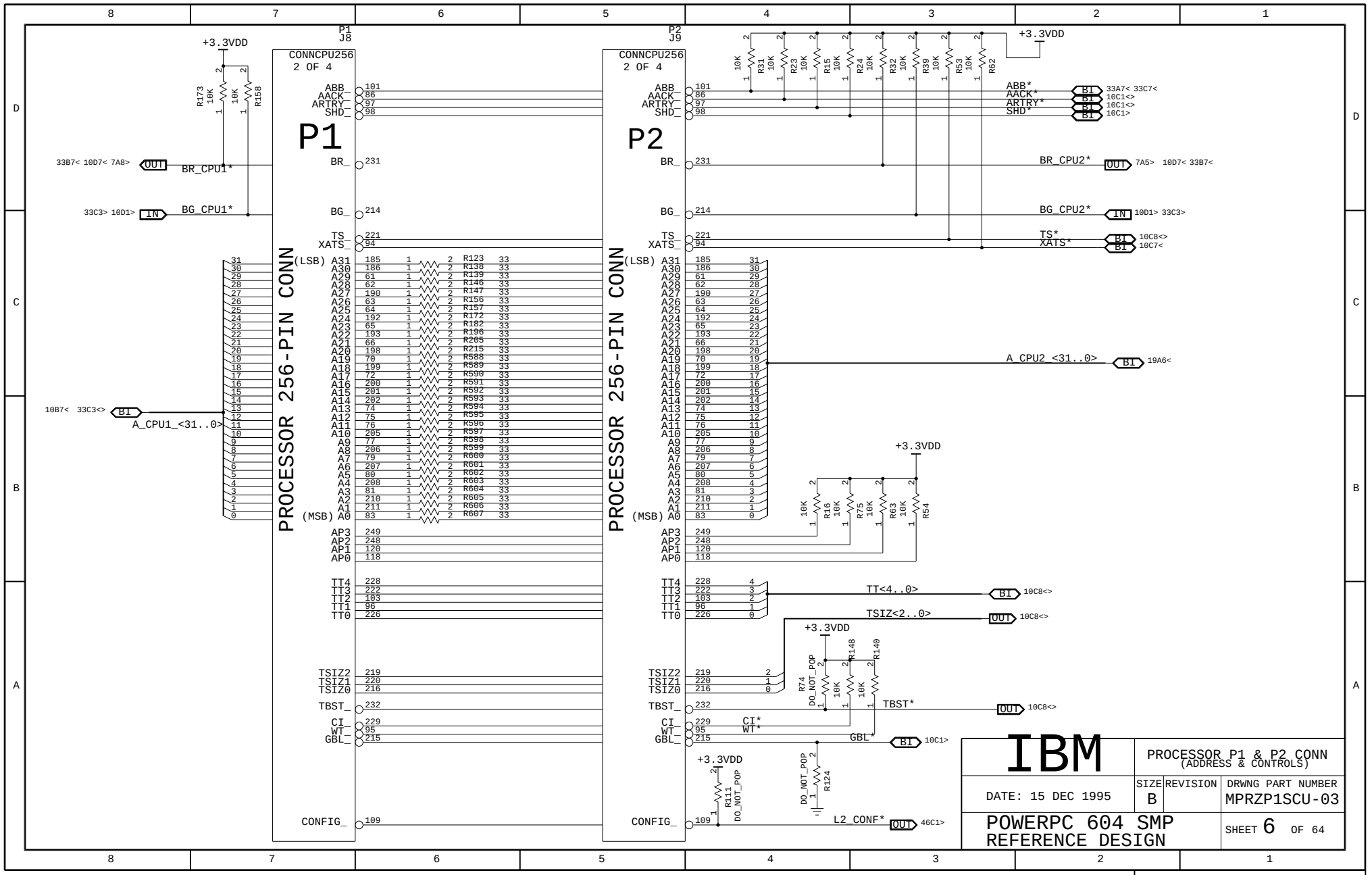
P1
J8
CONNCPU256
2 OF 4
PROCESSOR 256-PIN CONN
P2
J9
CONNCPU256
2 OF 4
PROCESSOR 256-PIN CONN
+3.3VDD
BR_CPU1*
BG_CPU1*
A_CPU1_<31..0>
BR_CPU2*
BG_CPU2*
A_CPU2 <31..0>
TS*
XATS*
ABB*
AACK*
ARTRY*
SHD*
TT<4..0>
TSIZ<2..0>
TBST*
CI*
WT*
GBL*
L2_CONF*
DO_NOT_POP
IBM
PROCESSOR P1 & P2 CONN
(ADDRESS & CONTROLS)
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
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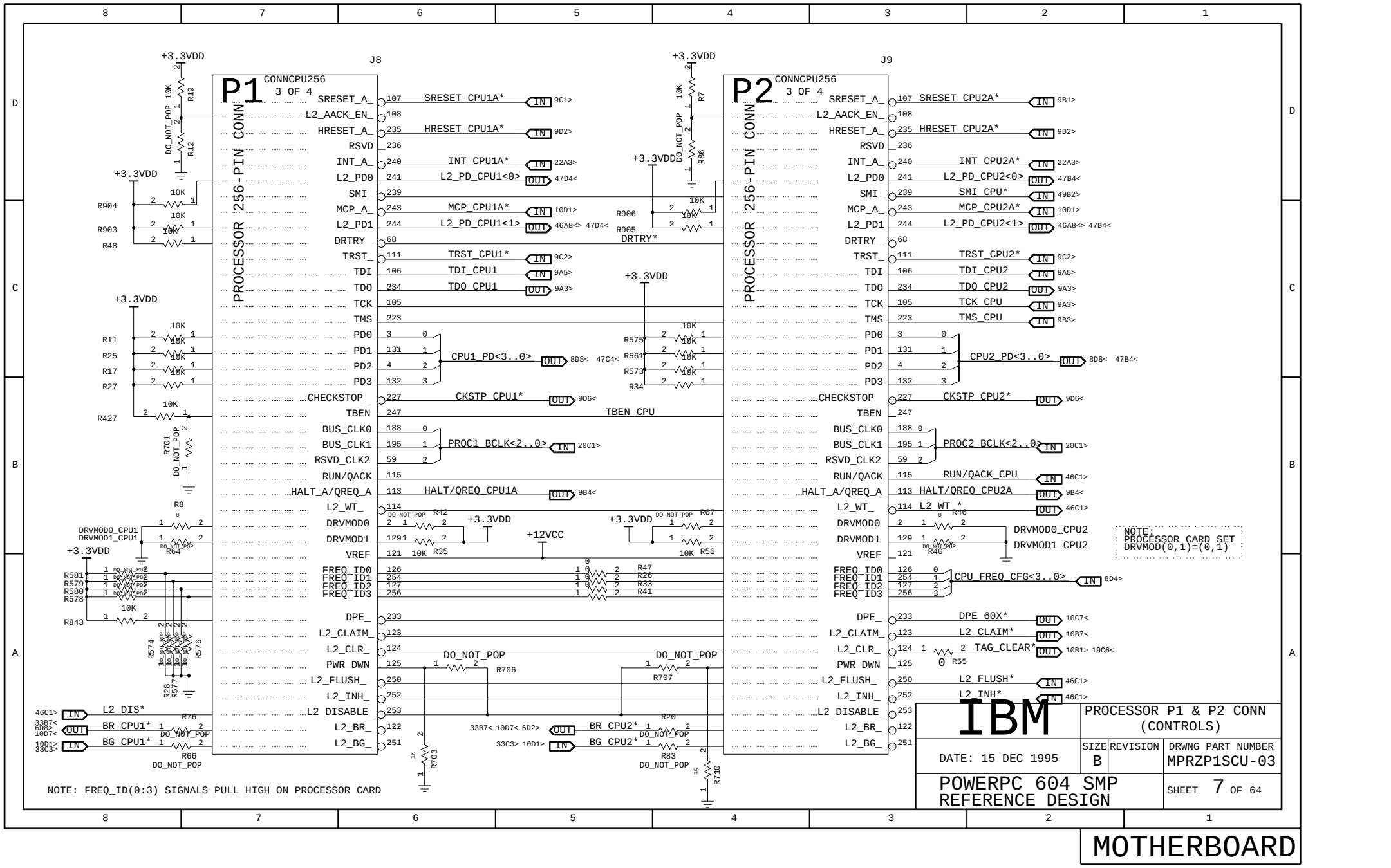
MOTHERBOARD


P1
CONNCPU256
3 OF 4
PROCESSOR 256-PIN CONN
J8
P2
CONNCPU256
3 OF 4
PROCESSOR 256-PIN CONN
J9
+3.3VDD
+12VCC
SRESET_A_
L2_AACK_EN_
HRESET_A_
RSVD
INT_A_
L2_PD0
SMI_
MCP_A_
L2_PD1
DRTRY_
TRST_
TDI
TDO
TCK
TMS
PD0
PD1
PD2
PD3
CHECKSTOP_
TBEN
BUS_CLK0
BUS_CLK1
RSVD_CLK2
RUN/QACK
HALT_A/QREQ_A
L2_WT_
DRVMOD0
DRVMOD1
VREF
FREQ_ID0
FREQ_ID1
FREQ_ID2
FREQ_ID3
DPE_
L2_CLAIM_
L2_CLR_
PWR_DWN
L2_FLUSH_
L2_INH_
L2_DISABLE_
L2_BR_
L2_BG_
SRESET_CPU1A*
HRESET_CPU1A*
INT_CPU1A*
L2_PD_CPU1<0>
MCP_CPU1A*
L2_PD_CPU1<1>
DRTRY*
TRST_CPU1*
TDI_CPU1
TDO_CPU1
CPU1_PD<3..0>
CKSTP_CPU1*
TBEN_CPU
PROC1_BCLK<2..0>
HALT/QREQ_CPU1A
DRVMOD0_CPU1
DRVMOD1_CPU1
L2_DIS*
BR_CPU1*
BG_CPU1*
BR_CPU2*
BG_CPU2*
SRESET_CPU2A*
HRESET_CPU2A*
INT_CPU2A*
L2_PD_CPU2<0>
SMI_CPU*
MCP_CPU2A*
L2_PD_CPU2<1>
TRST_CPU2*
TDI_CPU2
TDO_CPU2
TCK_CPU
TMS_CPU
CPU2_PD<3..0>
CKSTP_CPU2*
PROC2_BCLK<2..0>
RUN/QACK_CPU
HALT/QREQ_CPU2A
L2_WT_*
DRVMOD0_CPU2
DRVMOD1_CPU2
CPU_FREQ_CFG<3..0>
DPE_60X*
L2_CLAIM*
TAG_CLEAR*
L2_FLUSH*
L2_INH*
DO_NOT_POP
NOTE: PROCESSOR CARD SET DRVMOD(0,1)=(0,1)
NOTE: FREQ_ID(0:3) SIGNALS PULL HIGH ON PROCESSOR CARD
IBM
PROCESSOR P1 & P2 CONN (CONTROLS)
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN
SHEET 7 OF 64
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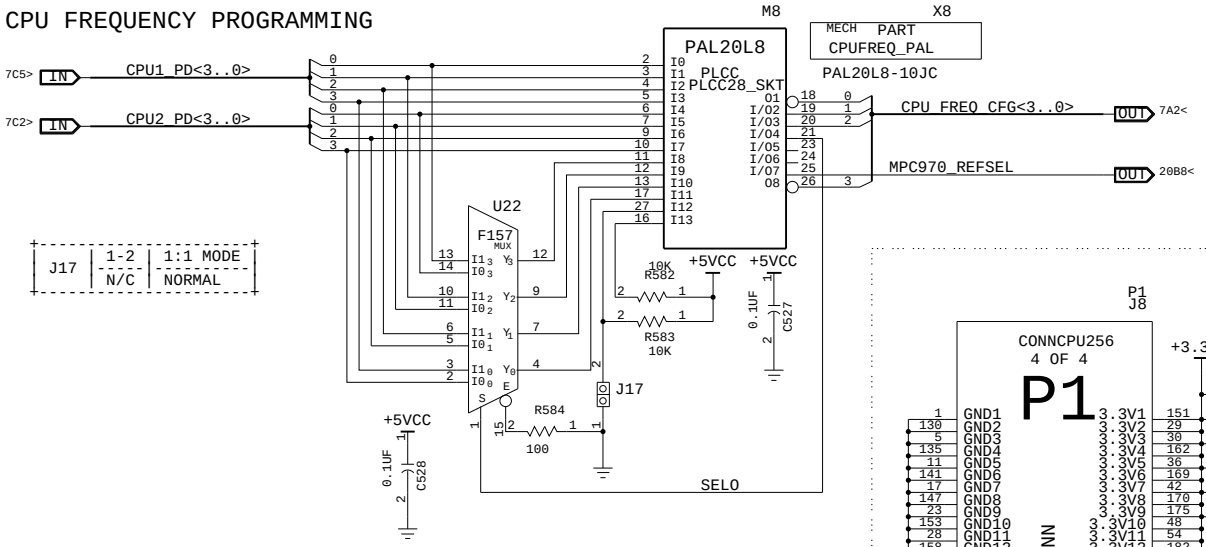
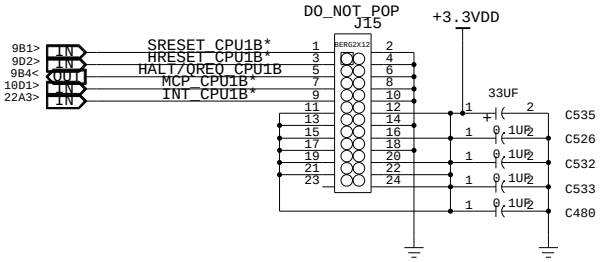
CPU FREQUENCY PROGRAMMING

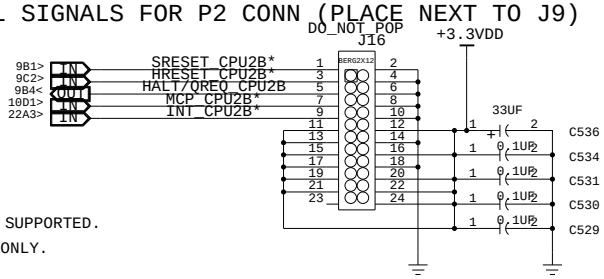


J17	1-2	1:1 MODE
	N/C	NORMAL

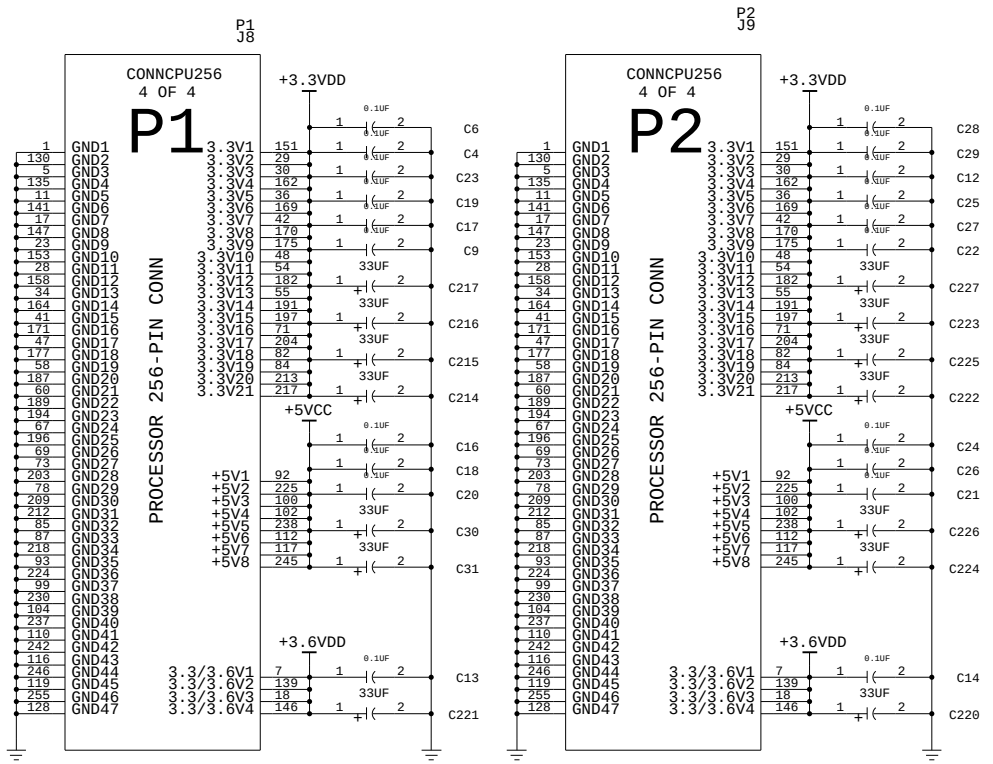
AUX CONTROL SIGNALS FOR P1 CONN (PLACE NEXT TO J8)



AUX CONTROL SIGNALS FOR P2 CONN (PLACE NEXT TO J9)



J15 & J16 ARE NOT SUPPORTED.
FOR EVALUATION ONLY.



IBM	PROCESSOR P1 & P2 CONN CPU FREQUENCY SELECT LOGIC		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
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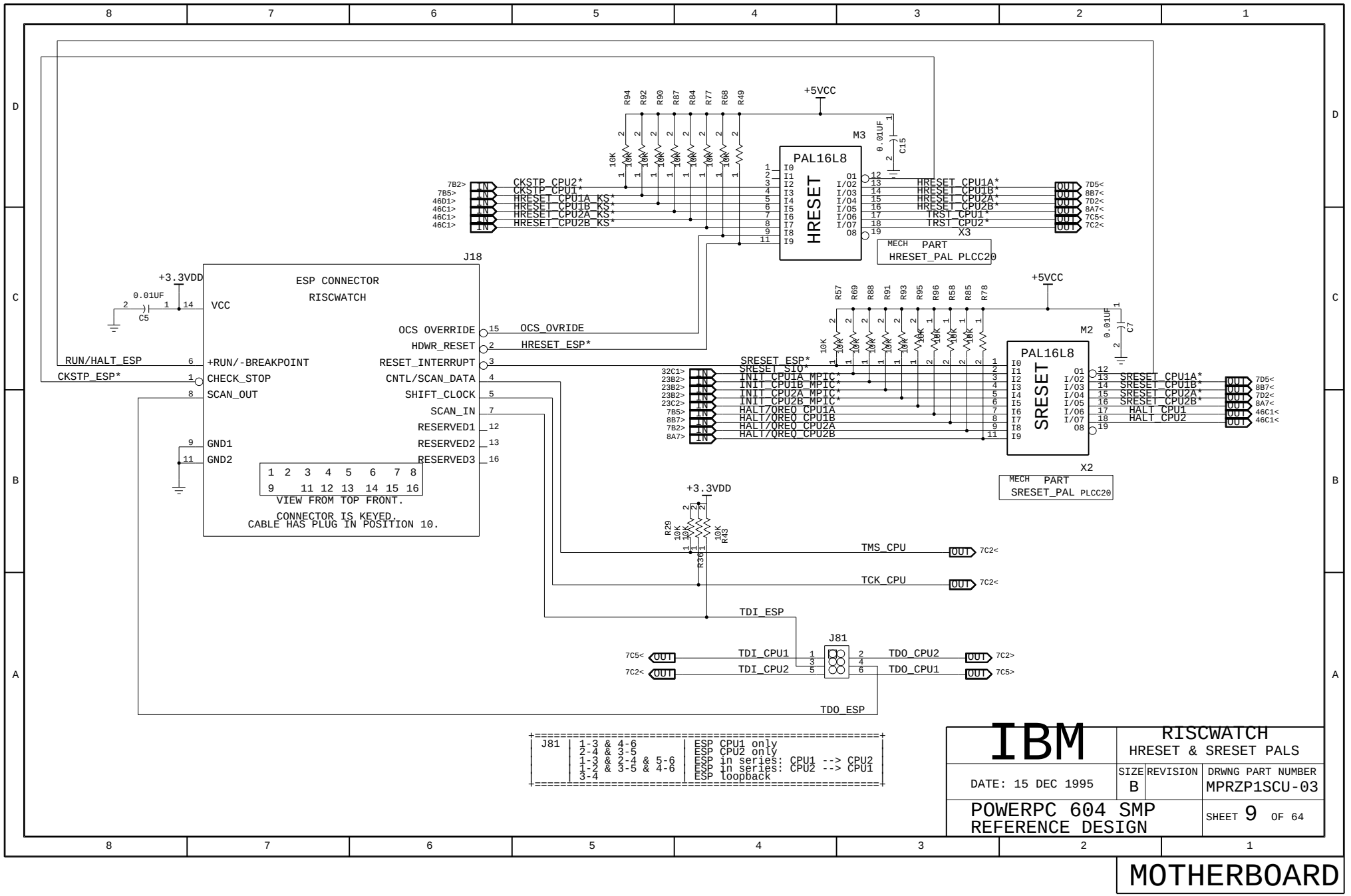

J81		
	1-3 & 4-6	ESP CPU1 only
	2-4 & 3-5	ESP CPU2 only
	1-3 & 2-4 & 5-6	ESP in series: CPU1 --> CPU2
	1-2 & 3-5 & 4-6	ESP in series: CPU2 --> CPU1
	3-4	ESP loopback

IBM

RISCWATCH
HRESET & SRESET PALS

DATE: 15 DEC 1995

SIZE	REVISION	DRWNG PART NUMBER
B		MPRZP1SCU-03

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REFERENCE DESIGN

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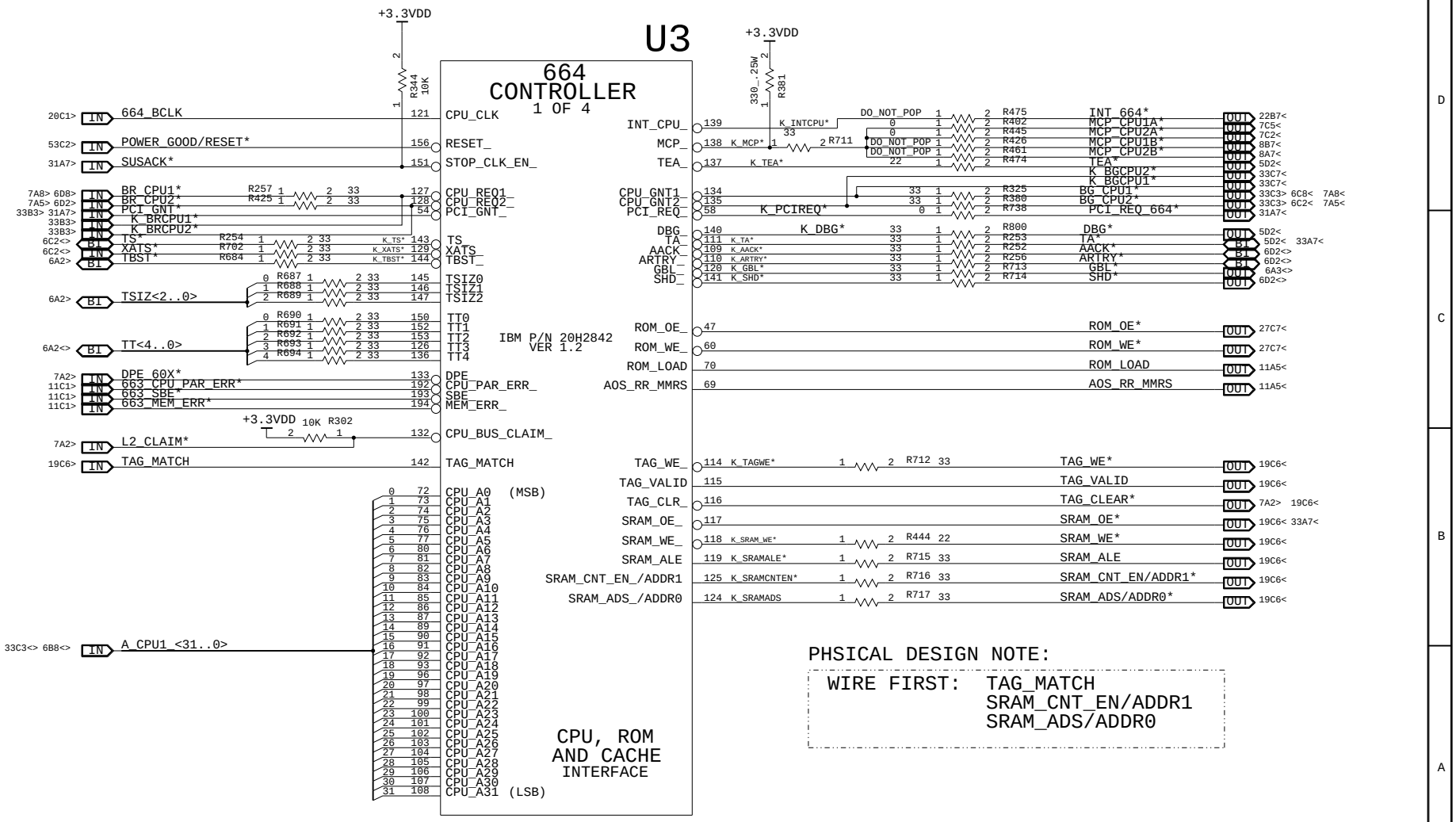

PHSICAL DESIGN NOTE:

WIRE FIRST: TAG_MATCH
SRAM_CNT_EN/ADDR1
SRAM_ADS/ADDR0

PHYSICAL DESIGN NOTE:

ALL SERIES RESISTORS MUST BE PLACED AS CLOSE TO 664 AS POSSIBLE.
0 OHM PLACEMENT IS NOT CRITICAL.

IBM

664 CONTROLLER
CENTRAL CONTROL PORTION

DATE: 15 DEC 1995

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POWERPC 604 SMP
REFERENCE DESIGN

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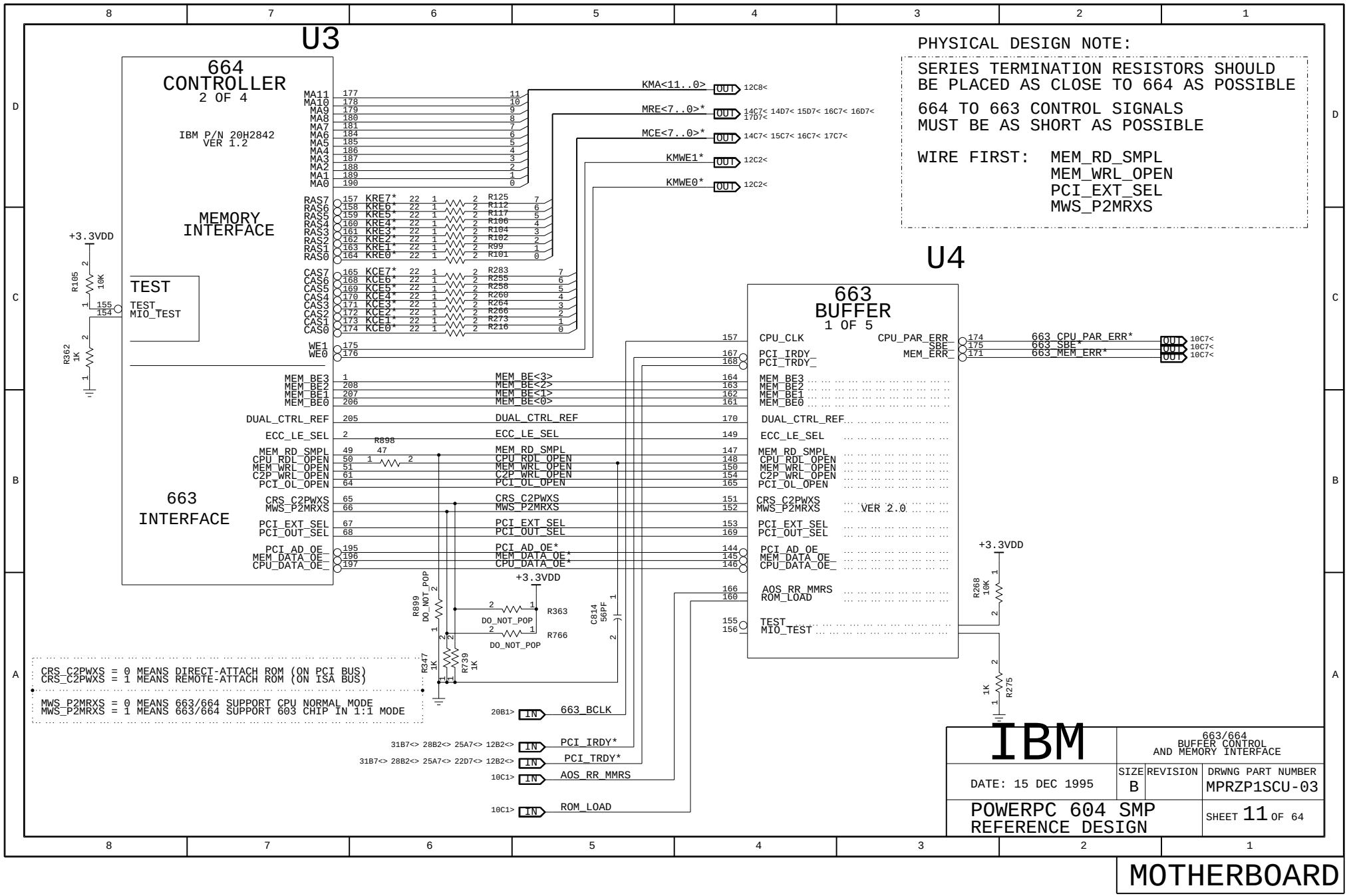
U3
664
CONTROLLER
2 OF 4
IBM P/N 20H2842
VER 1.2
MEMORY
INTERFACE
663
INTERFACE
TEST
TEST
MIO_TEST
U4
663
BUFFER
1 OF 5
VER 2.0
PHYSICAL DESIGN NOTE:
SERIES TERMINATION RESISTORS SHOULD
BE PLACED AS CLOSE TO 664 AS POSSIBLE
664 TO 663 CONTROL SIGNALS
MUST BE AS SHORT AS POSSIBLE
WIRE FIRST: MEM_RD_SMPL
MEM_WRL_OPEN
PCI_EXT_SEL
MWS_P2MRXS
CRS_C2PWXS = 0 MEANS DIRECT-ATTACH ROM (ON PCI BUS)
CRS_C2PWXS = 1 MEANS REMOTE-ATTACH ROM (ON ISA BUS)
MWS_P2MRXS = 0 MEANS 663/664 SUPPORT CPU NORMAL MODE
MWS_P2MRXS = 1 MEANS 663/664 SUPPORT 603 CHIP IN 1:1 MODE
+3.3VDD
DO_NOT_POP
663_BCLK
PCI_IRDY*
PCI_TRDY*
AOS_RR_MMRS
ROM_LOAD
IBM
663/664
BUFFER CONTROL
AND MEMORY INTERFACE
DATE: 15 DEC 1995
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REVISION
DRWNG PART NUMBER
MPRZP1SCU-03
POWERPC 604 SMP
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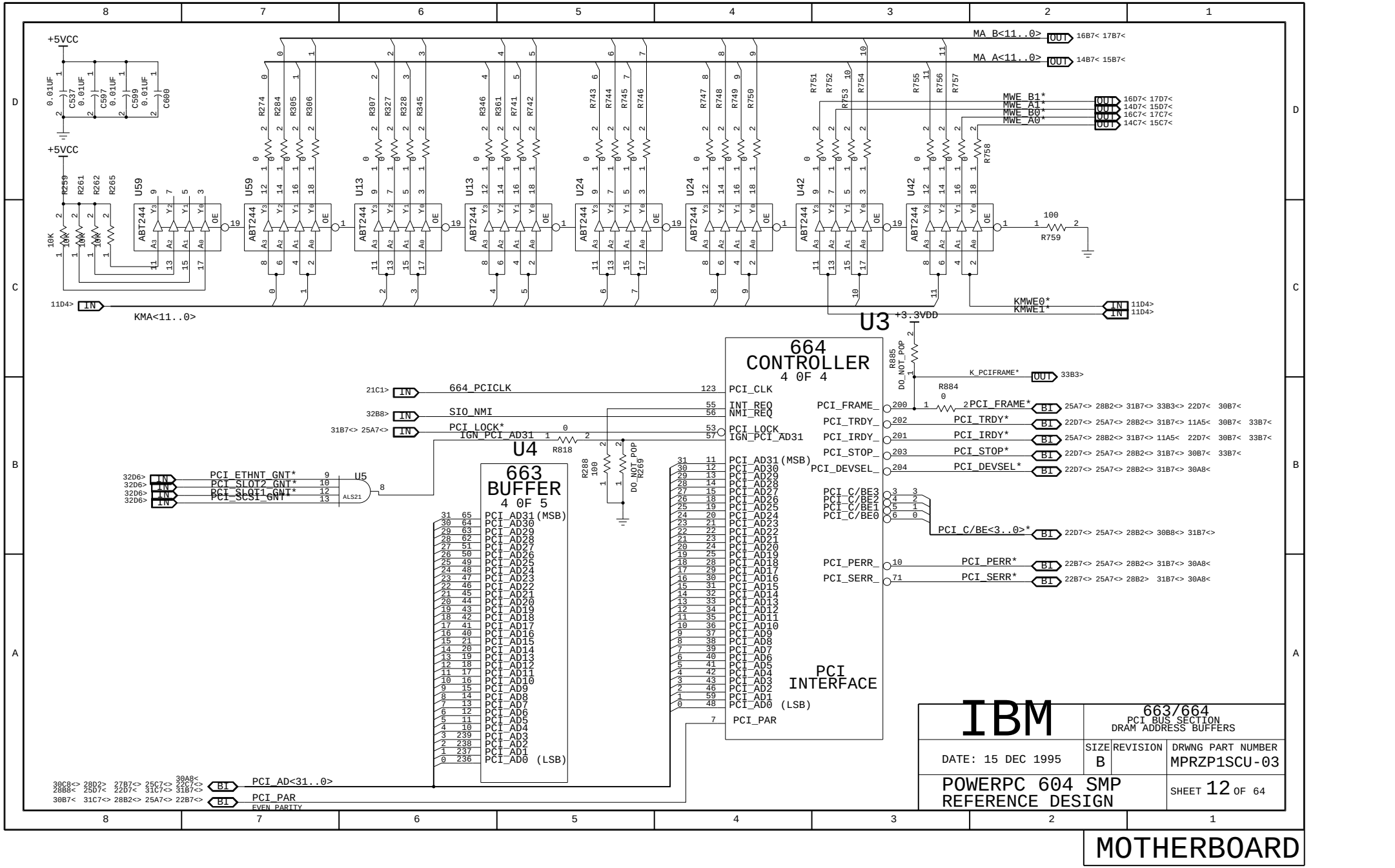

IBM	663/664 PCI BUS SECTION DRAM ADDRESS BUFFERS	
DATE: 15 DEC 1995	SIZE B	REVISION / DRWNG PART NUMBER MPRZP1SCU-03
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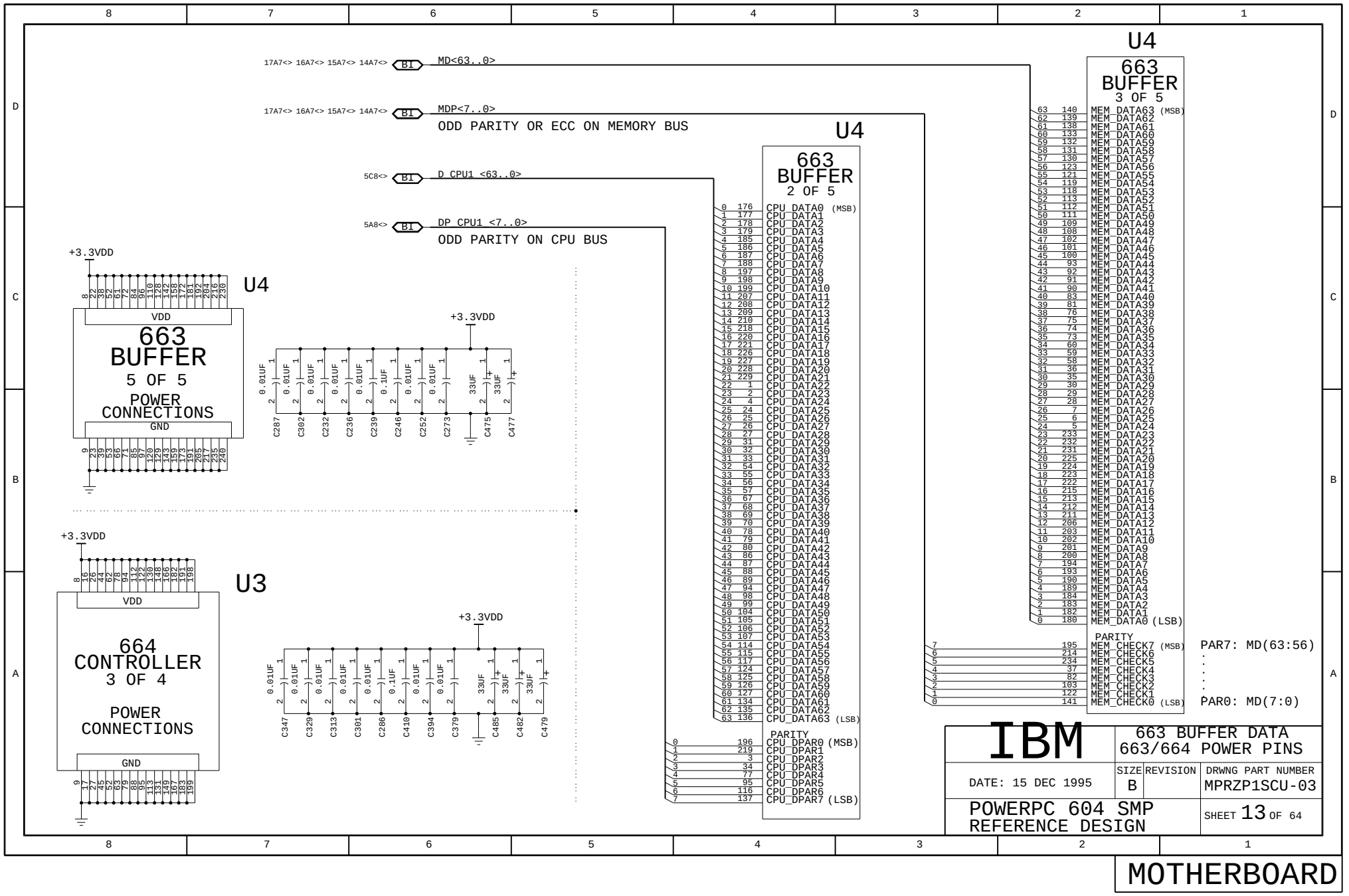
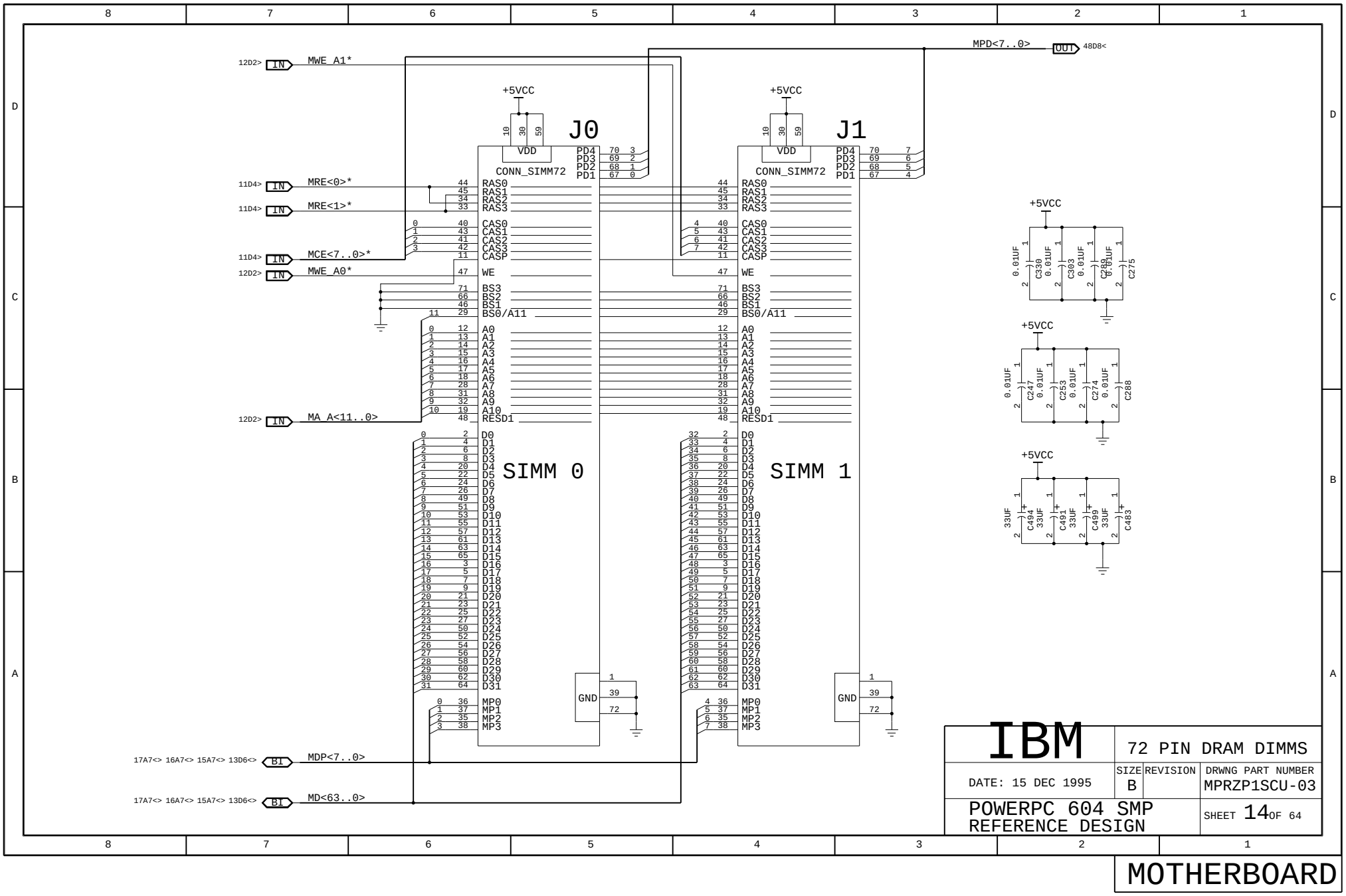

MD<63..0>
MDP<7..0>
ODD PARITY OR ECC ON MEMORY BUS
D_CPU1 <63..0>
DP_CPU1 <7..0>
ODD PARITY ON CPU BUS
U4
663 BUFFER 3 OF 5
MEM_DATA63 (MSB)
MEM_DATA62
MEM_DATA61
MEM_DATA60
MEM_DATA59
MEM_DATA58
MEM_DATA57
MEM_DATA56
MEM_DATA55
MEM_DATA54
MEM_DATA53
MEM_DATA52
MEM_DATA51
MEM_DATA50
MEM_DATA49
MEM_DATA48
MEM_DATA47
MEM_DATA46
MEM_DATA45
MEM_DATA44
MEM_DATA43
MEM_DATA42
MEM_DATA41
MEM_DATA40
MEM_DATA39
MEM_DATA38
MEM_DATA37
MEM_DATA36
MEM_DATA35
MEM_DATA34
MEM_DATA33
MEM_DATA32
MEM_DATA31
MEM_DATA30
MEM_DATA29
MEM_DATA28
MEM_DATA27
MEM_DATA26
MEM_DATA25
MEM_DATA24
MEM_DATA23
MEM_DATA22
MEM_DATA21
MEM_DATA20
MEM_DATA19
MEM_DATA18
MEM_DATA17
MEM_DATA16
MEM_DATA15
MEM_DATA14
MEM_DATA13
MEM_DATA12
MEM_DATA11
MEM_DATA10
MEM_DATA9
MEM_DATA8
MEM_DATA7
MEM_DATA6
MEM_DATA5
MEM_DATA4
MEM_DATA3
MEM_DATA2
MEM_DATA1
MEM_DATA0 (LSB)
PARITY
MEM_CHECK7 (MSB)
MEM_CHECK6
MEM_CHECK5
MEM_CHECK4
MEM_CHECK3
MEM_CHECK2
MEM_CHECK1
MEM_CHECK0 (LSB)
PAR7: MD(63:56)
PAR0: MD(7:0)
U4
663 BUFFER 2 OF 5
CPU_DATA0 (MSB)
CPU_DATA1
CPU_DATA2
CPU_DATA3
CPU_DATA4
CPU_DATA5
CPU_DATA6
CPU_DATA7
CPU_DATA8
CPU_DATA9
CPU_DATA10
CPU_DATA11
CPU_DATA12
CPU_DATA13
CPU_DATA14
CPU_DATA15
CPU_DATA16
CPU_DATA17
CPU_DATA18
CPU_DATA19
CPU_DATA20
CPU_DATA21
CPU_DATA22
CPU_DATA23
CPU_DATA24
CPU_DATA25
CPU_DATA26
CPU_DATA27
CPU_DATA28
CPU_DATA29
CPU_DATA30
CPU_DATA31
CPU_DATA32
CPU_DATA33
CPU_DATA34
CPU_DATA35
CPU_DATA36
CPU_DATA37
CPU_DATA38
CPU_DATA39
CPU_DATA40
CPU_DATA41
CPU_DATA42
CPU_DATA43
CPU_DATA44
CPU_DATA45
CPU_DATA46
CPU_DATA47
CPU_DATA48
CPU_DATA49
CPU_DATA50
CPU_DATA51
CPU_DATA52
CPU_DATA53
CPU_DATA54
CPU_DATA55
CPU_DATA56
CPU_DATA57
CPU_DATA58
CPU_DATA59
CPU_DATA60
CPU_DATA61
CPU_DATA62
CPU_DATA63 (LSB)
PARITY
CPU_DPAR0 (MSB)
CPU_DPAR1
CPU_DPAR2
CPU_DPAR3
CPU_DPAR4
CPU_DPAR5
CPU_DPAR6
CPU_DPAR7 (LSB)
U4
663 BUFFER 5 OF 5
POWER CONNECTIONS
VDD
GND
+3.3VDD
0.01UF
0.1UF
33UF
C287
C302
C232
C236
C239
C246
C252
C273
C475
C477
U3
664 CONTROLLER 3 OF 4
POWER CONNECTIONS
VDD
GND
+3.3VDD
0.01UF
0.1UF
33UF
C347
C329
C313
C301
C286
C410
C394
C379
C485
C482
C479
IBM
663 BUFFER DATA
663/664 POWER PINS
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 13 OF 64
MOTHERBOARD



IBM	72 PIN DRAM DIMMS	
DATE: 15 DEC 1995	SIZE B / REVISION	DRWNG PART NUMBER MPRZP1SCU-03
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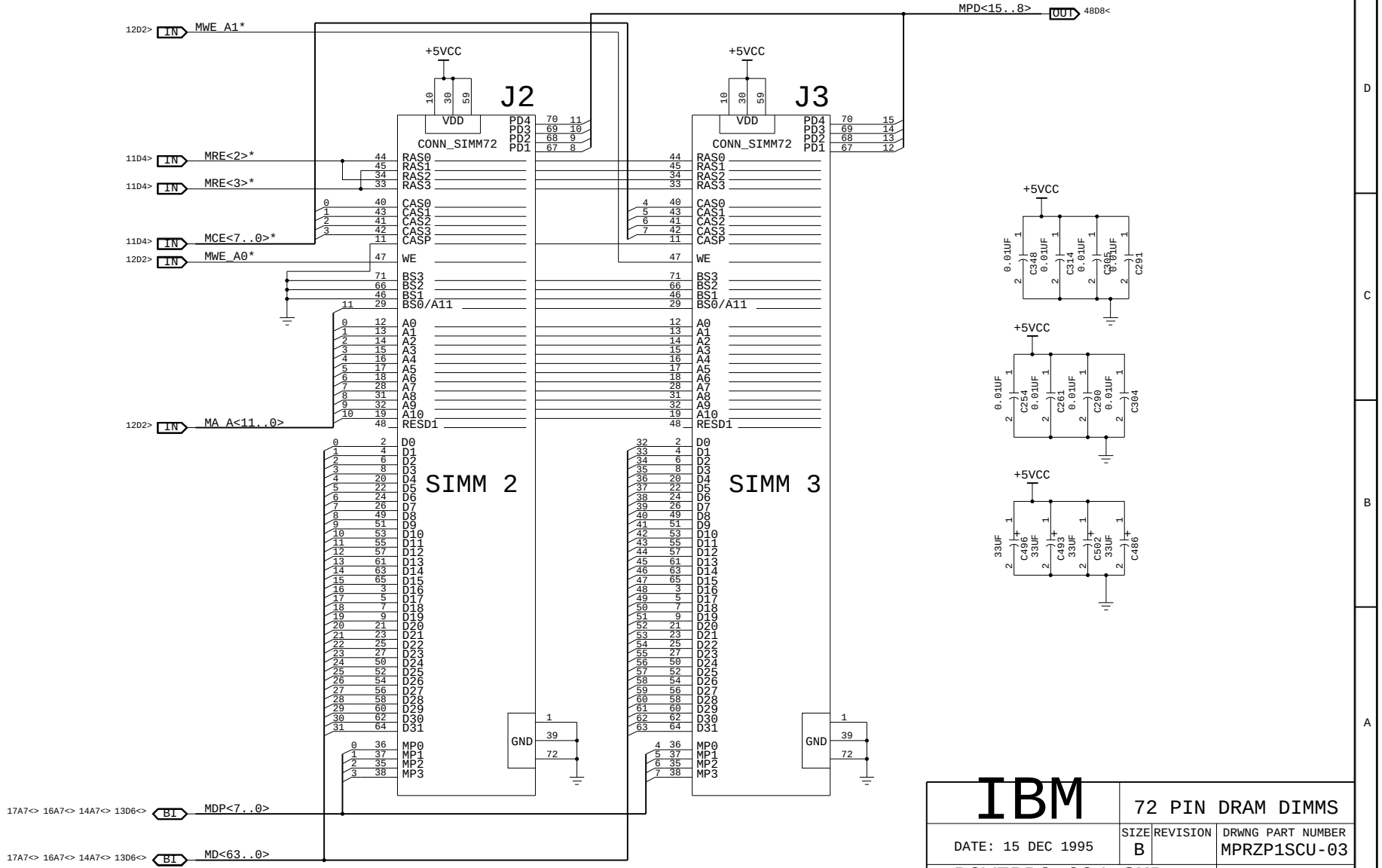
MWE_A1*
MPD<15..8>
+5VCC
J2
J3
VDD
CONN_SIMM72
PD4
PD3
PD2
PD1
MRE<2>*
MRE<3>*
MCE<7..0>*
MWE_A0*
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
CASP
WE
BS3
BS2
BS1
BS0/A11
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
RESD1
MA A<11..0>
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
MP0
MP1
MP2
MP3
SIMM 2
SIMM 3
GND
0.01UF
33UF
MDP<7..0>
MD<63..0>
IBM
72 PIN DRAM DIMMS
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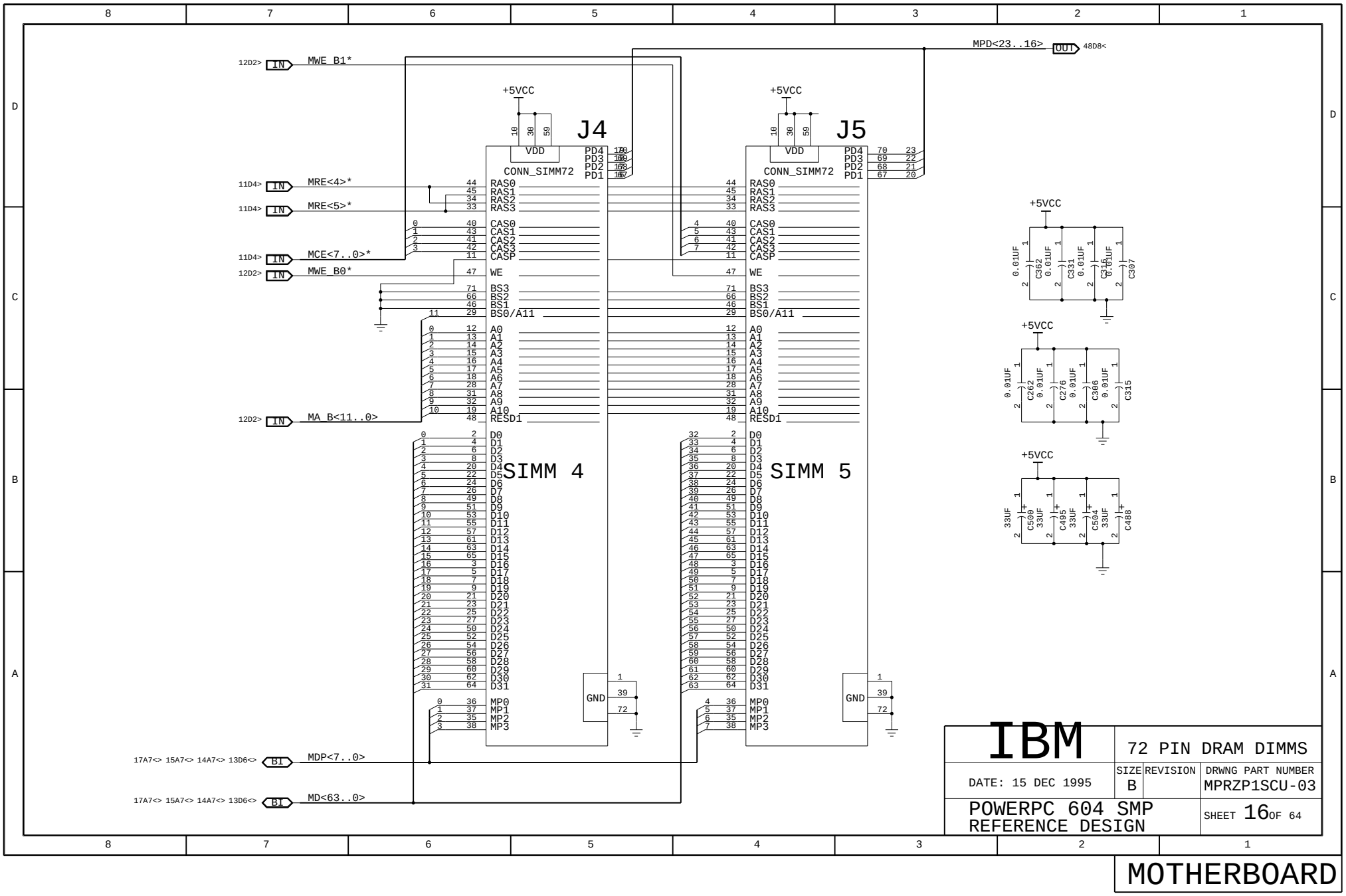
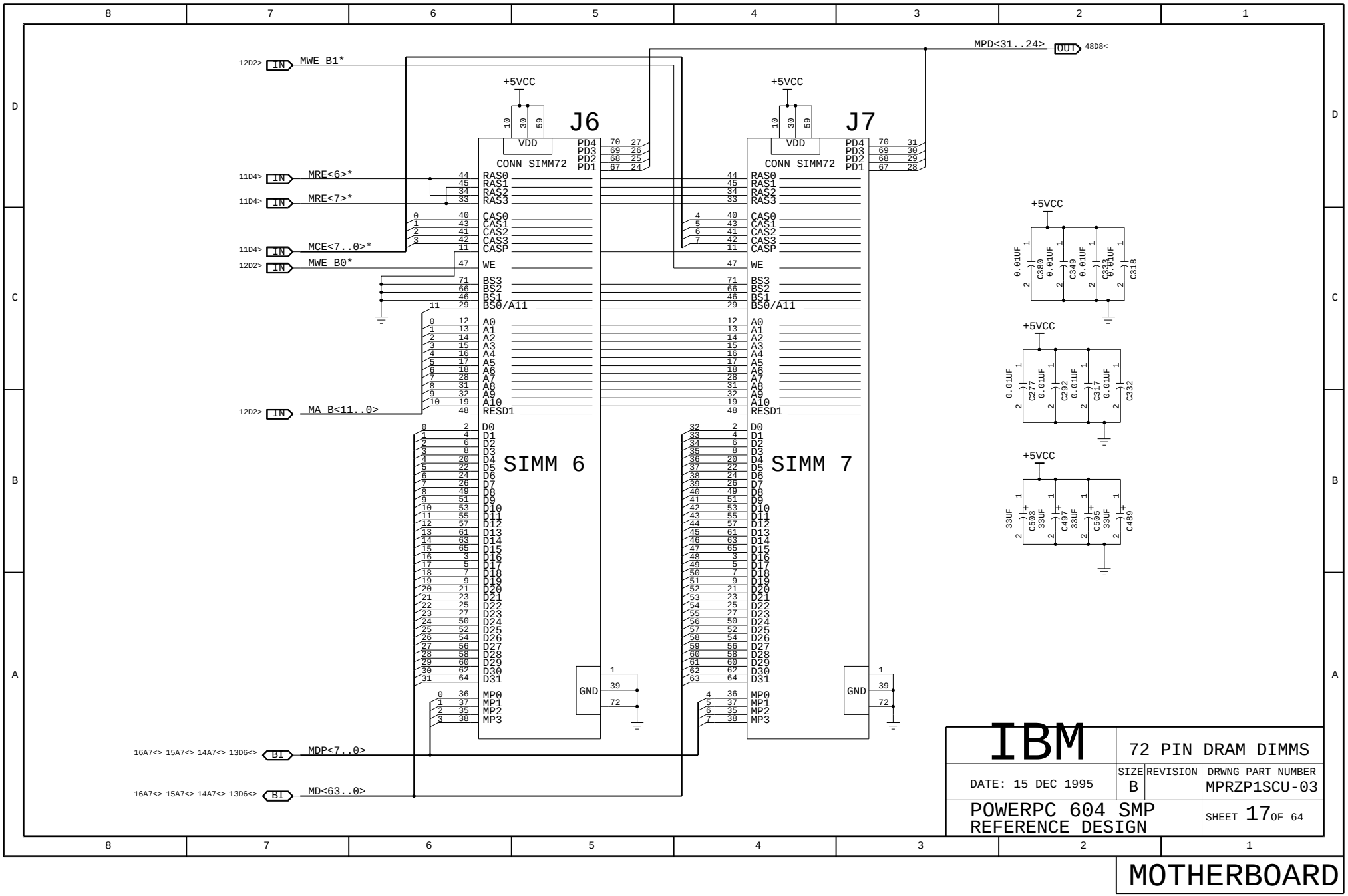
SHEET 15 OF 64
MOTHERBOARD



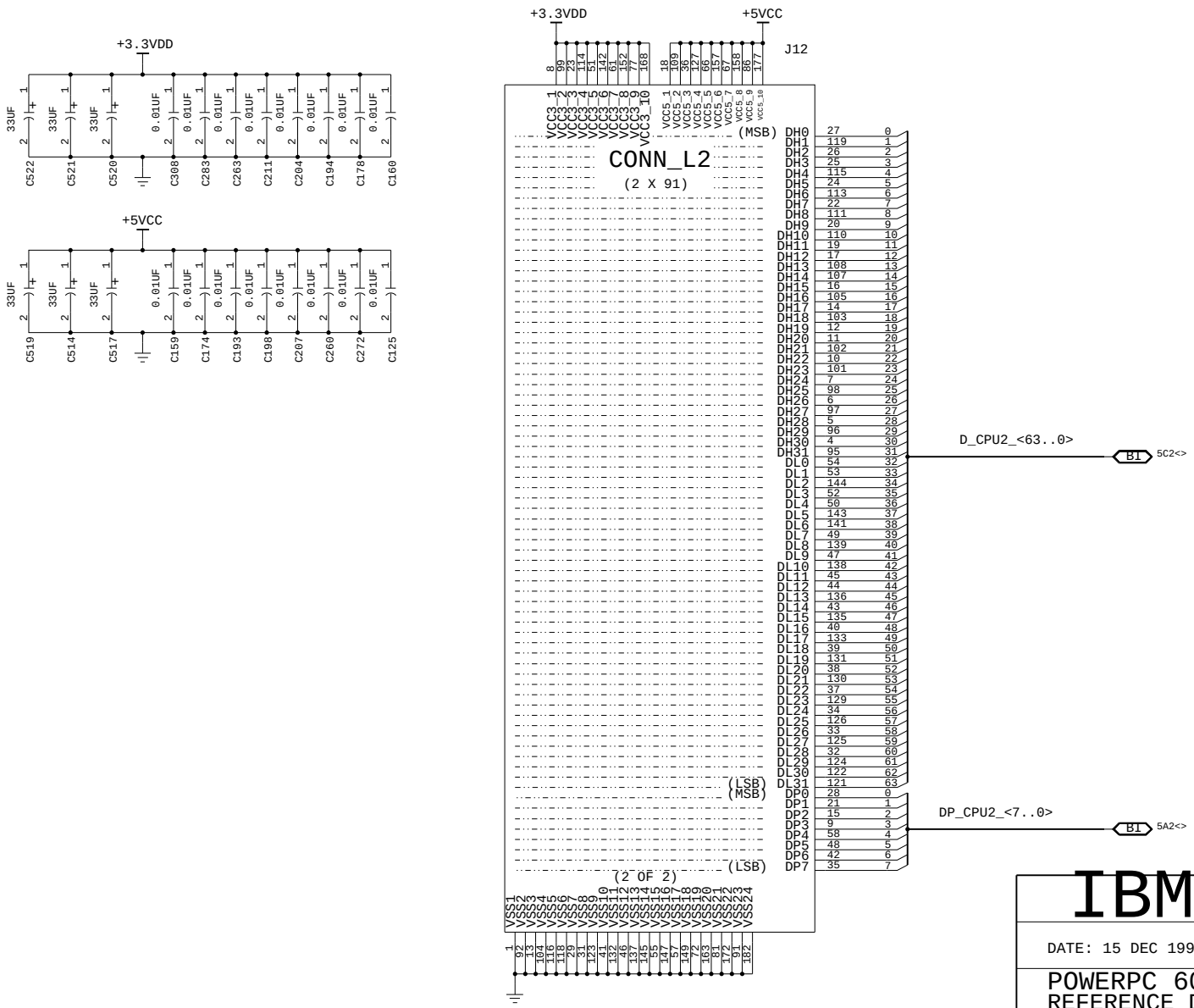
IBM	72 PIN DRAM DIMMS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 16 OF 64

MOTHERBOARD



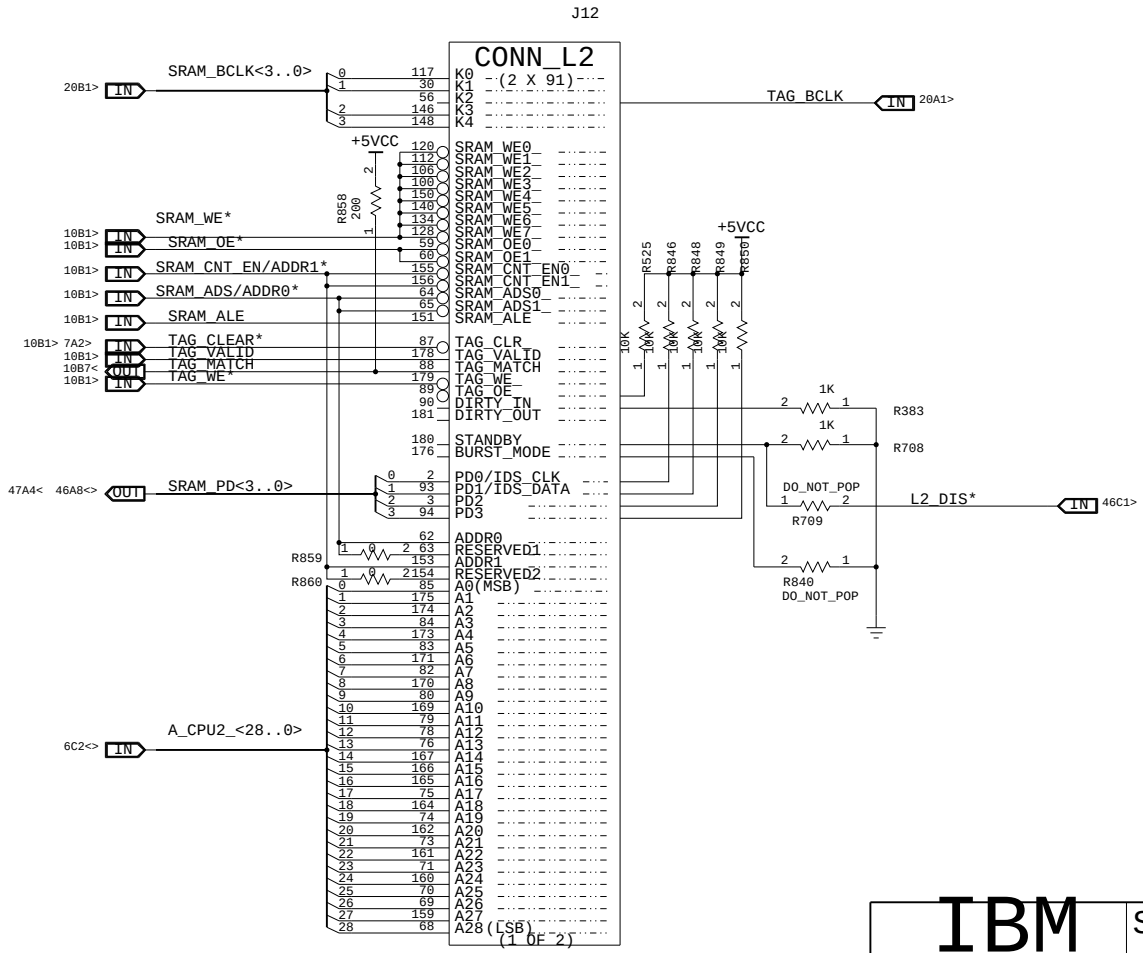
IBM	72 PIN DRAM DIMMS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 17 OF 64		

MOTHERBOARD



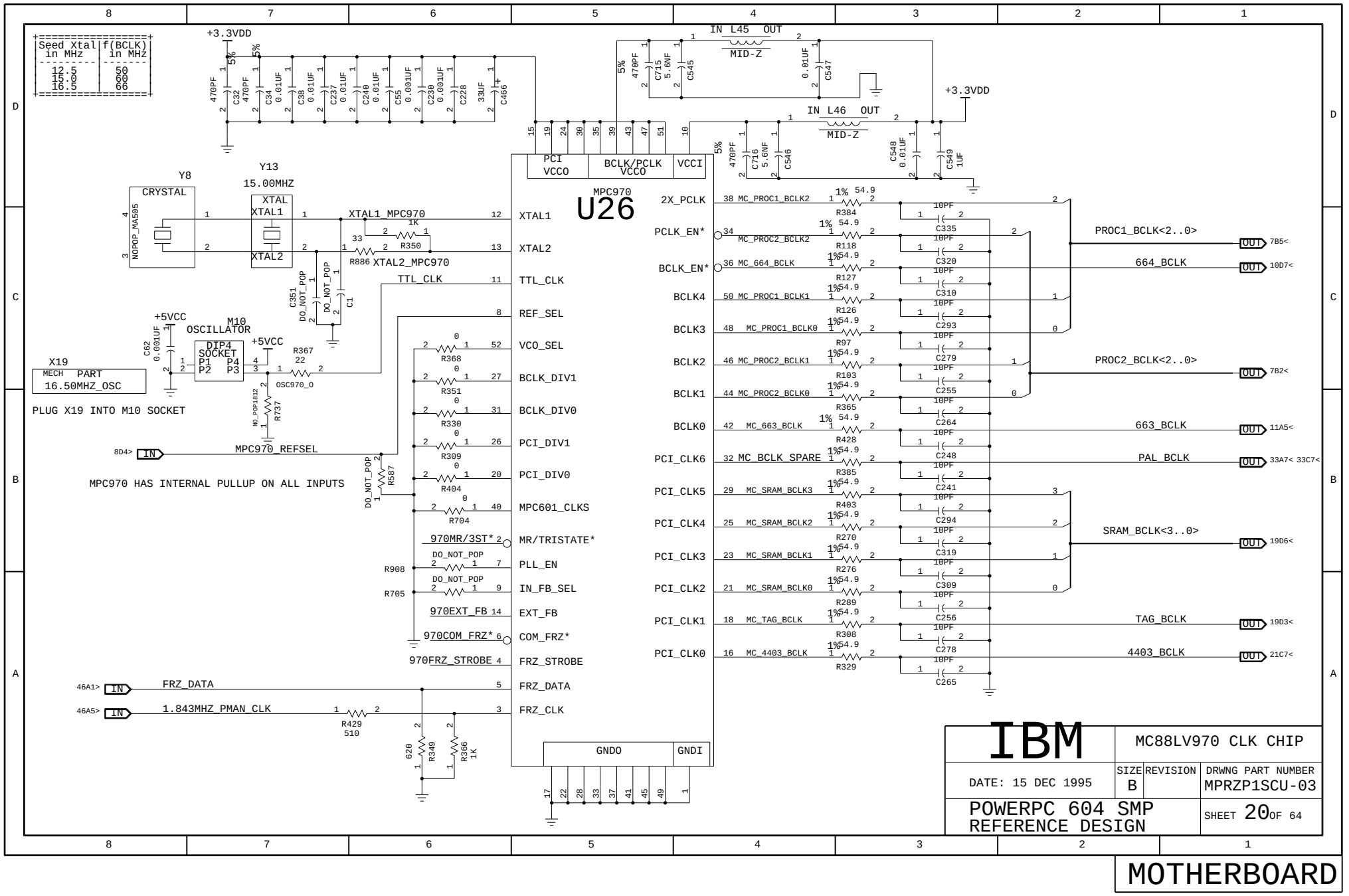
IBM	SRAM+TRAM CONN. (DATA)		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 18 OF 64		

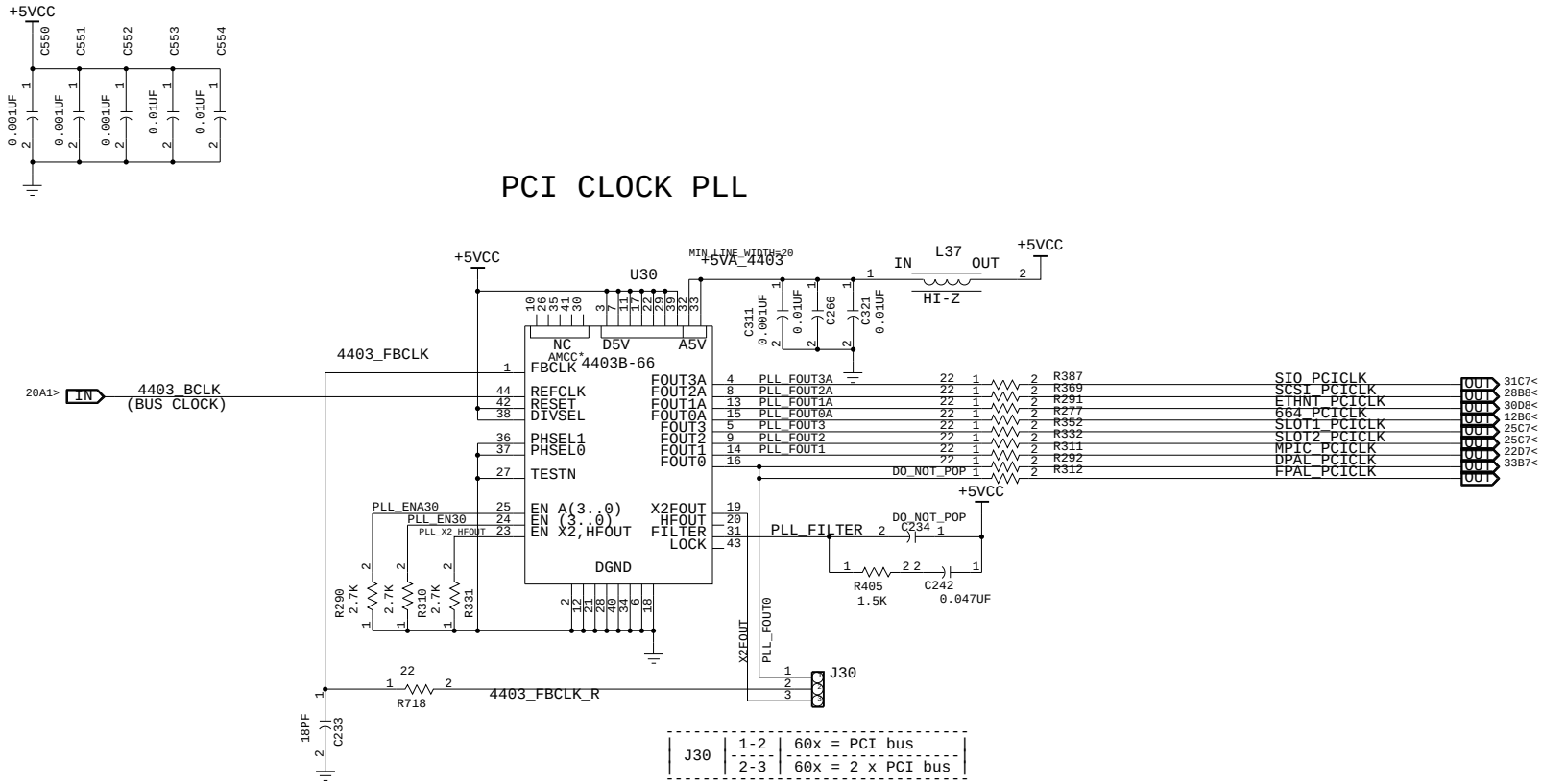
MOTHERBOARD



IBM	SRAM+TRAM CONN. (CONTROL)		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 19 OF 64		

MOTHERBOARD


Seed Xtal in MHz | f(BCLK) in MHz
12.5 | 50
15.0 | 60
16.5 | 66
+3.3VDD
IN L45 OUT
MID-Z
IN L46 OUT
MID-Z
+3.3VDD
PCI VCCO
BCLK/PCLK VCCO
VCCI
MPC970
U26
Y8
CRYSTAL
Y13
15.00MHZ
XTAL1_MPC970
XTAL2_MPC970
TTL_CLK
REF_SEL
VCO_SEL
BCLK_DIV1
BCLK_DIV0
PCI_DIV1
PCI_DIV0
MPC601_CLKS
970MR/3ST*
PLL_EN
IN_FB_SEL
970EXT_FB
EXT_FB
970COM_FRZ*
COM_FRZ*
970FRZ_STROBE
FRZ_STROBE
FRZ_DATA
FRZ_CLK
GNDO
GNDI
M10
OSCILLATOR
X19
MECH PART
16.50MHZ_OSC
PLUG X19 INTO M10 SOCKET
MPC970_REFSEL
MPC970 HAS INTERNAL PULLUP ON ALL INPUTS
FRZ_DATA
1.843MHZ_PMAN_CLK
2X_PCLK
PCLK_EN*
BCLK_EN*
BCLK4
BCLK3
BCLK2
BCLK1
BCLK0
PCI_CLK6
PCI_CLK5
PCI_CLK4
PCI_CLK3
PCI_CLK2
PCI_CLK1
PCI_CLK0
MC_PROC1_BCLK2
MC_PROC2_BCLK2
MC_664_BCLK
MC_PROC1_BCLK1
MC_PROC1_BCLK0
MC_PROC2_BCLK1
MC_PROC2_BCLK0
MC_663_BCLK
MC_BCLK_SPARE
MC_SRAM_BCLK3
MC_SRAM_BCLK2
MC_SRAM_BCLK1
MC_SRAM_BCLK0
MC_TAG_BCLK
MC_4403_BCLK
PROC1_BCLK<2..0>
PROC2_BCLK<2..0>
SRAM_BCLK<3..0>
664_BCLK
663_BCLK
PAL_BCLK
TAG_BCLK
4403_BCLK
IBM
MC88LV970 CLK CHIP
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN
SHEET 20 OF 64
MOTHERBOARD



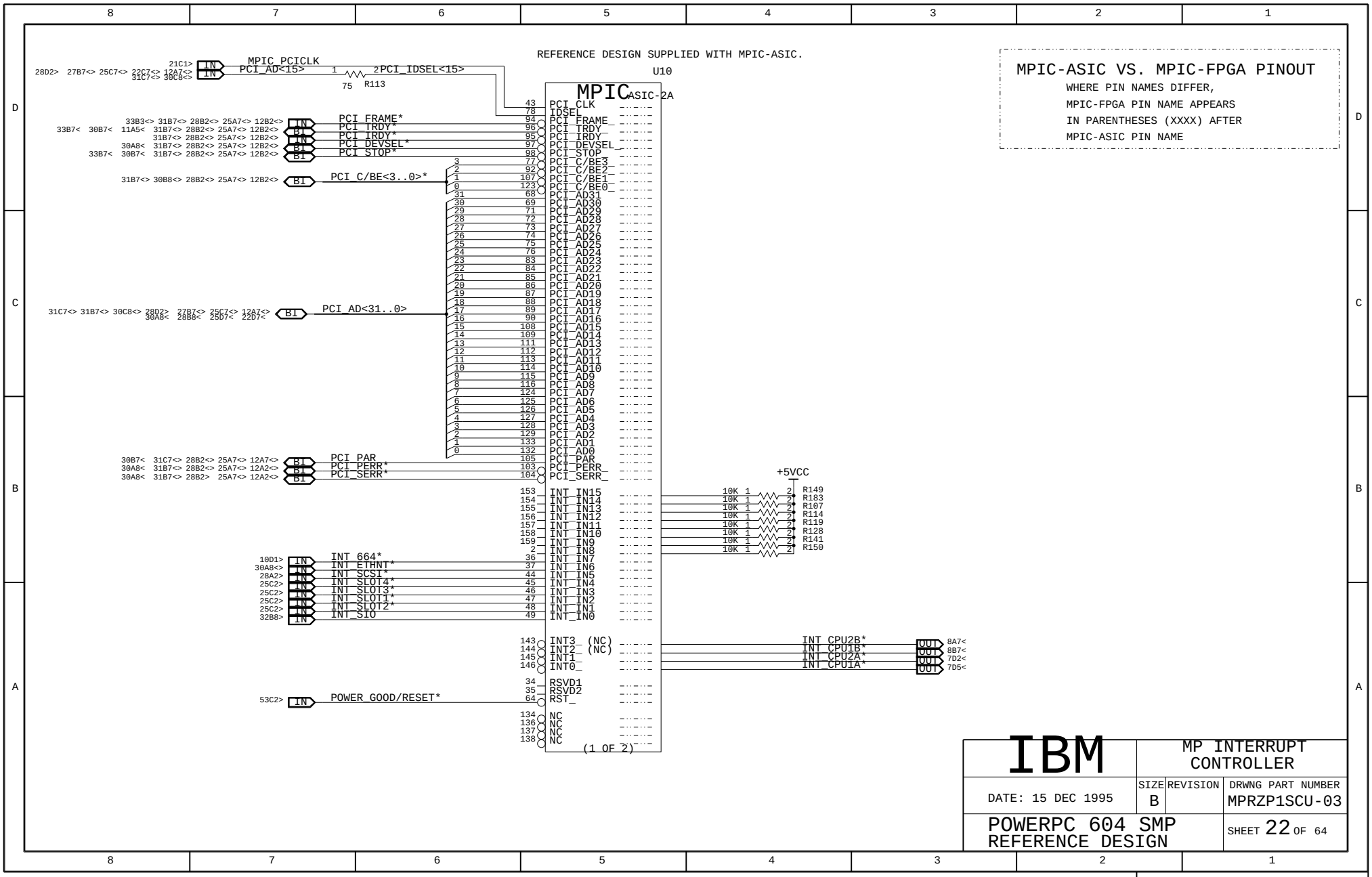
DIVSEL=0 --> VCO freq is divided by 4
DIVSEL=1 --> VCO freq is divided by 8

PHSEL (1:0)	Output fed to FBCLK	Output Phase Relationships		
		Fout(0-3)	HFout	X2Fout(/8)
00	Fout(0-3)	0	0	2(0)
00	X2Fout(/8)	0/2	0/4	0

0 implies the output is aligned with REFCLK
2() implies the output is at twice the freq of REFCLK

IBM	PCI CLOCKS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 21 OF 64		

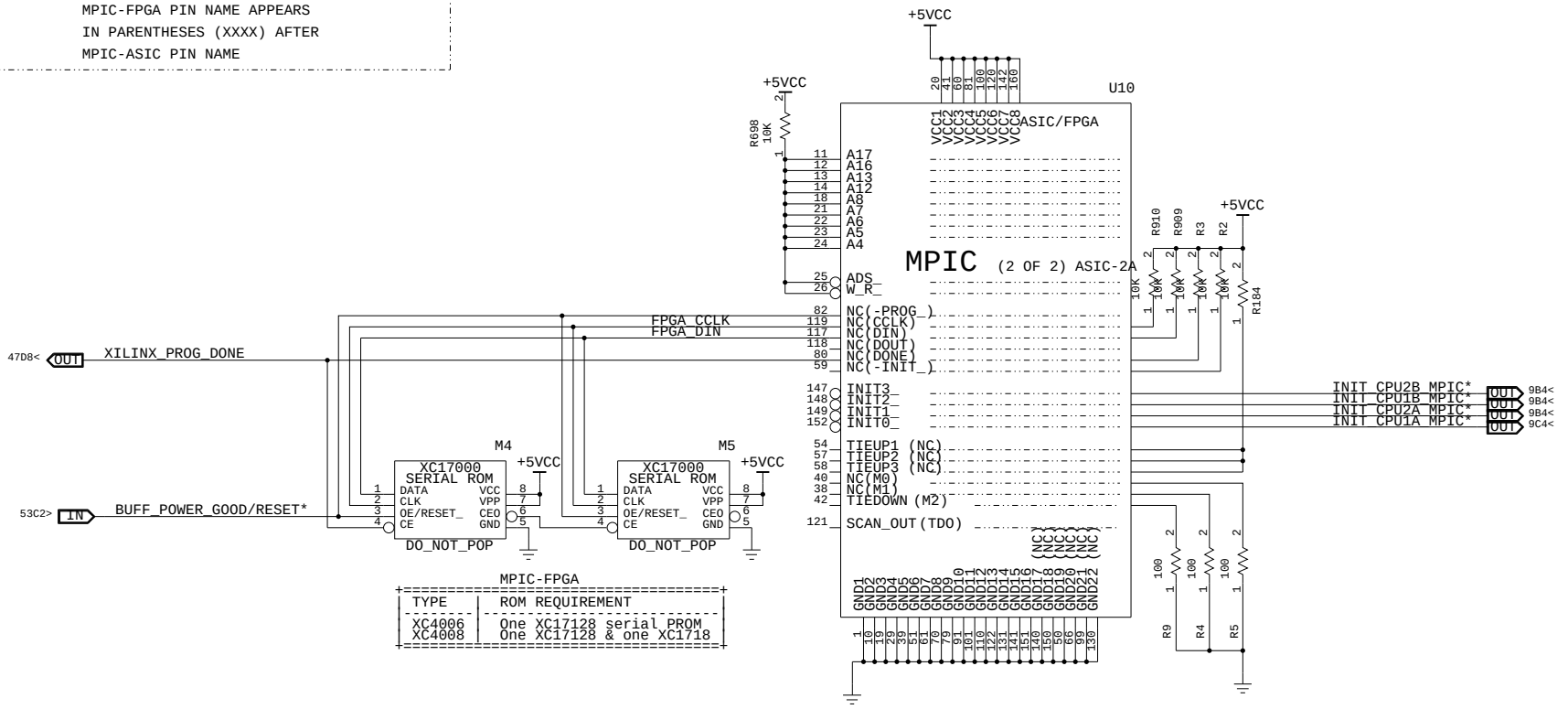
MOTHERBOARD


REFERENCE DESIGN SUPPLIED WITH MPIC-ASIC.
MPIC-ASIC VS. MPIC-FPGA PINOUT
WHERE PIN NAMES DIFFER,
MPIC-FPGA PIN NAME APPEARS
IN PARENTHESES (XXXX) AFTER
MPIC-ASIC PIN NAME
U10
MPIC ASIC-2A
MPIC_PCICLK
PCI_AD<15>
PCI_IDSEL<15>
R113
75
PCI_FRAME*
PCI_TRDY*
PCI_IRDY*
PCI_DEVSEL*
PCI_STOP*
PCI_C/BE<3..0>*
PCI_AD<31..0>
PCI_PAR
PCI_PERR*
PCI_SERR*
INT_664*
INT_ETHNT*
INT_SCSI*
INT_SLOT4*
INT_SLOT3*
INT_SLOT1*
INT_SLOT2*
INT_SIO
POWER_GOOD/RESET*
+5VCC
INT_CPU2B*
INT_CPU1B*
INT_CPU2A*
INT_CPU1A*
(1 OF 2)
IBM
MP INTERRUPT CONTROLLER
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN
SHEET 22 OF 64
MOTHERBOARD

MPCI-ASIC VS. MPIC-FPGA PINOUT

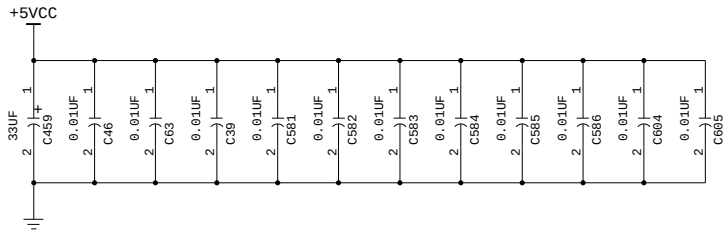
WHERE PIN NAMES DIFFER,
MPIC-FPGA PIN NAME APPEARS
IN PARENTHESES (XXXX) AFTER
MPIC-ASIC PIN NAME

REFERENCE DESIGN SUPPLIED WITH MPIC-ASIC.



MPIC-FPGA

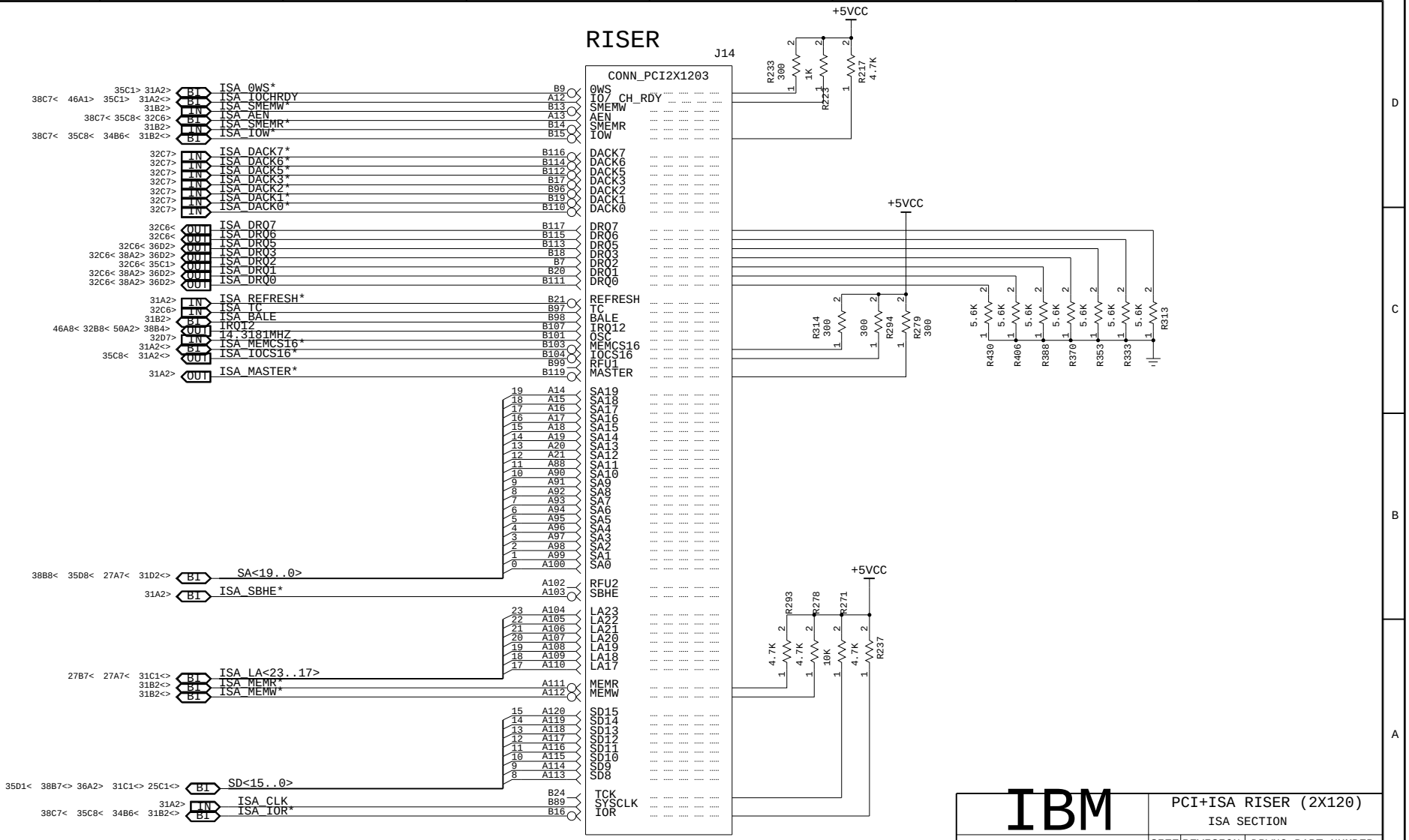
TYPE	ROM REQUIREMENT
XC4006	One XC17128 serial PROM
XC4008	One XC17128 & one XC1718



IBM	MP INTERRUPT CONTROLLER		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 23 OF 64		

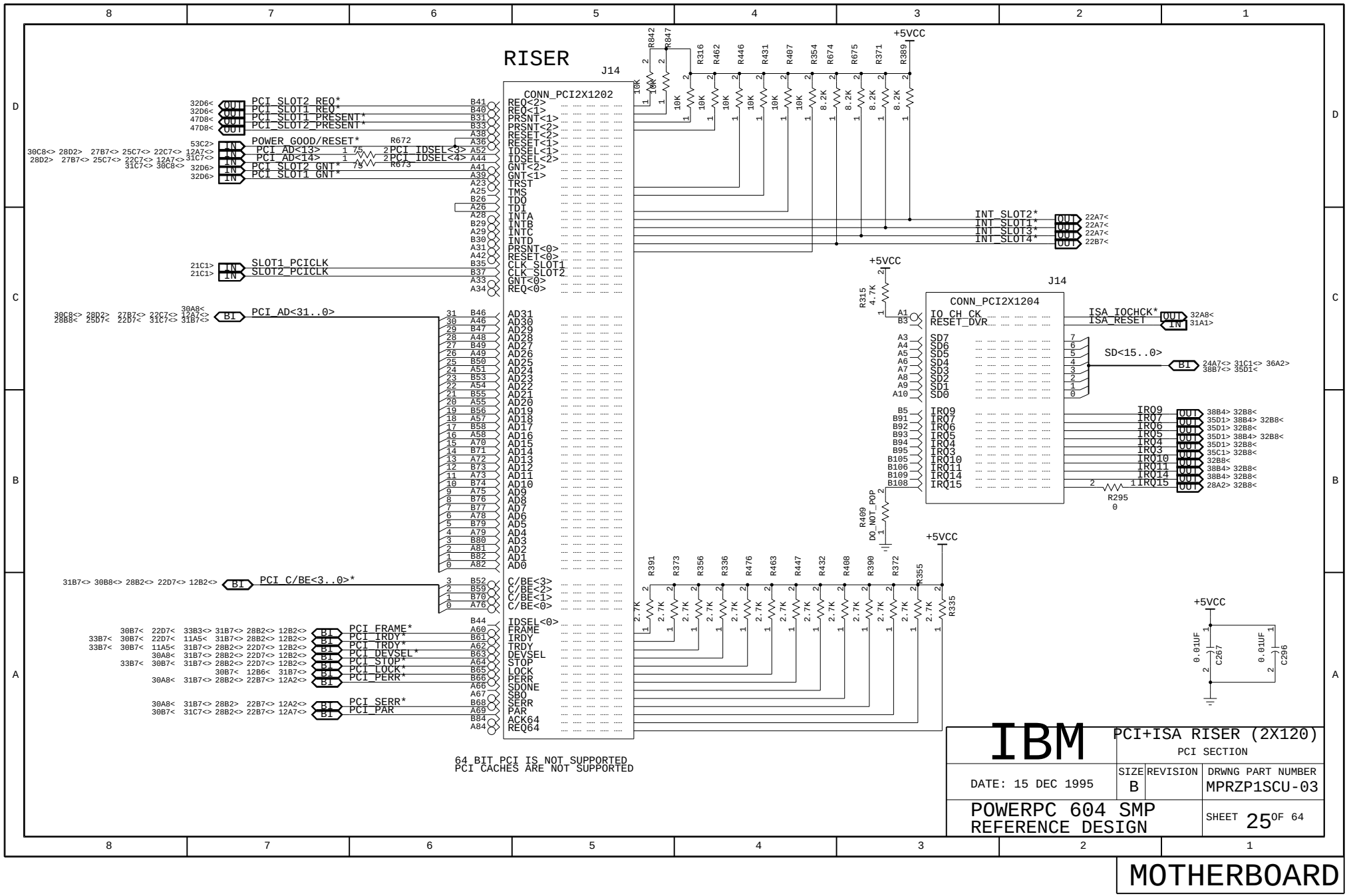
MOTHERBOARD

RISER

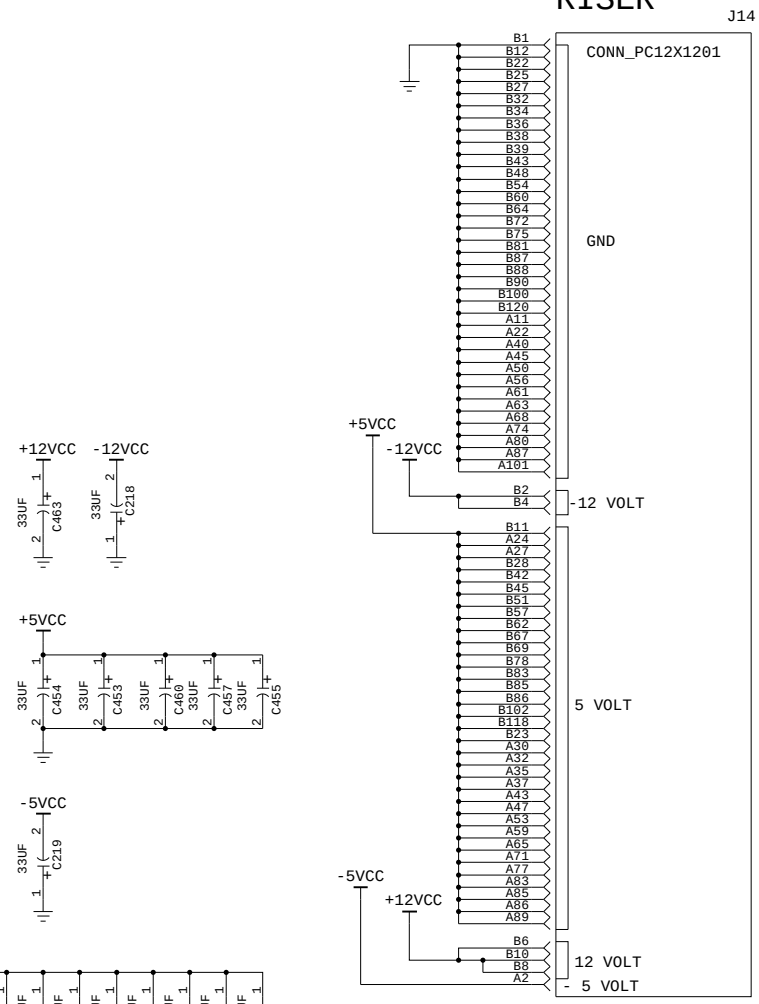


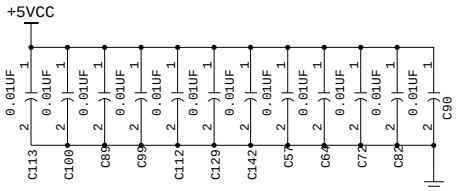
IBM	PCI+ISA RISER (2X120) ISA SECTION		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 24 OF 64		

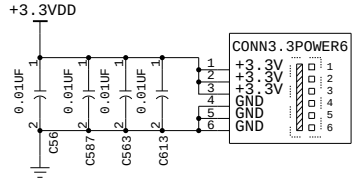
MOTHERBOARD


RISER
J14
CONN_PCI2X1202
PCI SLOT2 REQ*
PCI SLOT1 REQ*
PCI SLOT1 PRESENT*
PCI SLOT2 PRESENT*
POWER GOOD/RESET*
PCI AD<13>
PCI AD<14>
PCI SLOT2 GNT*
PCI SLOT1 GNT*
SLOT1 PCICLK
SLOT2 PCICLK
PCI AD<31..0>
PCI C/BE<3..0>*
PCI FRAME*
PCI IRDY*
PCI TRDY*
PCI DEVSEL*
PCI STOP*
PCI LOCK*
PCI PERR*
PCI SERR*
PCI PAR
+5VCC
INT_SLOT2*
INT_SLOT1*
INT_SLOT3*
INT_SLOT4*
J14
CONN_PCI2X1204
ISA_IOCHCK*
ISA_RESET
SD<15..0>
DO_NOT_POP
64 BIT PCI IS NOT SUPPORTED
PCI CACHES ARE NOT SUPPORTED
IBM
PCI+ISA RISER (2X120)
PCI SECTION
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 25 OF 64
MOTHERBOARD

RISER



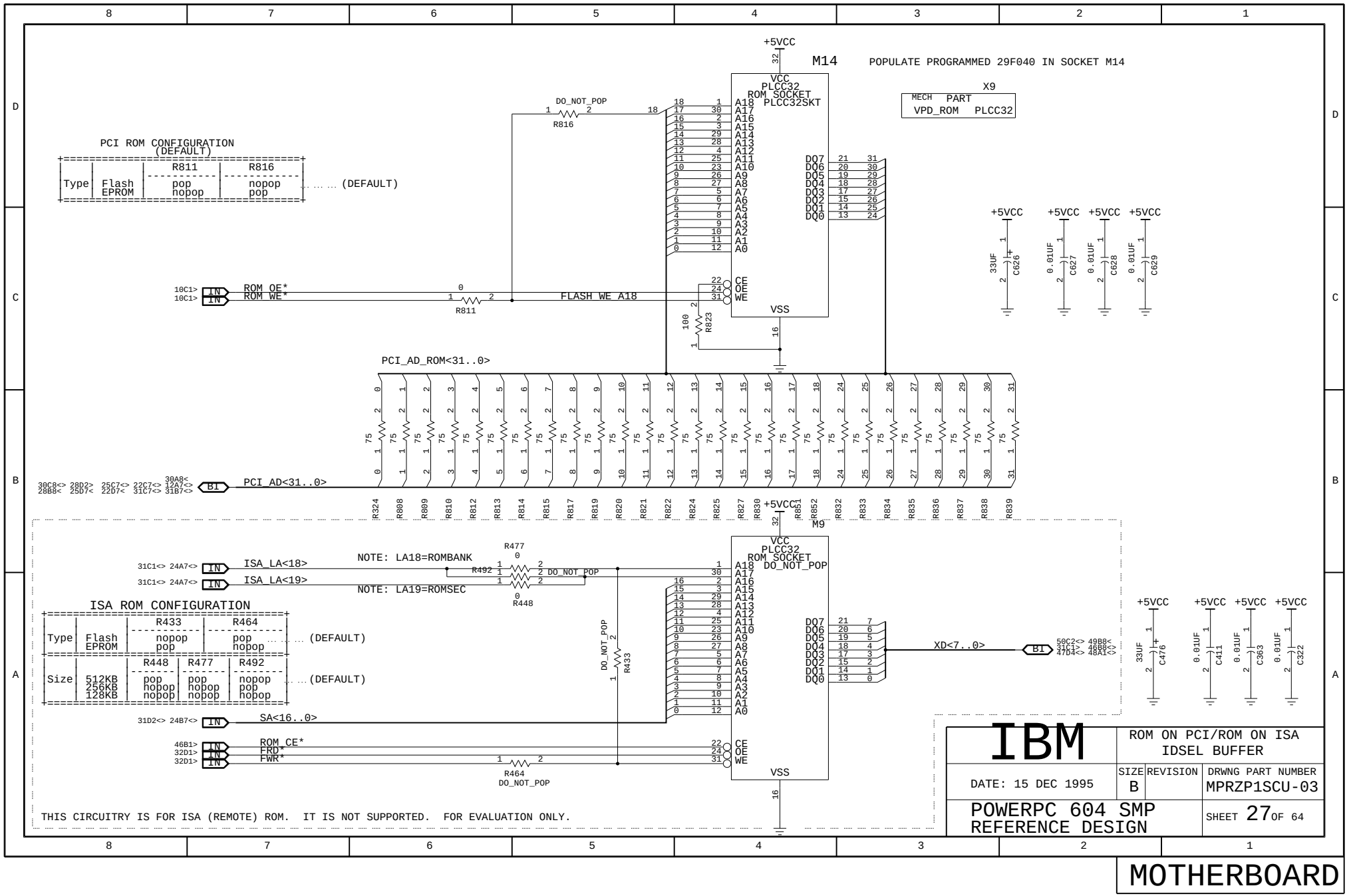




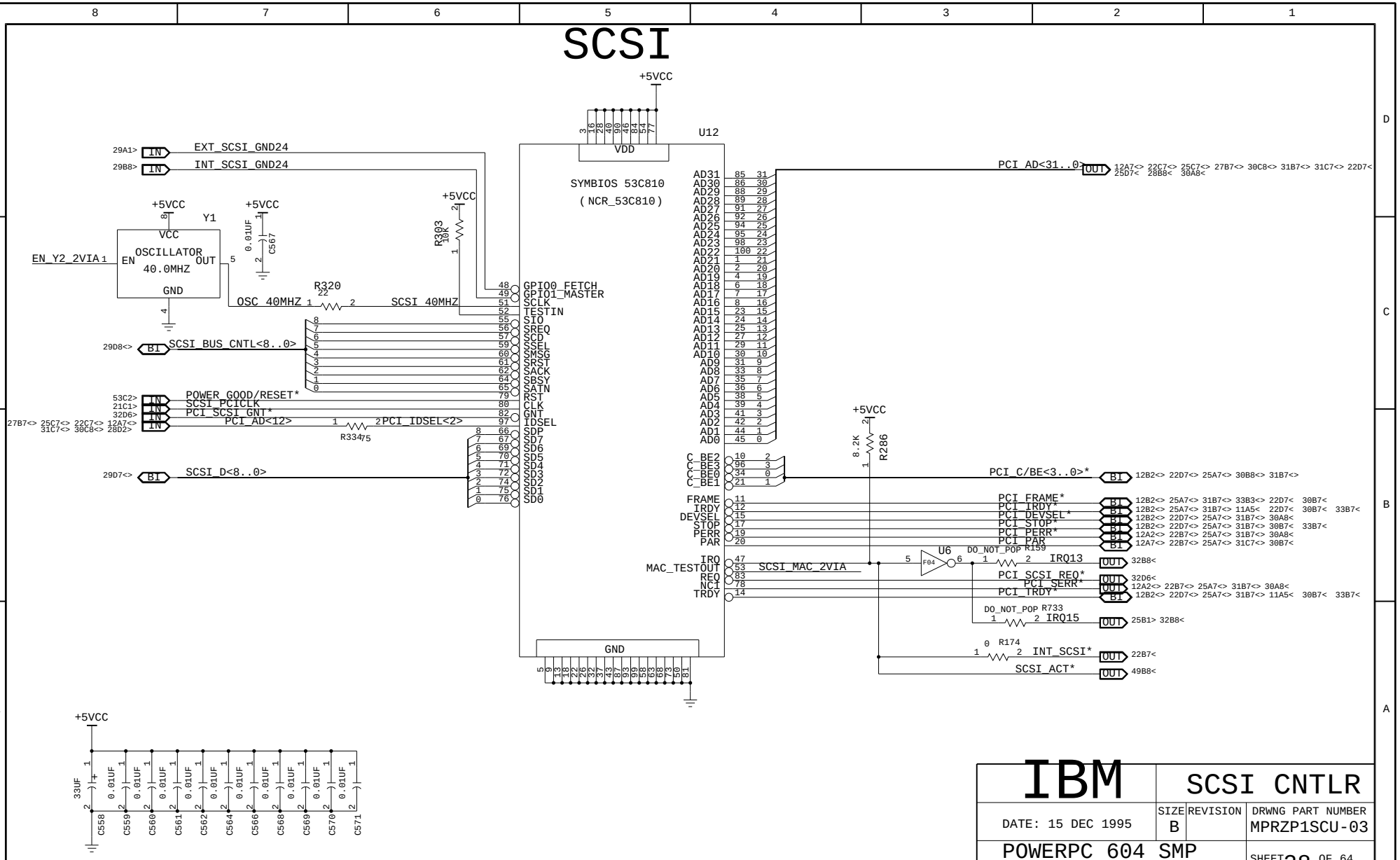
J50 PROVIDES +3.3V (FROM PLANAR POWER SUPPLY)
FOR RISER CARDS WHICH NEED +3.3VOLTS

IBM	PCI+ISA RISER (2X120) POWER PINS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 26 OF 64		

MOTHERBOARD


M14
POPULATE PROGRAMMED 29F040 IN SOCKET M14
+5VCC
VCC
PLCC32
ROM SOCKET
PLCC32SKT
X9
MECH PART
VPD_ROM PLCC32
DO_NOT_POP
R816
PCI ROM CONFIGURATION
(DEFAULT)
Type Flash EPROM
R811 pop nopop
R816 nopop pop
(DEFAULT)
ROM_OE*
ROM_WE*
R811
FLASH_WE_A18
R823
VSS
PCI_AD_ROM<31..0>
PCI_AD<31..0>
M9
NOTE: LA18=ROMBANK
NOTE: LA19=ROMSEC
ISA_LA<18>
ISA_LA<19>
R477
R492
R448
DO_NOT_POP
ISA ROM CONFIGURATION
Type Flash EPROM
R433 nopop pop
R464 pop nopop
(DEFAULT)
Size 512KB 256KB 128KB
R448 pop nopop nopop
R477 pop nopop nopop
R492 nopop pop nopop
(DEFAULT)
R433
SA<16..0>
ROM_CE*
FRD*
FWR*
R464
DO_NOT_POP
XD<7..0>
THIS CIRCUITRY IS FOR ISA (REMOTE) ROM. IT IS NOT SUPPORTED. FOR EVALUATION ONLY.
IBM
ROM ON PCI/ROM ON ISA
IDSEL BUFFER
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 27 OF 64
MOTHERBOARD

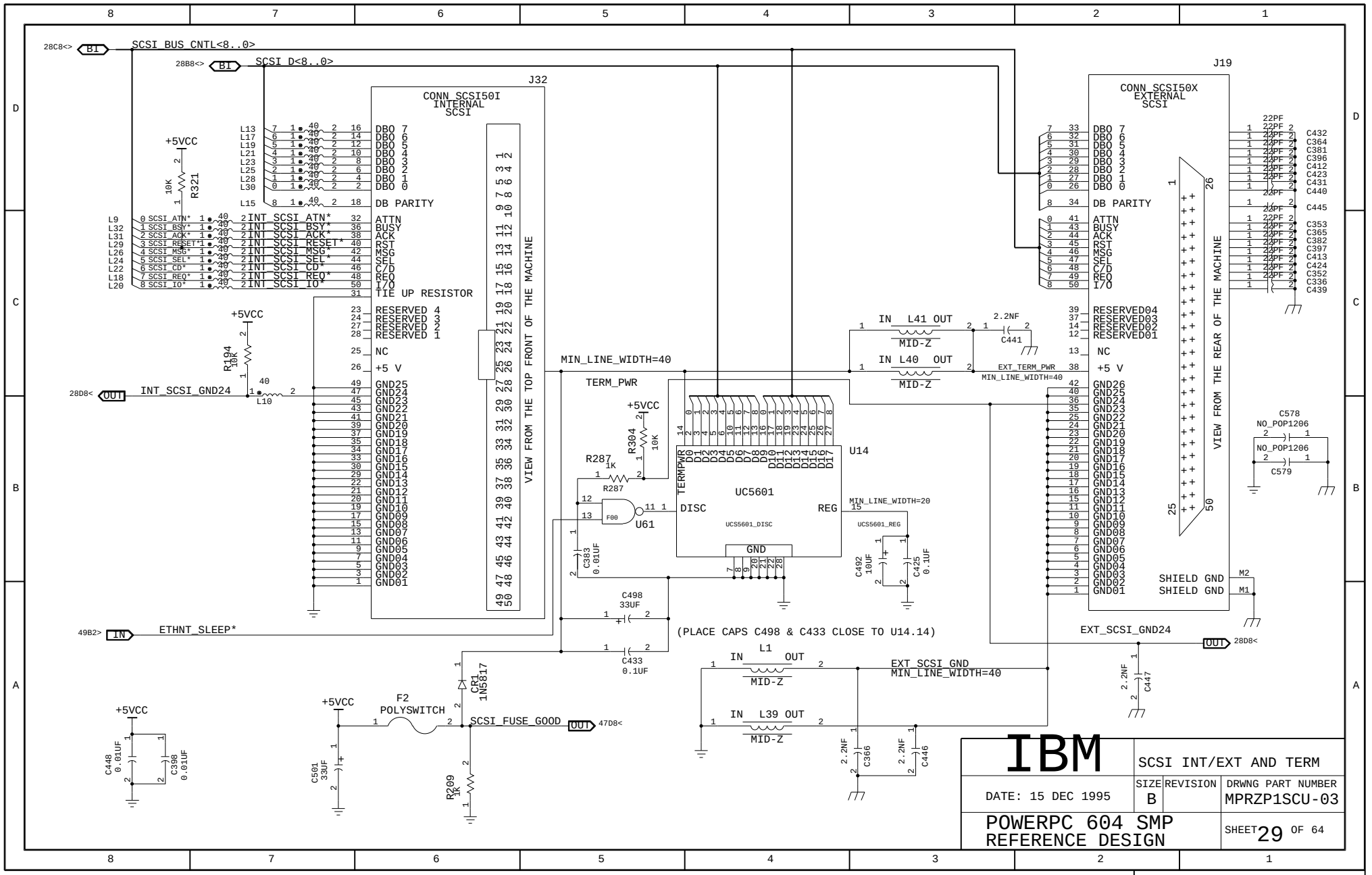
SCSI

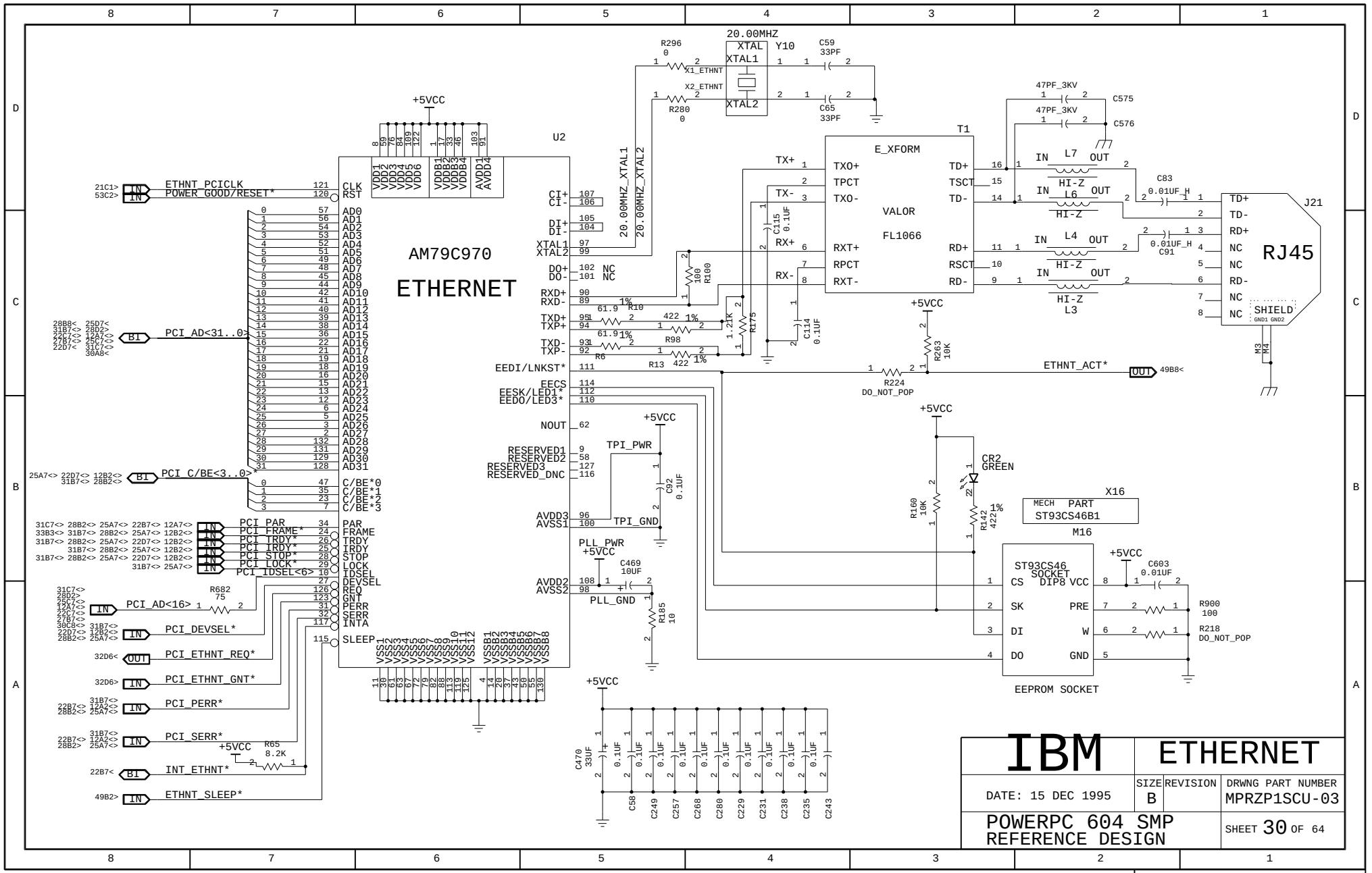


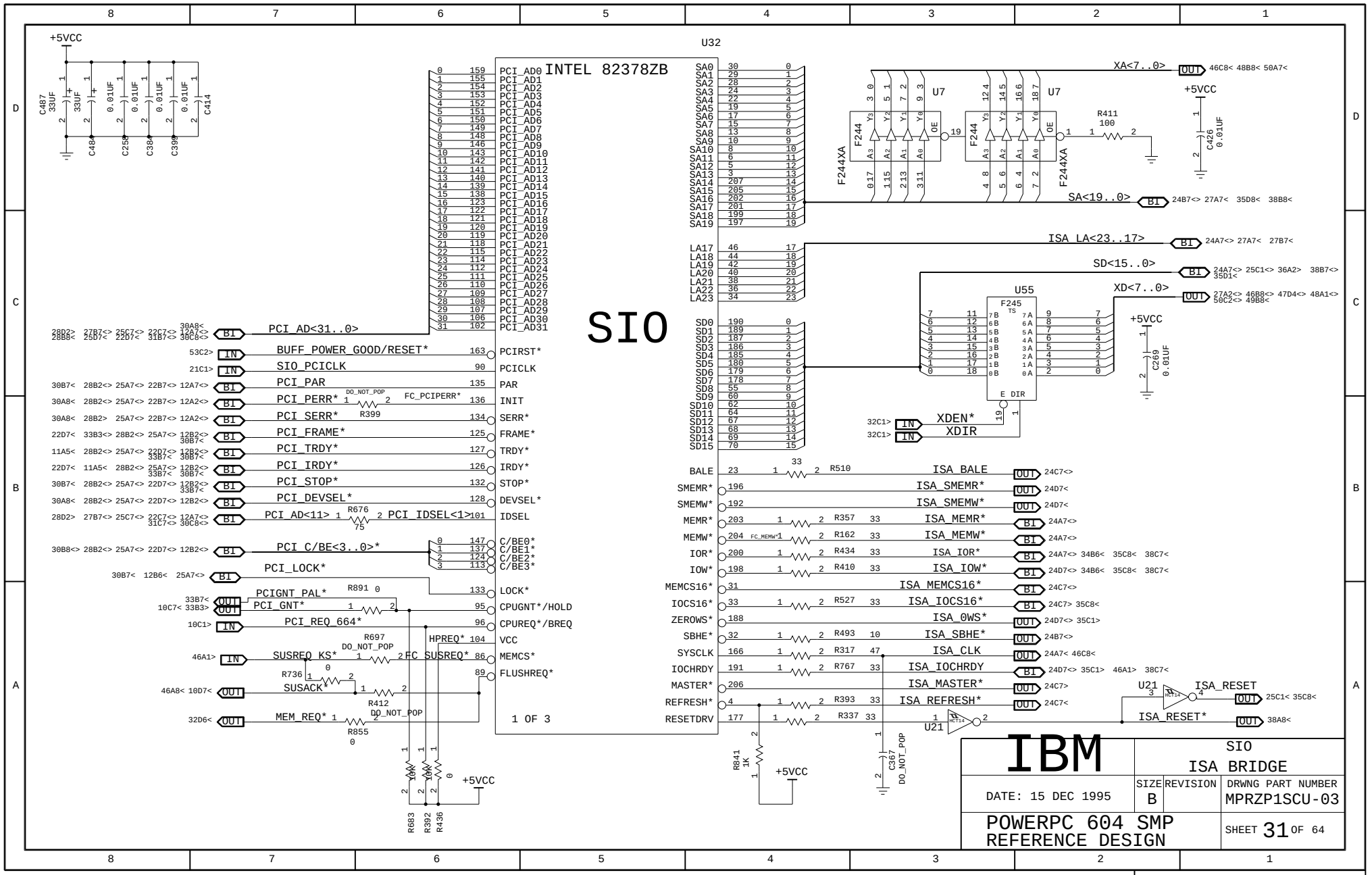
* TRADEMARK OF NATIONAL CASH REGISTER CORP.

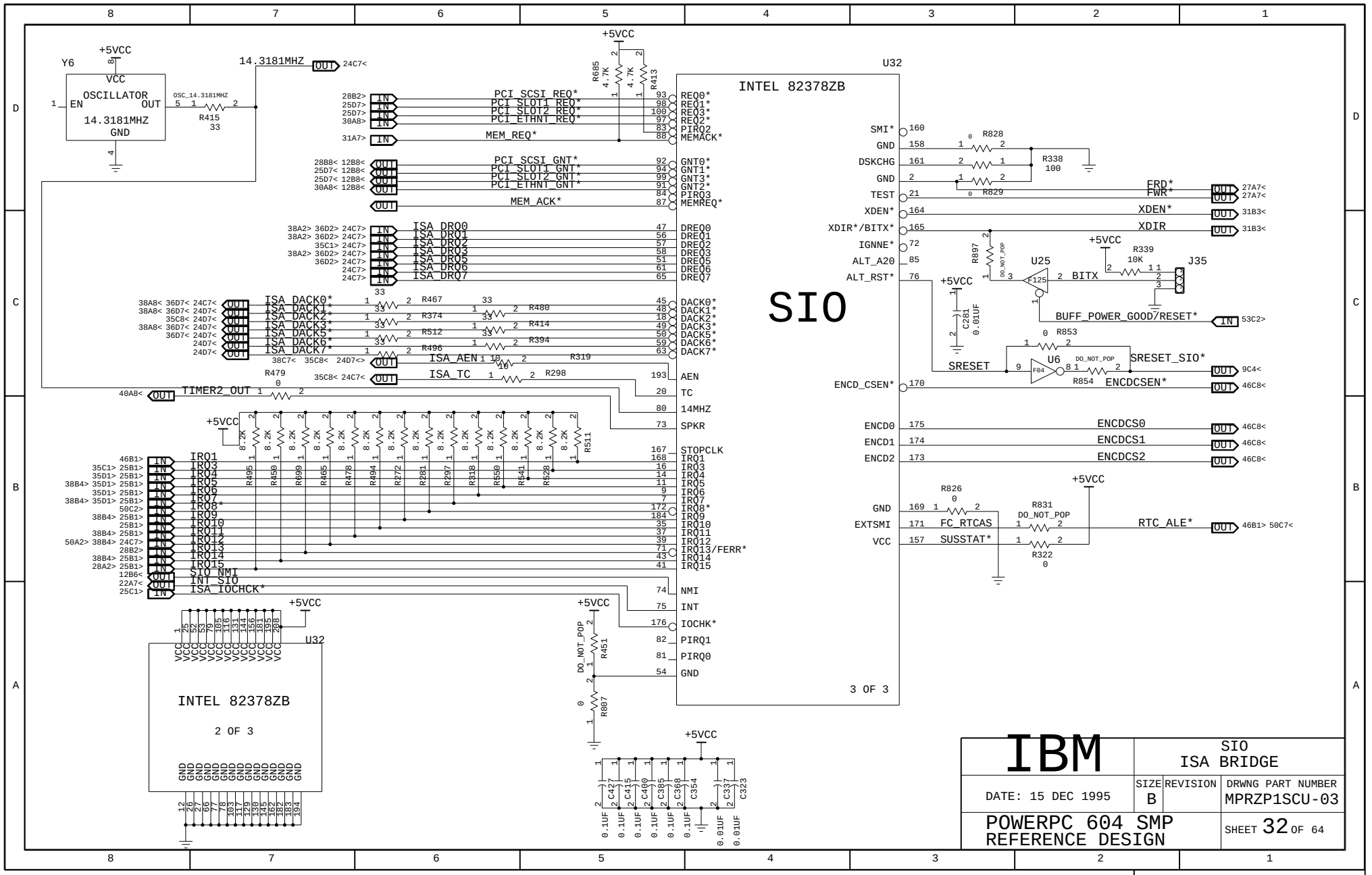
IBM	SCSI CNTLR		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 28 OF 64

MOTHERBOARD

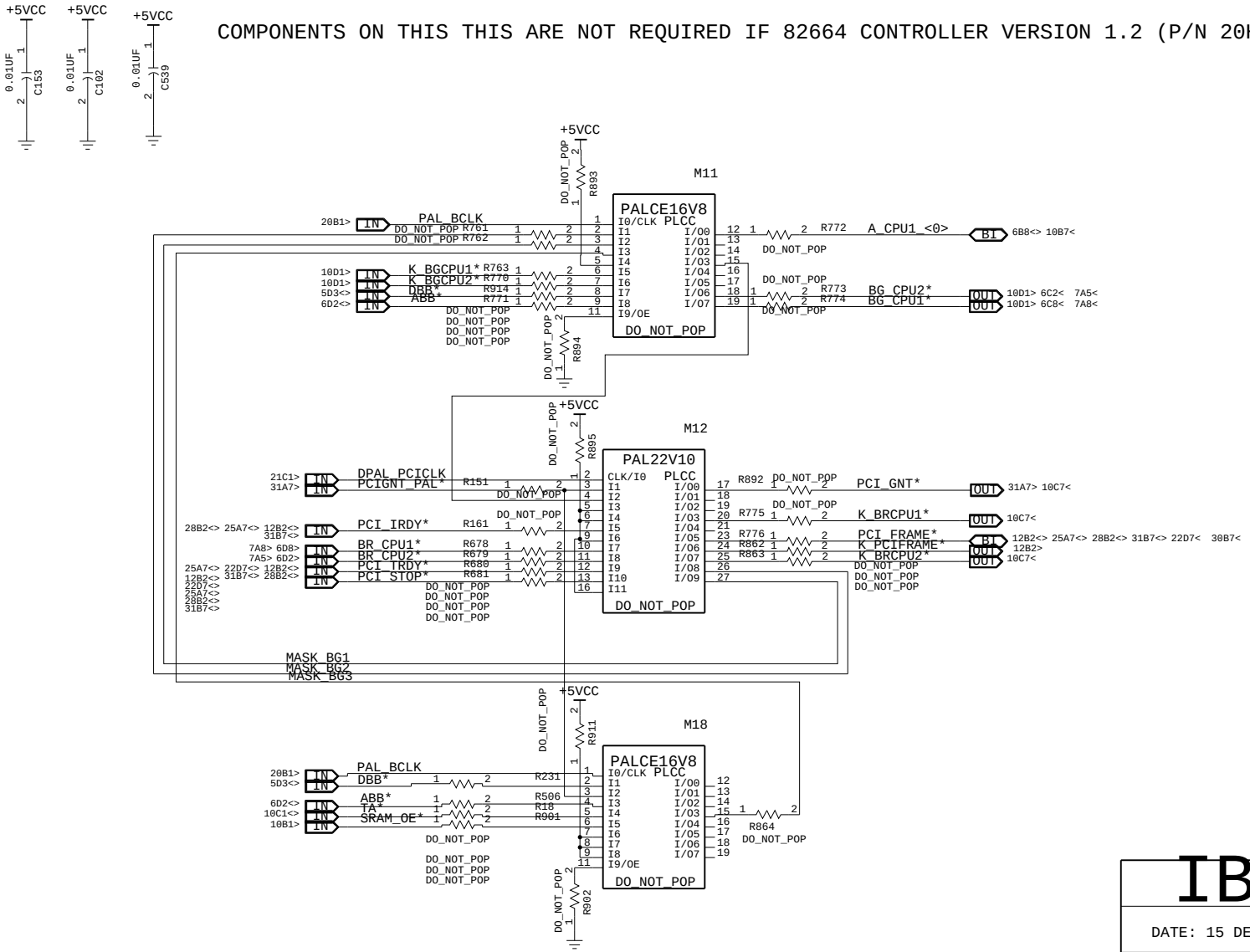

SCSI BUS CNTL<8..0>
SCSI D<8..0>
J32
CONN SCSI50I
INTERNAL
SCSI
VIEW FROM THE TOP FRONT OF THE MACHINE
J19
CONN SCSI50X
EXTERNAL
SCSI
VIEW FROM THE REAR OF THE MACHINE
DB PARITY
ATTN
BUSY
ACK
RST
MSG
SEL
C/D
REQ
I/O
TIE UP RESISTOR
RESERVED 4
RESERVED 3
RESERVED 2
RESERVED 1
NC
+5 V
INT_SCSI_GND24
MIN_LINE_WIDTH=40
TERM_PWR
EXT_TERM_PWR
U14
UC5601
DISC
REG
U61
F00
GND
ETHNT_SLEEP*
(PLACE CAPS C498 & C433 CLOSE TO U14.14)
EXT_SCSI_GND24
EXT_SCSI_GND
SCSI_FUSE_GOOD
F2
POLYSWITCH
CR1
1N5817
SHIELD GND
MID-Z
IBM
SCSI INT/EXT AND TERM
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 29 OF 64
MOTHERBOARD


AM79C970
ETHERNET
U2
20.00MHZ
XTAL Y10
XTAL1
XTAL2
20.00MHZ_XTAL1
20.00MHZ_XTAL2
T1
E_XFORM
VALOR
FL1066
TX+
TX-
RX+
RX-
TXO+
TPCT
TXO-
RXT+
RPCT
RXT-
TD+
TSCT
TD-
RD+
RSCT
RD-
RJ45
J21
SHIELD
ETHNT_PCICLK
POWER_GOOD/RESET*
PCI_AD<31..0>
PCI C/BE<3..0>
PCI_PAR
PCI_FRAME*
PCI_TRDY*
PCI_IRDY*
PCI_STOP*
PCI_LOCK*
PCI_IDSEL<6>
PCI_AD<16>
PCI_DEVSEL*
PCI_ETHNT_REQ*
PCI_ETHNT_GNT*
PCI_PERR*
PCI_SERR*
INT_ETHNT*
ETHNT_SLEEP*
ETHNT_ACT*
EEDI/LNKST*
EECS
EESK/LED1*
EEDO/LED3*
NOUT
TPI_PWR
TPI_GND
PLL_PWR
PLL_GND
ST93CS46
SOCKET
DIP8
EEPROM SOCKET
ST93CS46B1
M16
X16
CR2
GREEN
+5VCC
IBM
ETHERNET
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 30 OF 64
MOTHERBOARD


SIO
INTEL 82378ZB
U32
1 OF 3
PCI_AD<31..0>
BUFF_POWER_GOOD/RESET*
SIO_PCICLK
PCI_PAR
PCI_PERR*
PCI_SERR*
PCI_FRAME*
PCI_TRDY*
PCI_IRDY*
PCI_STOP*
PCI_DEVSEL*
PCI_AD<11>
PCI_IDSEL<1>
PCI C/BE<3..0>*
PCI_LOCK*
PCIGNT_PAL*
PCI_GNT*
PCI_REQ_664*
SUSREQ_KS*
FC_SUSREQ*
SUSACK*
MEM_REQ*
HPREQ*
FC_PCIPERR*
PCIRST*
PCICLK
PAR
INIT
SERR*
FRAME*
TRDY*
IRDY*
STOP*
DEVSEL*
IDSEL
C/BE0*
C/BE1*
C/BE2*
C/BE3*
LOCK*
CPUGNT*/HOLD
CPUREQ*/BREQ
VCC
MEMCS*
FLUSHREQ*
SA<19..0>
ISA LA<23..17>
SD<15..0>
XA<7..0>
XD<7..0>
XDEN*
XDIR
ISA_BALE
ISA_SMEMR*
ISA_SMEMW*
ISA_MEMR*
ISA_MEMW*
ISA_IOR*
ISA_IOW*
ISA_MEMCS16*
ISA_IOCS16*
ISA_0WS*
ISA_SBHE*
ISA_CLK
ISA_IOCHRDY
ISA_MASTER*
ISA_REFRESH*
ISA_RESET
ISA_RESET*
U7
U55
U21
F244
F245
F244XA
+5VCC
IBM
SIO
ISA BRIDGE
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 31 OF 64
MOTHERBOARD

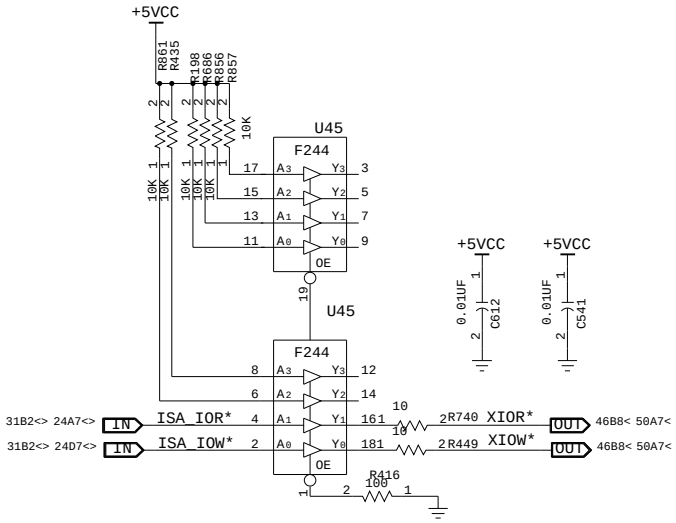

SIO
INTEL 82378ZB
U32
3 OF 3
INTEL 82378ZB
2 OF 3
U32
Y6
OSCILLATOR
14.3181MHZ
GND
VCC
EN
OUT
R415
33
PCI_SCSI_REQ*
PCI_SLOT1_REQ*
PCI_SLOT2_REQ*
PCI_ETHNT_REQ*
MEM_REQ*
PCI_SCSI_GNT*
PCI_SLOT1_GNT*
PCI_SLOT2_GNT*
PCI_ETHNT_GNT*
MEM_ACK*
ISA_DRQ0
ISA_DRQ1
ISA_DRQ2
ISA_DRQ3
ISA_DRQ5
ISA_DRQ6
ISA_DRQ7
ISA_DACK0*
ISA_DACK1*
ISA_DACK2*
ISA_DACK3*
ISA_DACK5*
ISA_DACK6*
ISA_DACK7*
ISA_AEN
ISA_TC
TIMER2_OUT
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8*
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13
IRQ14
IRQ15
SIO_NMI
INT_SIO
ISA_IOCHCK*
REQ0*
REQ1*
REQ3*
REQ2*
PIRQ2
MEMACK*
GNT0*
GNT1*
GNT3*
GNT2*
PIRQ3
MEMREQ*
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
DACK0*
DACK1*
DACK2*
DACK3*
DACK5*
DACK6*
DACK7*
AEN
TC
14MHZ
SPKR
STOPCLK
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8*
IRQ9
IRQ10
IRQ11
IRQ12
IRQ13/FERR*
IRQ14
IRQ15
NMI
INT
IOCHK*
PIRQ1
PIRQ0
GND
SMI*
GND
DSKCHG
GND
TEST
XDEN*
XDIR*/BITX*
IGNNE*
ALT_A20
ALT_RST*
ENCD_CSEN*
ENCD0
ENCD1
ENCD2
GND
EXTSMI
VCC
FRD*
FWR*
XDEN*
XDIR
BITX
BUFF_POWER_GOOD/RESET*
SRESET
SRESET_SIO*
ENCDCSEN*
ENCDCS0
ENCDCS1
ENCDCS2
FC_RTCAS
SUSSTAT*
RTC_ALE*
+5VCC
R338
100
R339
10K
J35
U25
U6
C281
0.01UF
R828
R829
R853
R854
R826
R831
R322
R451
R807
R685
4.7K
R413
4.7K
R511
8.2K
R467
R480
R374
R414
R512
R394
R496
R319
R298
R479
R495
R450
R699
R465
R478
R494
R272
R281
R297
R318
R530
R541
R528
C427
C415
C400
C385
C368
C354
C337
C323
0.1UF
0.01UF
DO_NOT_POP
IBM
SIO
ISA BRIDGE
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 32 OF 64
MOTHERBOARD

COMPONENTS ON THIS THIS ARE NOT REQUIRED IF 82664 CONTROLLER VERSION 1.2 (P/N 20H2842) OR LATER IS USED



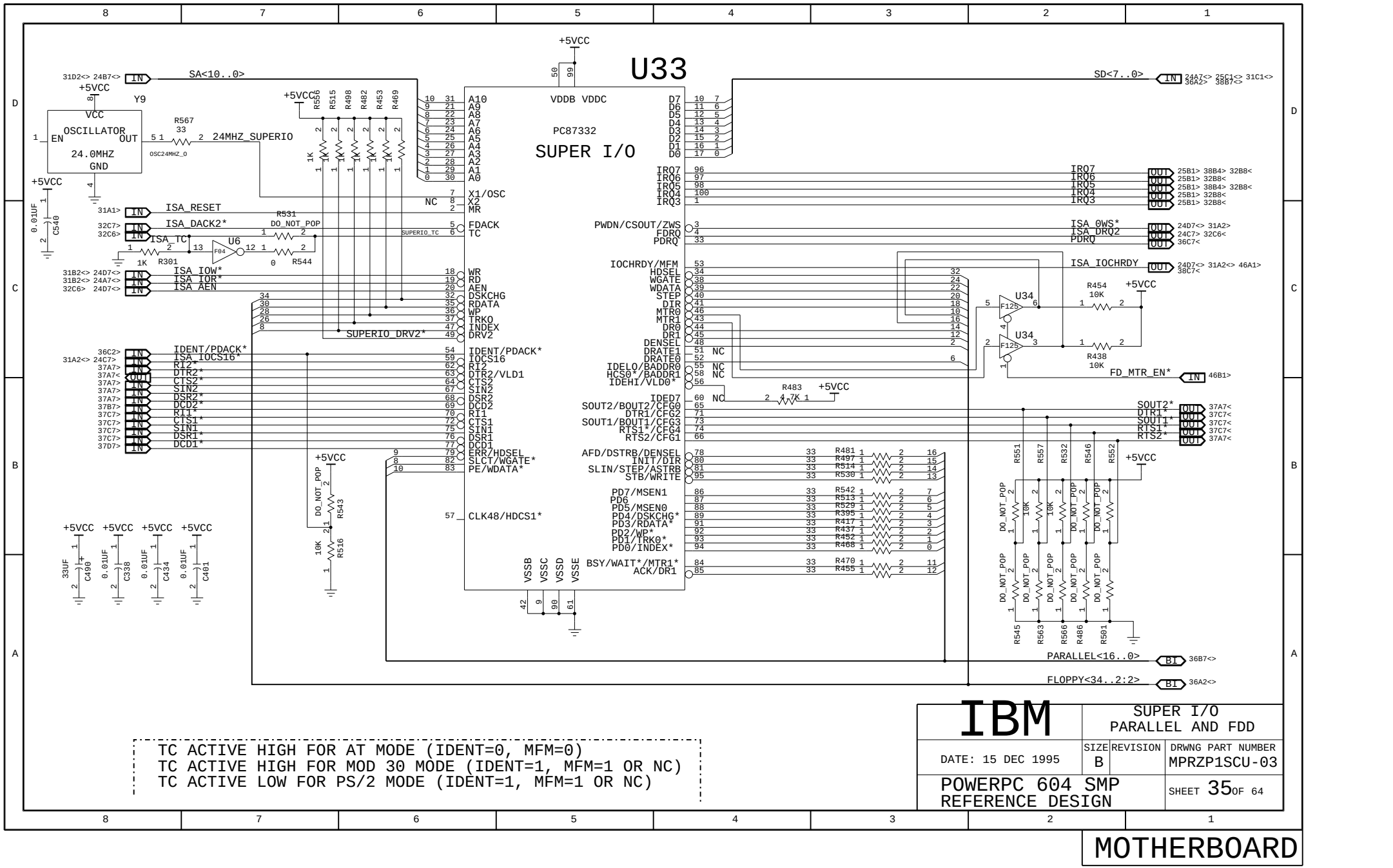
IBM			SPARE PALS
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 33 OF 64

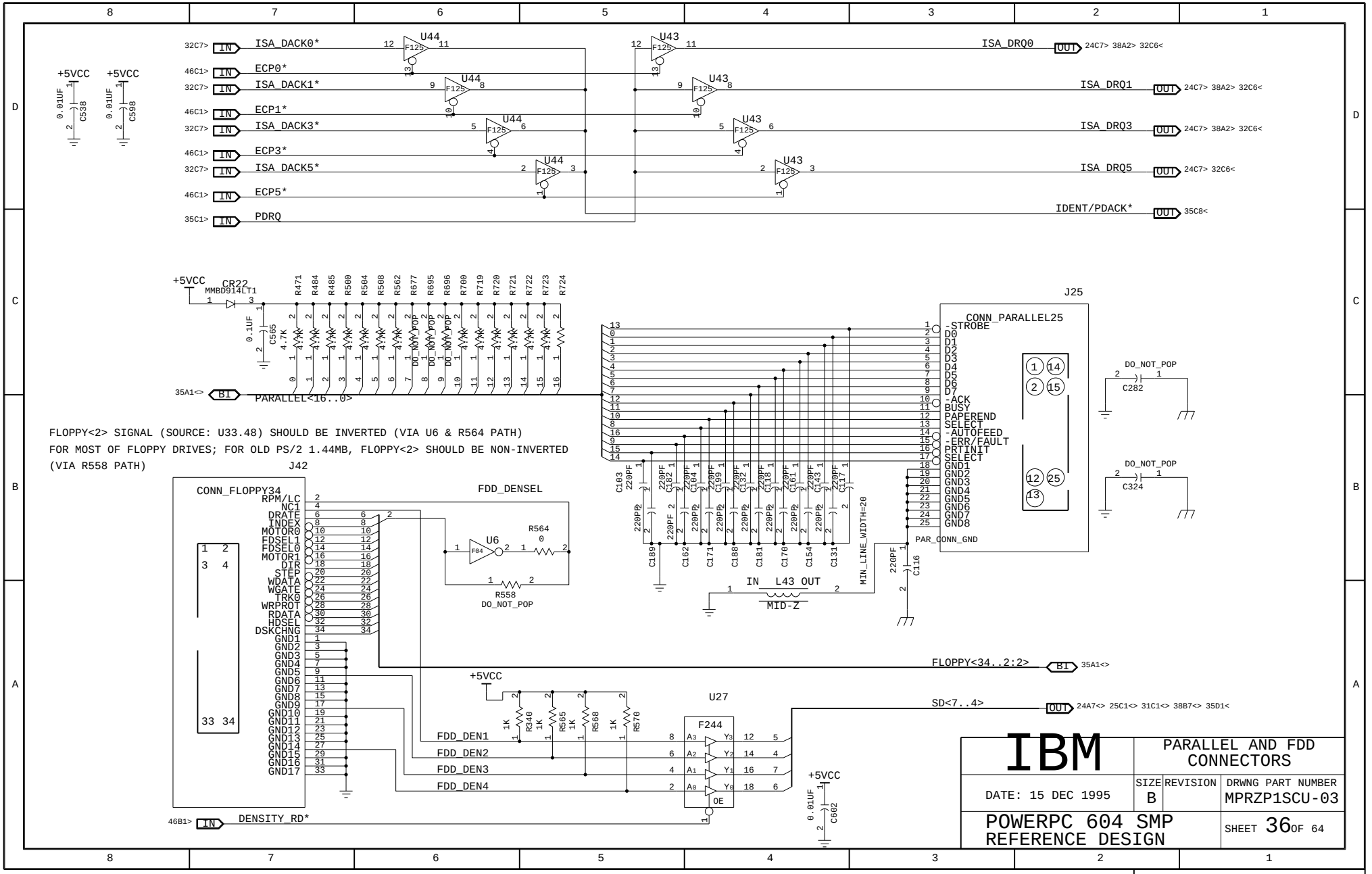
MOTHERBOARD



IBM	XIORW BUFFER		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 34 OF 64		

MOTHERBOARD


U33
SUPER I/O
PC87332
VDDB VDDC
VSSB VSSC VSSD VSSE
+5VCC
SA<10..0>
SD<7..0>
Y9
OSCILLATOR
24.0MHZ
24MHZ_SUPERIO
OSC24MHZ_O
R567
33
ISA_RESET
ISA_DACK2*
ISA_TC
DO_NOT_POP
SUPERIO_TC
U6
R301
R544
R531
ISA_IOW*
ISA_IOR*
ISA_AEN
SUPERIO_DRV2*
IDENT/PDACK*
ISA_IOCS16*
RI2*
DTR2*
CTS2*
SIN2
DSR2*
DCD2*
RI1*
CTS1*
SIN1
DSR1*
DCD1*
ERR/HDSEL
SLCT/WGATE*
PE/WDATA*
CLK48/HDCS1*
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
X1/OSC
X2
MR
FDACK
TC
WR
RD
AEN
DSKCHG
RDATA
WP
TRK0
INDEX
DRV2
IDENT/PDACK*
IOCS16
RI2
DTR2/VLD1
CTS2
SIN2
DSR2
DCD2
RI1
CTS1
SIN1
DSR1
DCD1
D7
D6
D5
D4
D3
D2
D1
D0
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
PWDN/CSOUT/ZWS
FDRQ
PDRQ
IOCHRDY/MFM
HDSEL
WGATE
WDATA
STEP
DIR
MTR0
MTR1
DR0
DR1
DENSEL
DRATE1
DRATE0
IDELO/BADDR0
HCS0*/BADDR1
IDEHI/VLD0*
IDED7
SOUT2/BOUT2/CFG0
DTR1/CFG2
SOUT1/BOUT1/CFG3
RTS1*/CFG4
RTS2/CFG1
AFD/DSTRB/DENSEL
INIT/DIR
SLIN/STEP/ASTRB
STB/WRITE
PD7/MSEN1
PD6
PD5/MSEN0
PD4/DSKCHG*
PD3/RDATA*
PD2/WP*
PD1/TRK0*
PD0/INDEX*
BSY/WAIT*/MTR1*
ACK/DR1
ISA_0WS*
ISA_DRQ2
ISA_IOCHRDY
FD_MTR_EN*
SOUT2*
DTR1*
SOUT1*
RTS1*
RTS2*
PARALLEL<16..0>
FLOPPY<34..2:2>
TC ACTIVE HIGH FOR AT MODE (IDENT=0, MFM=0)
TC ACTIVE HIGH FOR MOD 30 MODE (IDENT=1, MFM=1 OR NC)
TC ACTIVE LOW FOR PS/2 MODE (IDENT=1, MFM=1 OR NC)
IBM
SUPER I/O
PARALLEL AND FDD
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 35 OF 64
MOTHERBOARD

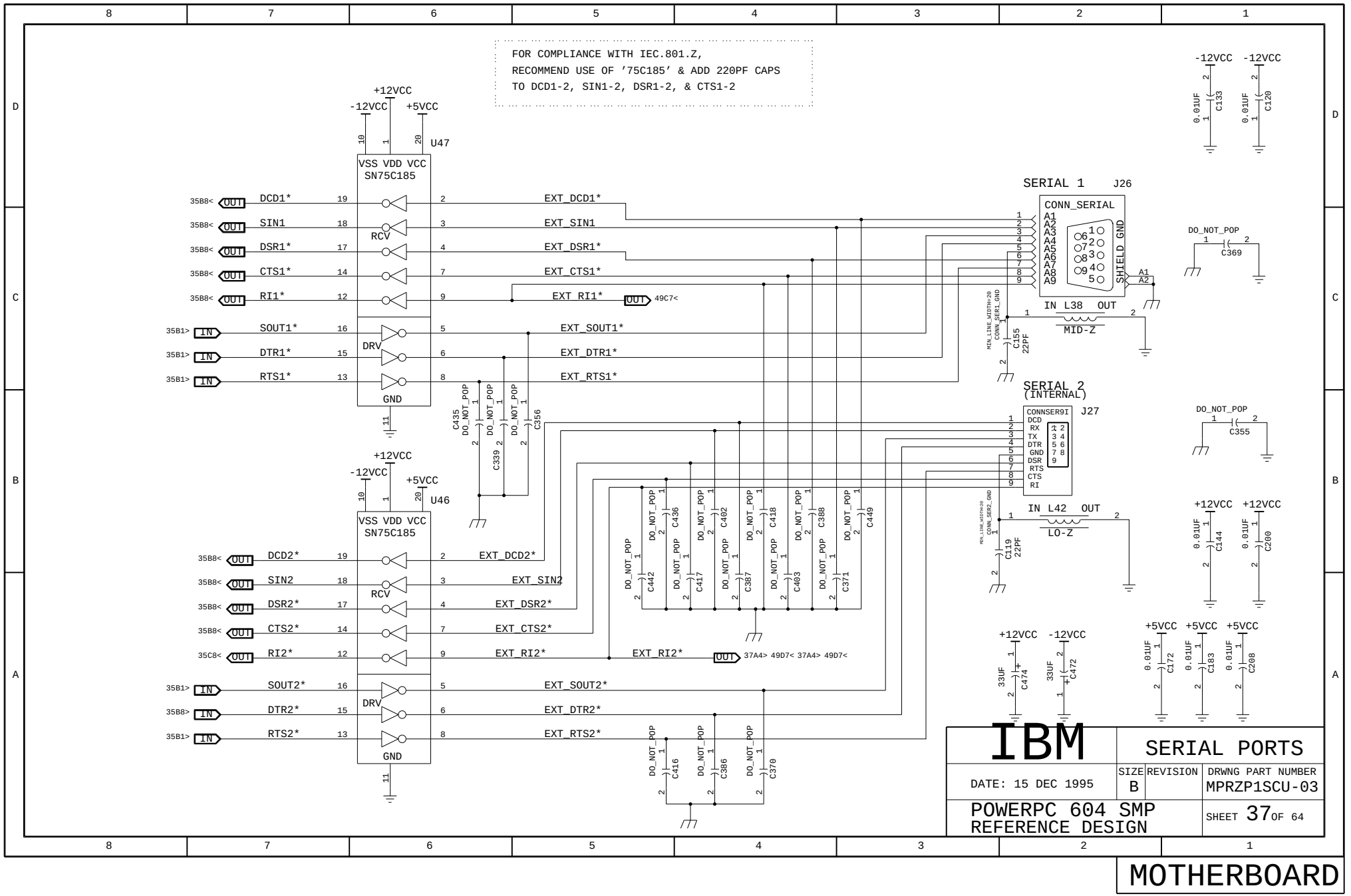


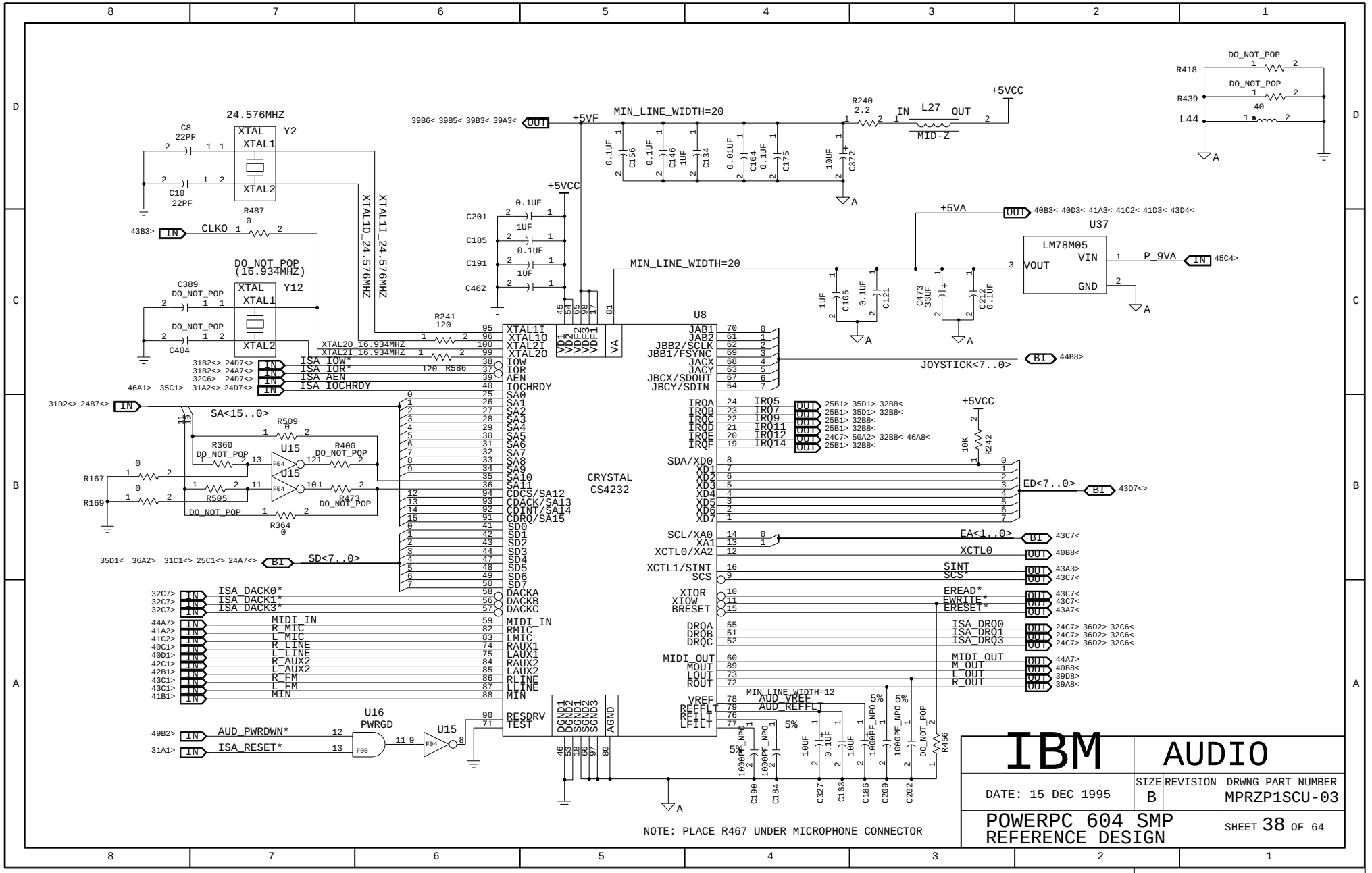
IBM

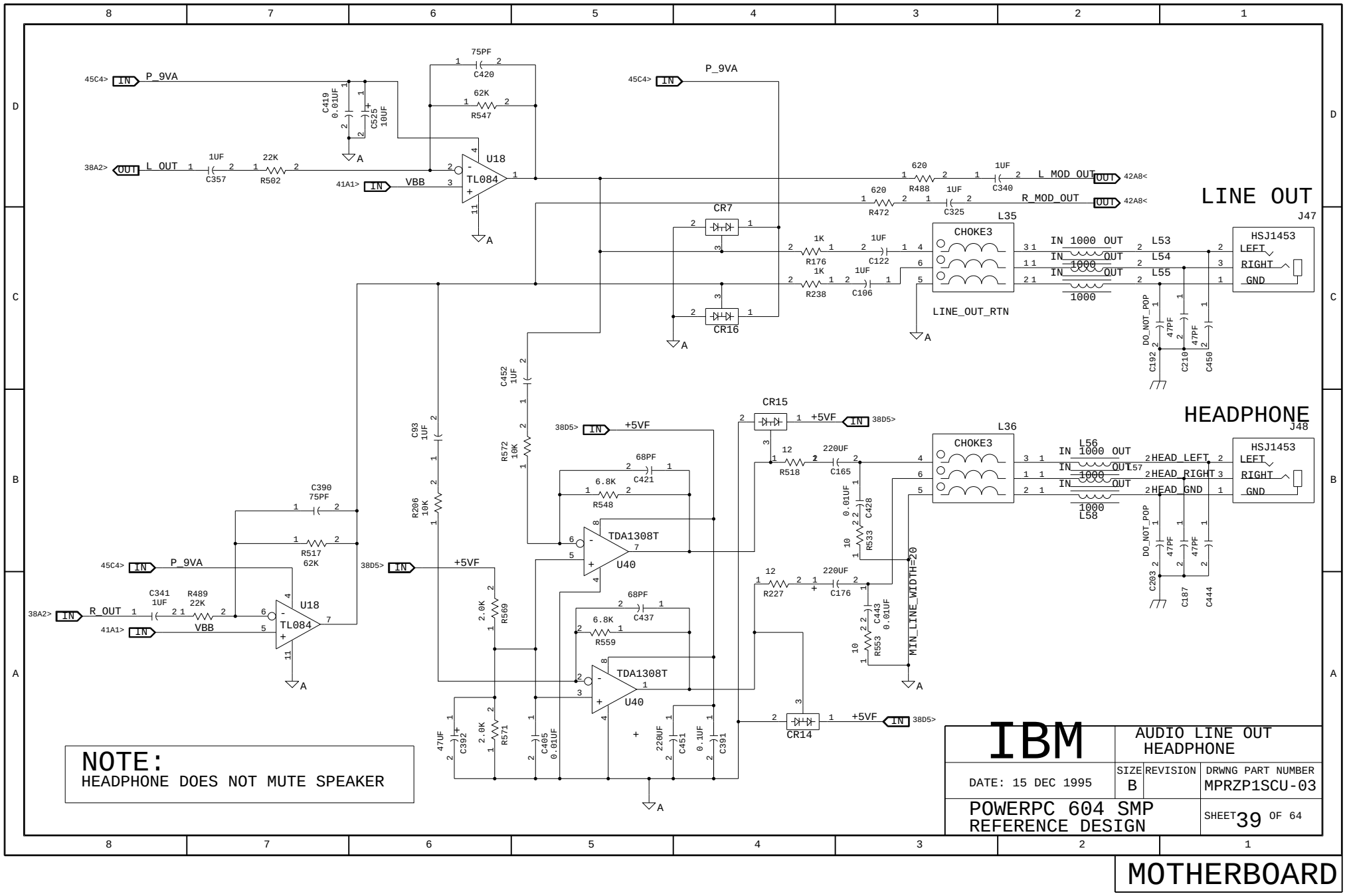
PARALLEL AND FDD CONNECTORS

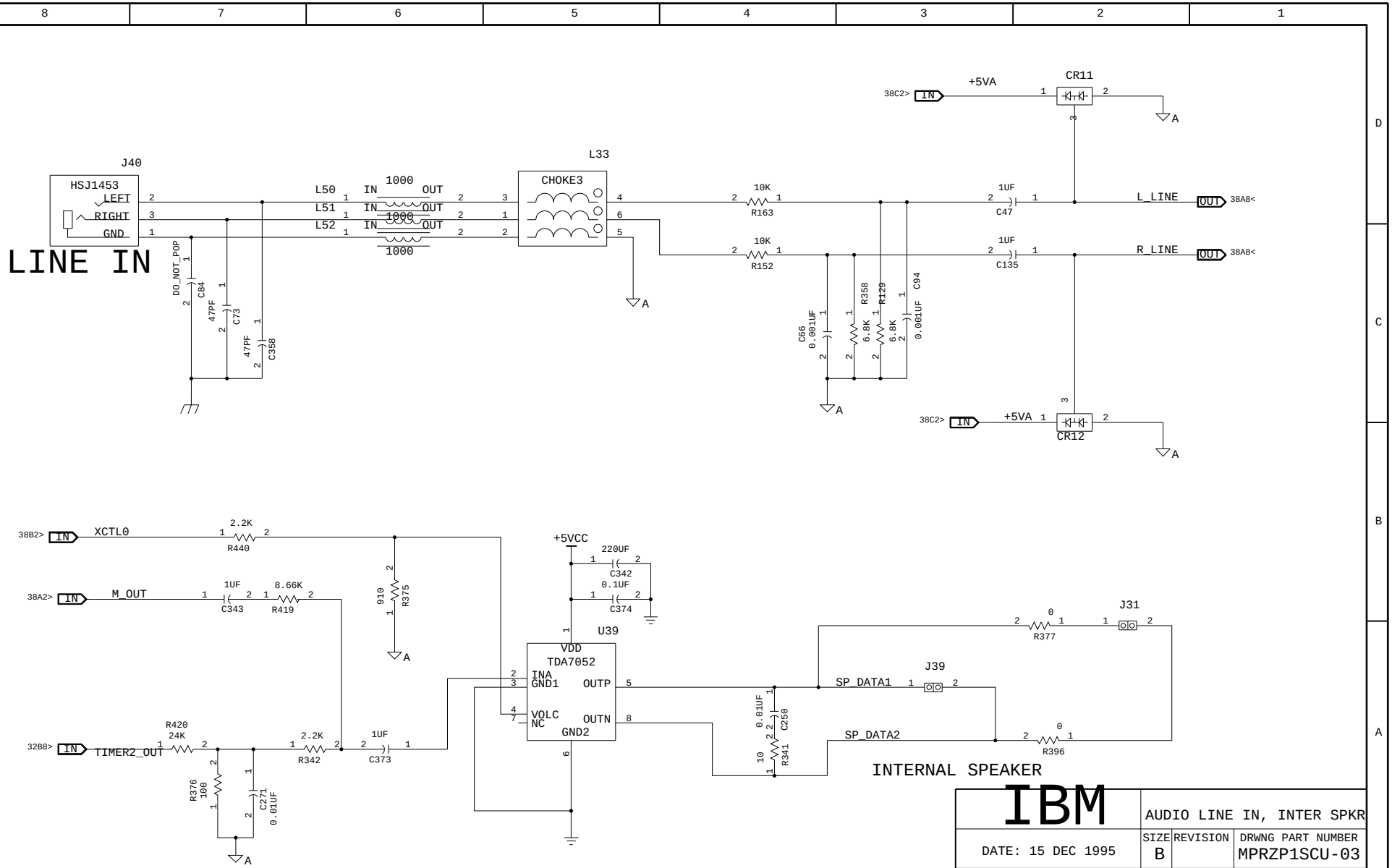
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 36 OF 64

MOTHERBOARD


FOR COMPLIANCE WITH IEC.801.Z,
RECOMMEND USE OF '75C185' & ADD 220PF CAPS
TO DCD1-2, SIN1-2, DSR1-2, & CTS1-2
U47
U46
SN75C185
VSS VDD VCC
RCV
DRV
GND
+12VCC
-12VCC
+5VCC
DCD1*
SIN1
DSR1*
CTS1*
RI1*
SOUT1*
DTR1*
RTS1*
DCD2*
SIN2
DSR2*
CTS2*
RI2*
SOUT2*
DTR2*
RTS2*
EXT_DCD1*
EXT_SIN1
EXT_DSR1*
EXT_CTS1*
EXT_RI1*
EXT_SOUT1*
EXT_DTR1*
EXT_RTS1*
EXT_DCD2*
EXT_SIN2
EXT_DSR2*
EXT_CTS2*
EXT_RI2*
EXT_SOUT2*
EXT_DTR2*
EXT_RTS2*
SERIAL 1 J26
CONN_SERIAL
SHIELD GND
IN L38 OUT
MID-Z
SERIAL 2
(INTERNAL)
CONNSER9I
J27
IN L42 OUT
LO-Z
DO_NOT_POP
0.01UF
33UF
22PF
MOTHERBOARD
IBM
SERIAL PORTS
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 37 OF 64


24.576MHZ
Y2
XTAL1
XTAL2
C8 22PF
C10 22PF
R487 0
CLKO
XTAL1O_24.576MHZ
XTAL1I_24.576MHZ
DO_NOT_POP (16.934MHZ)
Y12
C389 DO_NOT_POP
C404 DO_NOT_POP
R241 120
XTAL2O_16.934MHZ
XTAL2I_16.934MHZ
R586 120
ISA_IOW*
ISA_IOR*
ISA_AEN
ISA_IOCHRDY
SA<15..0>
R509 0
R360 DO_NOT_POP
R400 DO_NOT_POP
R167 0
R169 0
R505
R473 DO_NOT_POP
R364 0
U15
SD<7..0>
ISA_DACK0*
ISA_DACK1*
ISA_DACK3*
MIDI_IN
R_MIC
L_MIC
R_LINE
L_LINE
R_AUX2
L_AUX2
R_FM
L_FM
MIN
U16 PWRGD
AUD_PWRDWN*
ISA_RESET*
RESDRV
TEST
CRYSTAL CS4232
XTAL1I
XTAL1O
XTAL2I
XTAL2O
IOW
IOR
AEN
IOCHRDY
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
CDCS/SA12
CDACK/SA13
CDINT/SA14
CDRQ/SA15
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
DACKA
DACKB
DACKC
MIDI_IN
RMIC
LMIC
RAUX1
LAUX1
RAUX2
LAUX2
RLINE
LLINE
MIN
RESDRV
TEST
VD1
VD2
VD3
VD4
VD5
VA
DGND1
DGND2
DGND3
SGND2
SGND3
AGND
+5VF
MIN_LINE_WIDTH=20
R240 2.2
L27 MID-Z
C156 0.1UF
C146 1UF
C134
C164 0.01UF
C175 0.1UF
C372 10UF
+5VCC
C201 0.1UF
C185 1UF
C191 0.1UF
C462 1UF
U8
JAB1
JAB2
JBB2/SCLK
JBB1/FSYNC
JACX
JACY
JBCX/SDOUT
JBCY/SDIN
JOYSTICK<7..0>
IRQA
IRQB
IRQC
IRQD
IRQE
IRQF
IRQ5
IRQ7
IRQ9
IRQ11
IRQ12
IRQ14
SDA/XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
ED<7..0>
SCL/XA0
XA1
XCTL0/XA2
XCTL1/SINT
SCS
XIOR
XIOW
BRESET
DRQA
DRQB
DRQC
MIDI_OUT
MOUT
LOUT
ROUT
EA<1..0>
XCTL0
SINT
SCS*
EREAD*
EWRITE*
ERESET*
ISA_DRQ0
ISA_DRQ1
ISA_DRQ3
M_OUT
L_OUT
R_OUT
VREF
REFFLT
REFILT
LFILT
AUD_VREF
AUD_REFFLT
MIN_LINE_WIDTH=12
5%
1000PF_NPO
10UF
0.1UF
R456 DO_NOT_POP
C190
C184
C327
C163
C186
C209
C202
+5VA
U37
LM78M05
VIN
VOUT
GND
P_9VA
C105 1UF
C121 0.1UF
C473 330UF
C212 0.1UF
R242 10K
R418 DO_NOT_POP
R439 DO_NOT_POP
40
L44
NOTE: PLACE R467 UNDER MICROPHONE CONNECTOR
IBM
AUDIO
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN
SHEET 38 OF 64
MOTHERBOARD


LINE OUT
HEADPHONE
J47
J48
HSJ1453
LEFT
RIGHT
GND
CHOKE3
L35
L36
L53
L54
L55
L56
L57
L58
IN 1000 OUT
1000
L_MOD_OUT
R_MOD_OUT
LINE_OUT_RTN
HEAD_LEFT
HEAD_RIGHT
HEAD_GND
DO_NOT_POP
CR7
CR16
CR15
CR14
U18
TL084
U40
TDA1308T
L_OUT
R_OUT
VBB
P_9VA
+5VF
MIN_LINE_WIDTH=20
NOTE:
HEADPHONE DOES NOT MUTE SPEAKER
IBM
AUDIO LINE OUT
HEADPHONE
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 39 OF 64
MOTHERBOARD

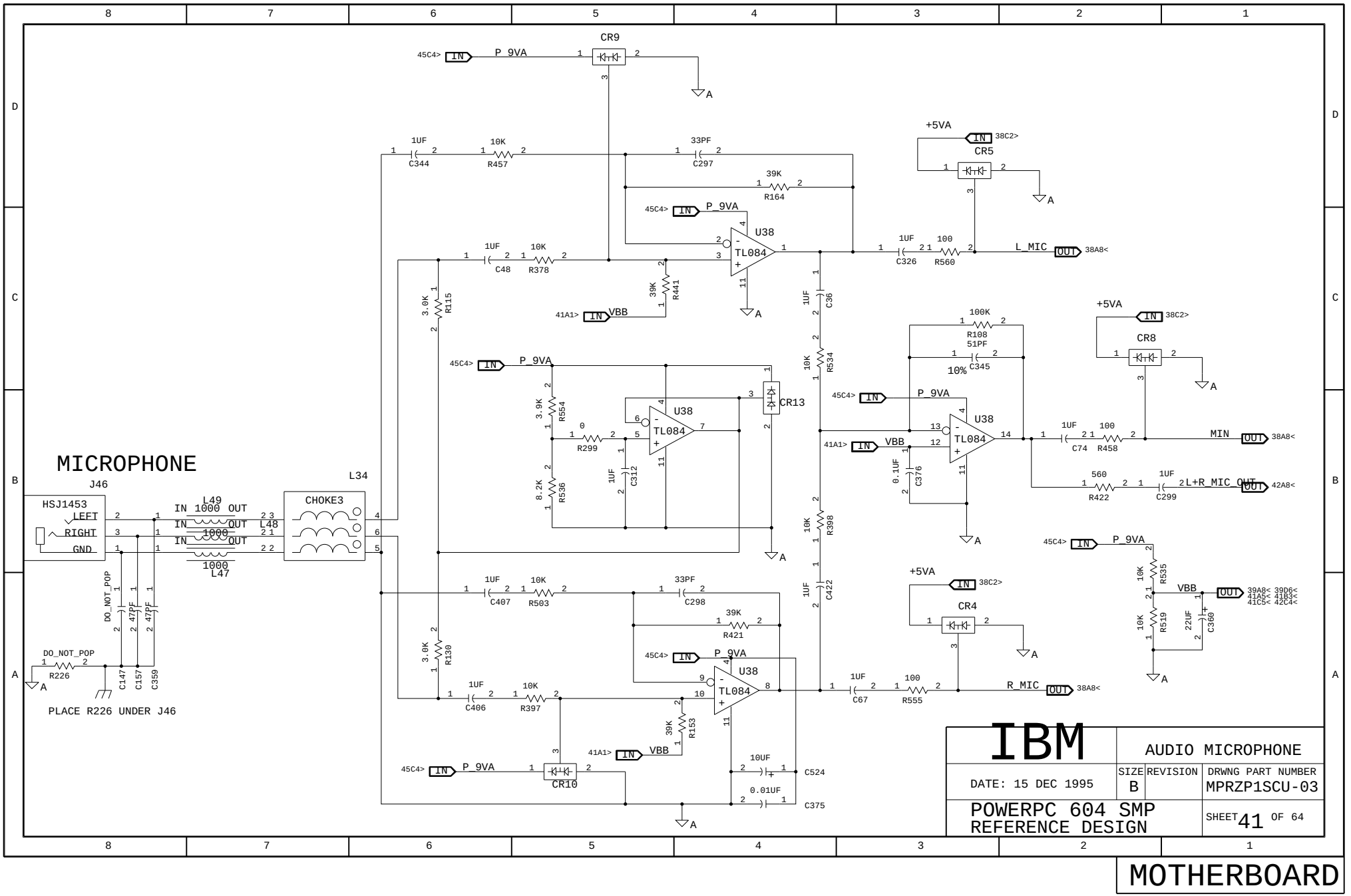


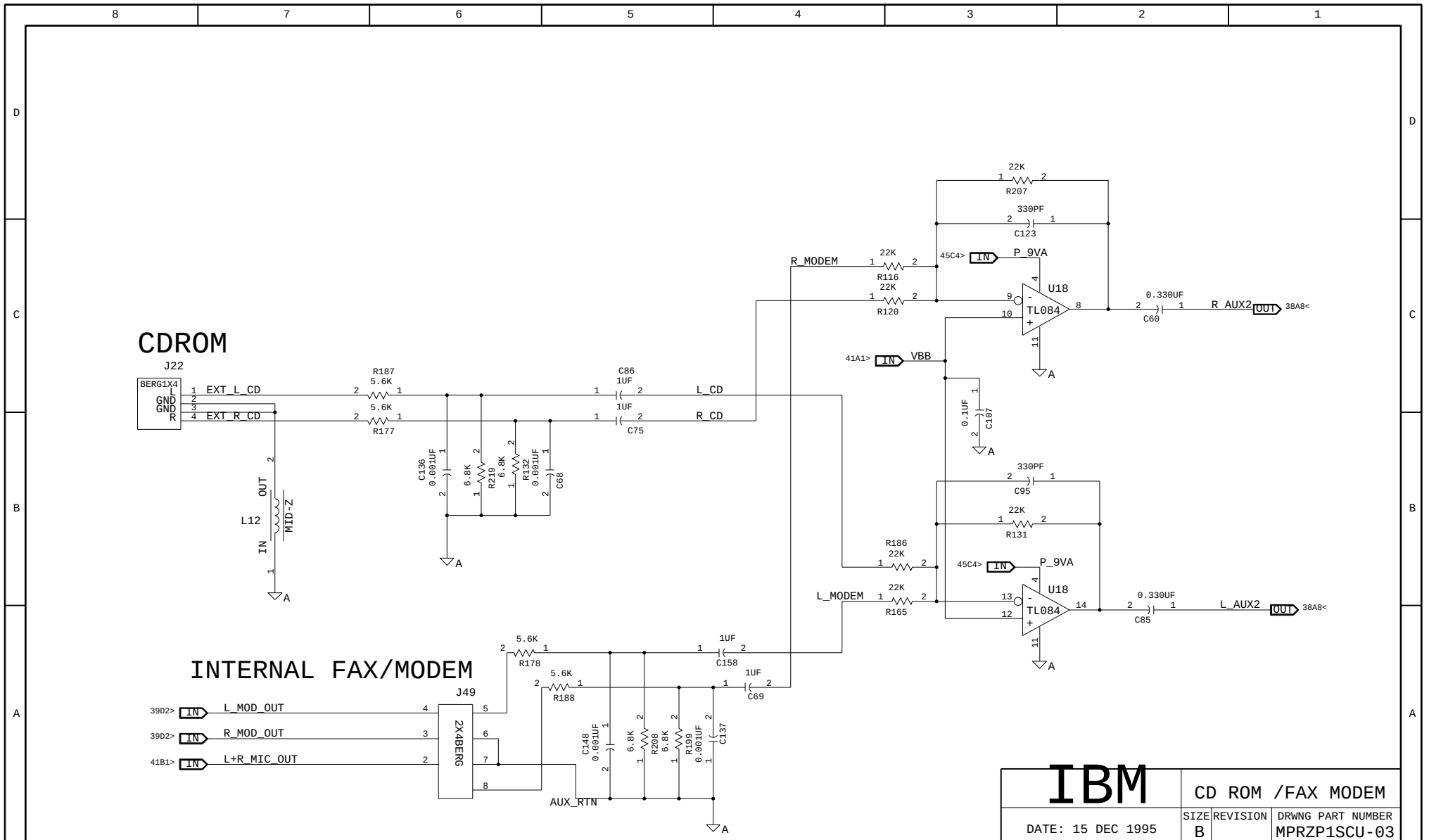
IBM

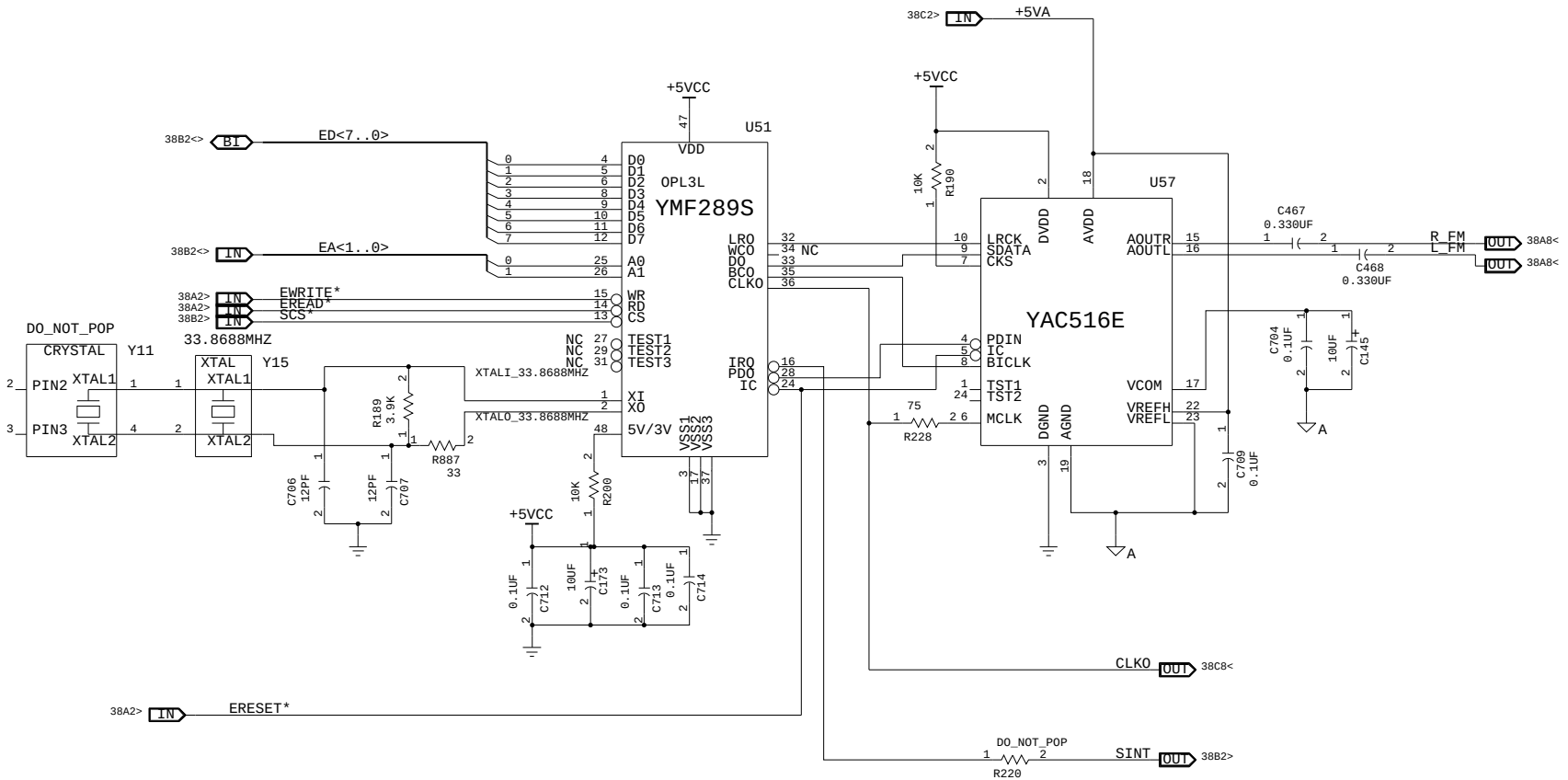
AUDIO LINE IN, INTER SPKR

DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 40 OF 64

MOTHERBOARD

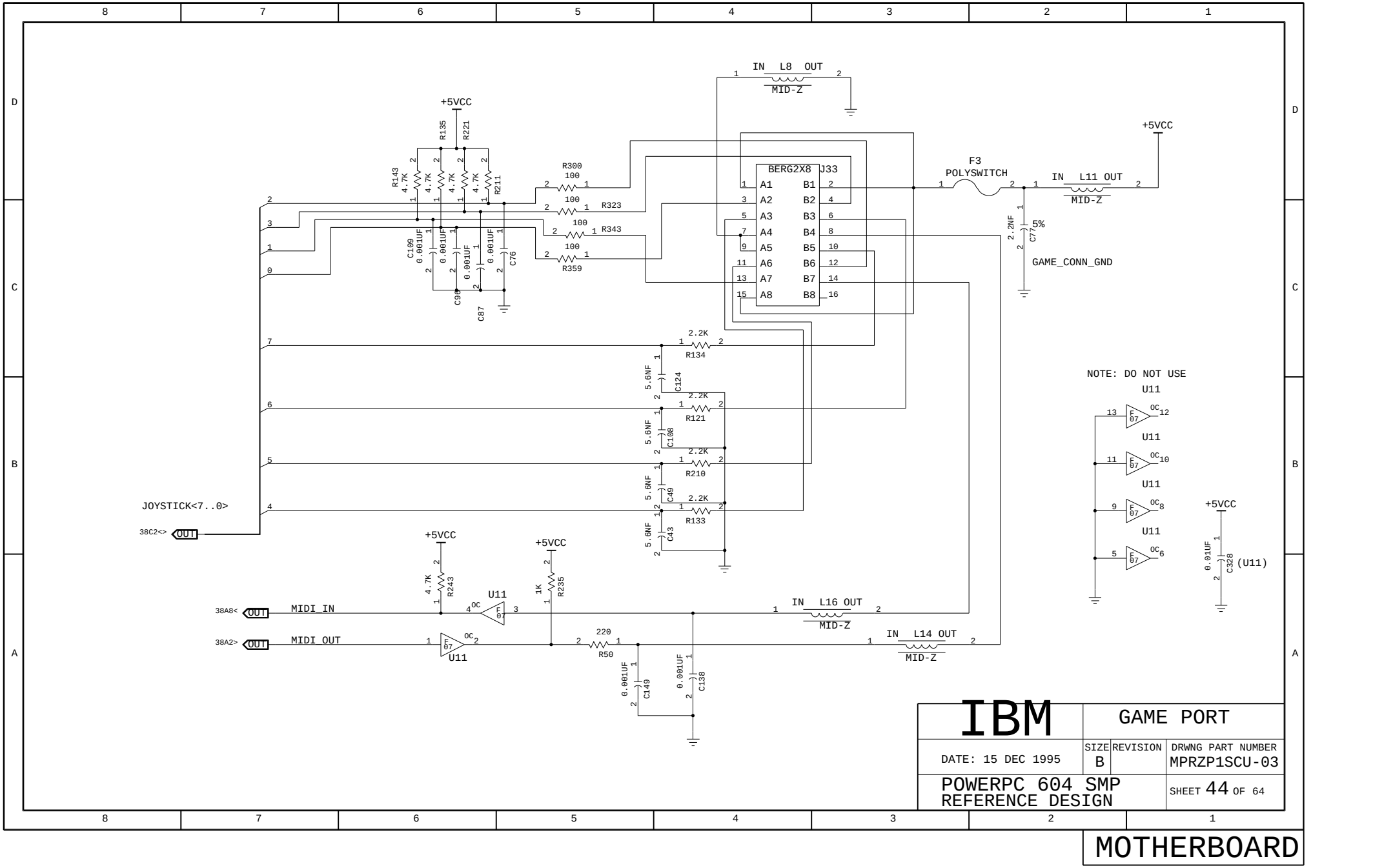

MICROPHONE
J46
HSJ1453
LEFT
RIGHT
GND
L49
L48
L47
1000
CHOKE3
L34
DO_NOT_POP
R226
PLACE R226 UNDER J46
CR9
CR5
CR8
CR4
CR10
CR13
U38
TL084
P_9VA
VBB
+5VA
L_MIC
R_MIC
MIN
L+R_MIC_OUT
IBM
AUDIO MICROPHONE
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 41 OF 64
MOTHERBOARD


CDROM
J22
BERG1X4
EXT_L_CD
EXT_R_CD
R187
5.6K
R177
C86
1UF
C75
L_CD
R_CD
C136
0.001UF
R219
6.8K
R132
C68
L12
MID-Z
R_MODEM
L_MODEM
22K
R207
330PF
C123
R116
R120
P_9VA
U18
TL084
0.330UF
C60
R_AUX2
VBB
0.1UF
C107
C95
R131
R186
R165
C85
L_AUX2
INTERNAL FAX/MODEM
J49
2X4BERG
L_MOD_OUT
R_MOD_OUT
L+R_MIC_OUT
R178
R188
C158
C69
C148
R208
R199
C137
AUX_RTN
IBM
CD ROM /FAX MODEM
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 42 OF 64
MOTHERBOARD



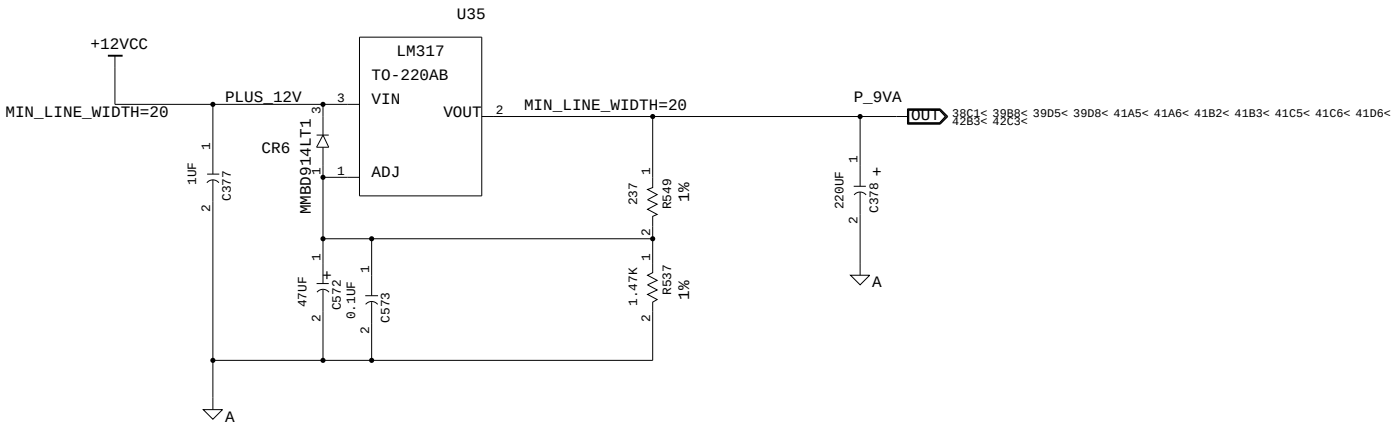
IBM	AUDIO		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 43 OF 64		

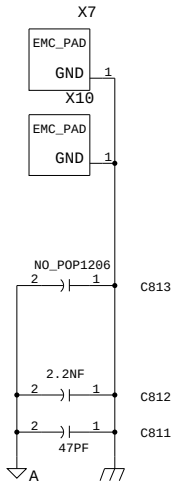
MOTHERBOARD



IBM	GAME PORT		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 44 OF 64		

MOTHERBOARD





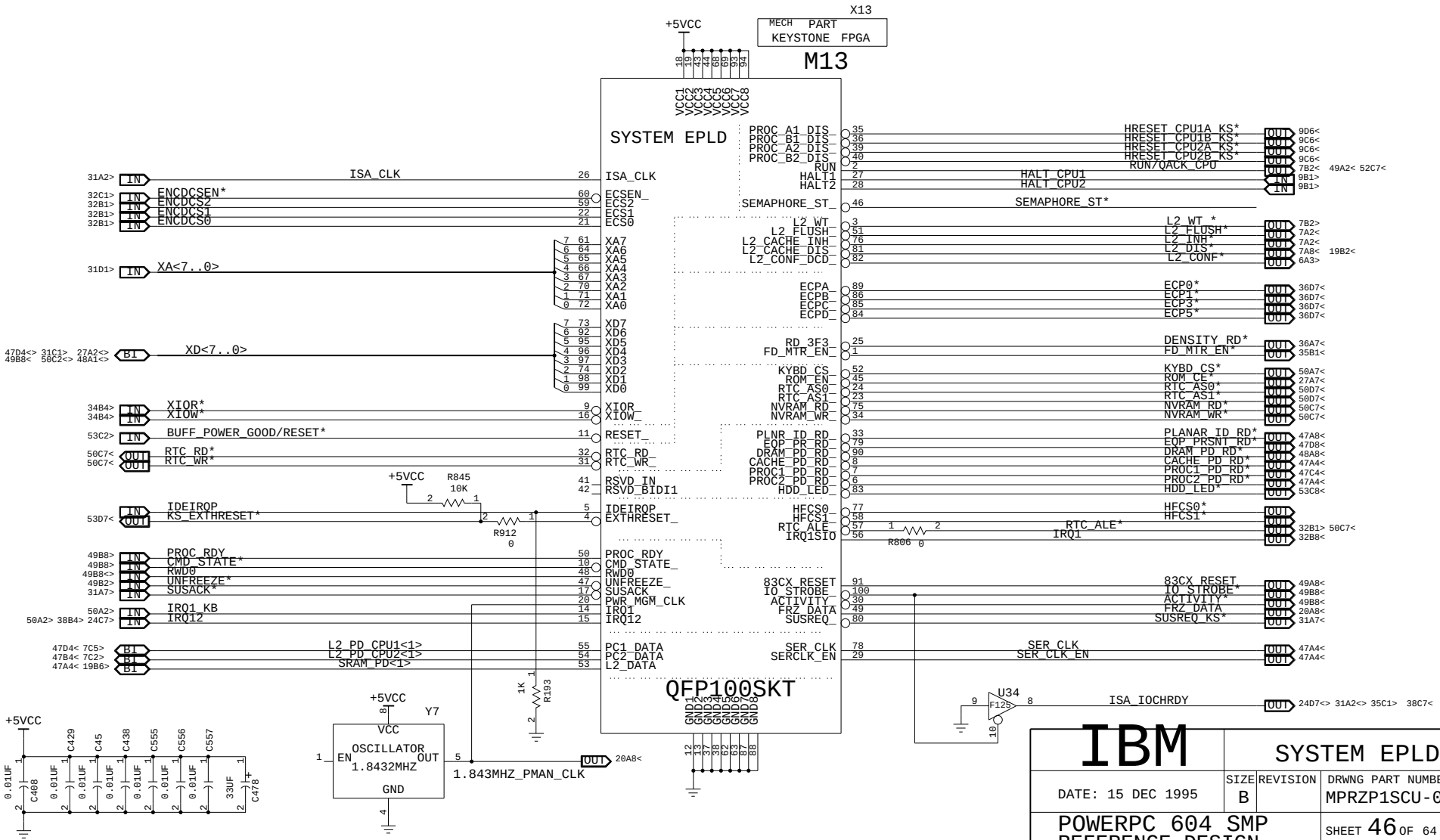
PLACE EMC_PAD AT AUDIO JACKS

PLACE C813 AT AUDIO MOUNTING HOLE

IBM	AUDIO +9V REGULATION		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 45 OF 64		

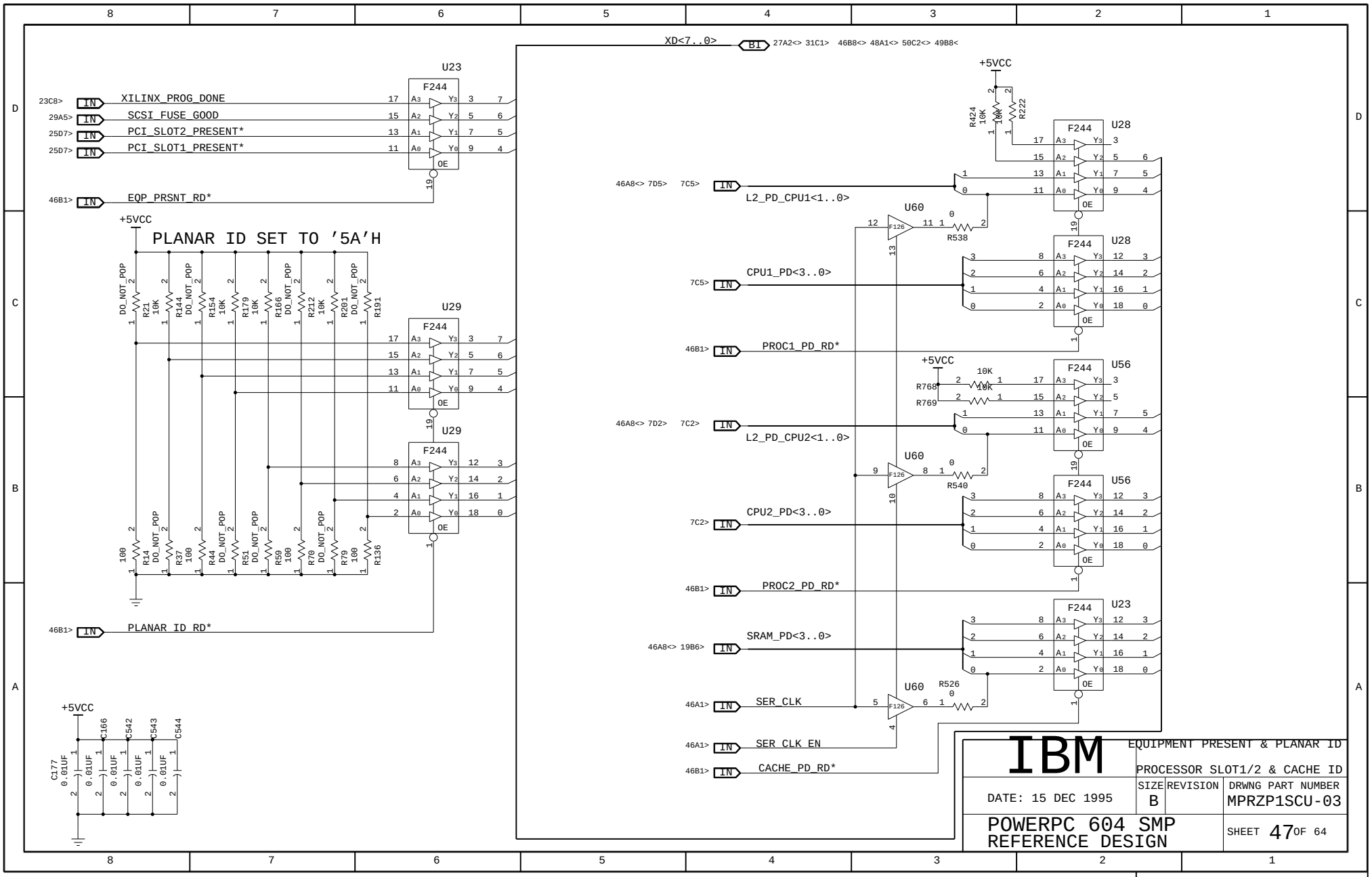
MOTHERBOARD

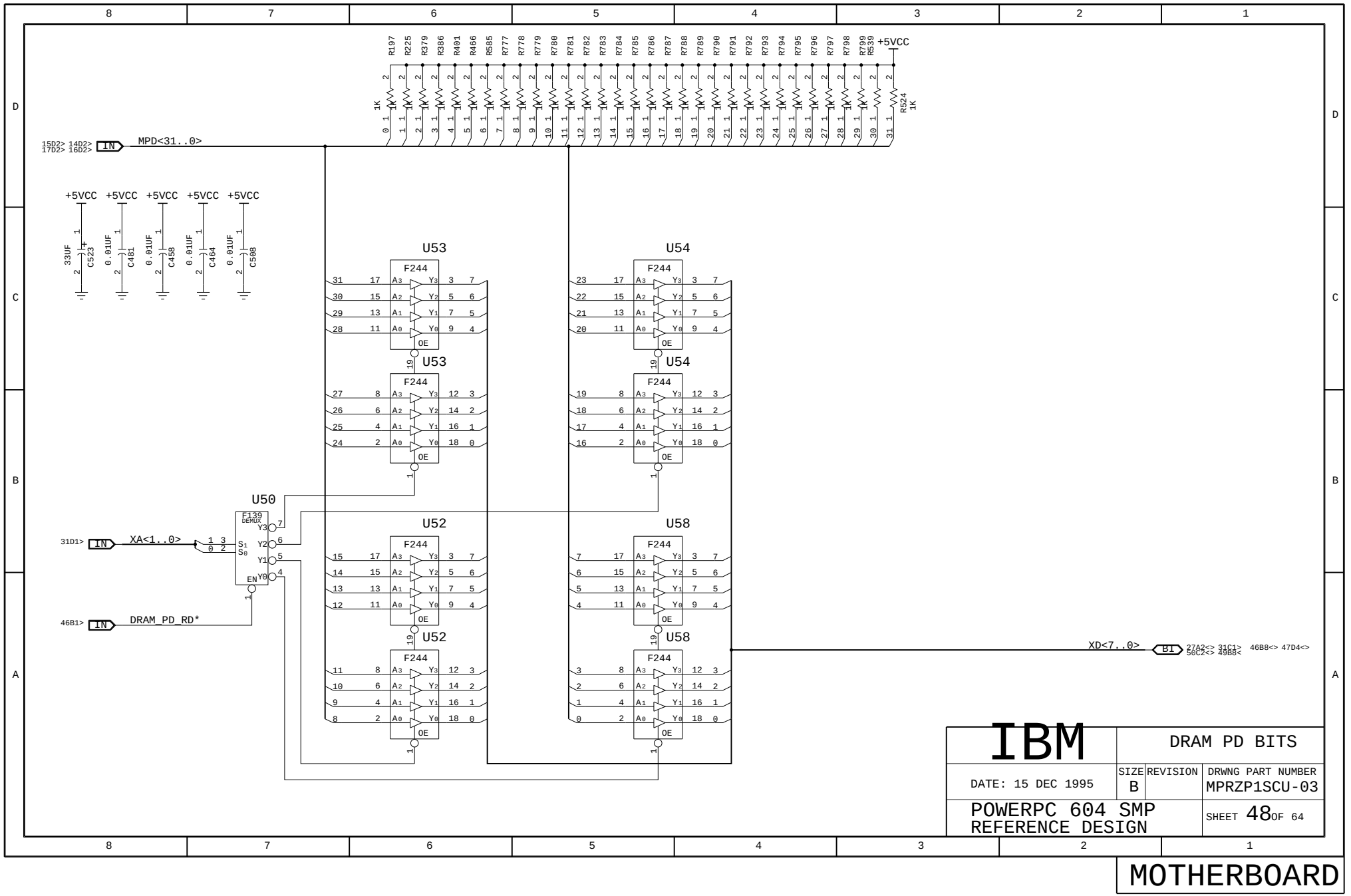
SYSTEM EPLD



IBM	SYSTEM EPLD		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 46 OF 64		

MOTHERBOARD


XD<7..0>
B1
27A2<> 31C1> 46B8<> 48A1<> 50C2<> 49B8<
U23
F244
23C8>
IN
XILINX_PROG_DONE
29A5>
SCSI_FUSE_GOOD
25D7>
PCI_SLOT2_PRESENT*
25D7>
PCI_SLOT1_PRESENT*
46B1>
EQP_PRSNT_RD*
+5VCC
PLANAR ID SET TO '5A'H
DO_NOT_POP
R21 10K
R144
R154 10K
R179 10K
R166
R212 10K
R201
R191
U29
R14 100
R37 100
R44
R51
R59 100
R70
R79 100
R136
46B1>
PLANAR ID RD*
C177 0.01UF
C166 0.01UF
C542 0.01UF
C543 0.01UF
C544 0.01UF
U28
U56
U60
F126
R424 10K
R222 10K
R538
R768 10K
R769 10K
R540
R526
46A8<> 7D5>
7C5>
L2_PD_CPU1<1..0>
CPU1_PD<3..0>
PROC1_PD_RD*
46A8<> 7D2>
7C2>
L2_PD_CPU2<1..0>
CPU2_PD<3..0>
PROC2_PD_RD*
SRAM_PD<3..0>
46A8<> 19B6>
46A1>
SER_CLK
SER_CLK EN
46B1>
CACHE_PD_RD*
IBM
EQUIPMENT PRESENT & PLANAR ID
PROCESSOR SLOT1/2 & CACHE ID
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 47 OF 64
MOTHERBOARD



IBM

DRAM PD BITS

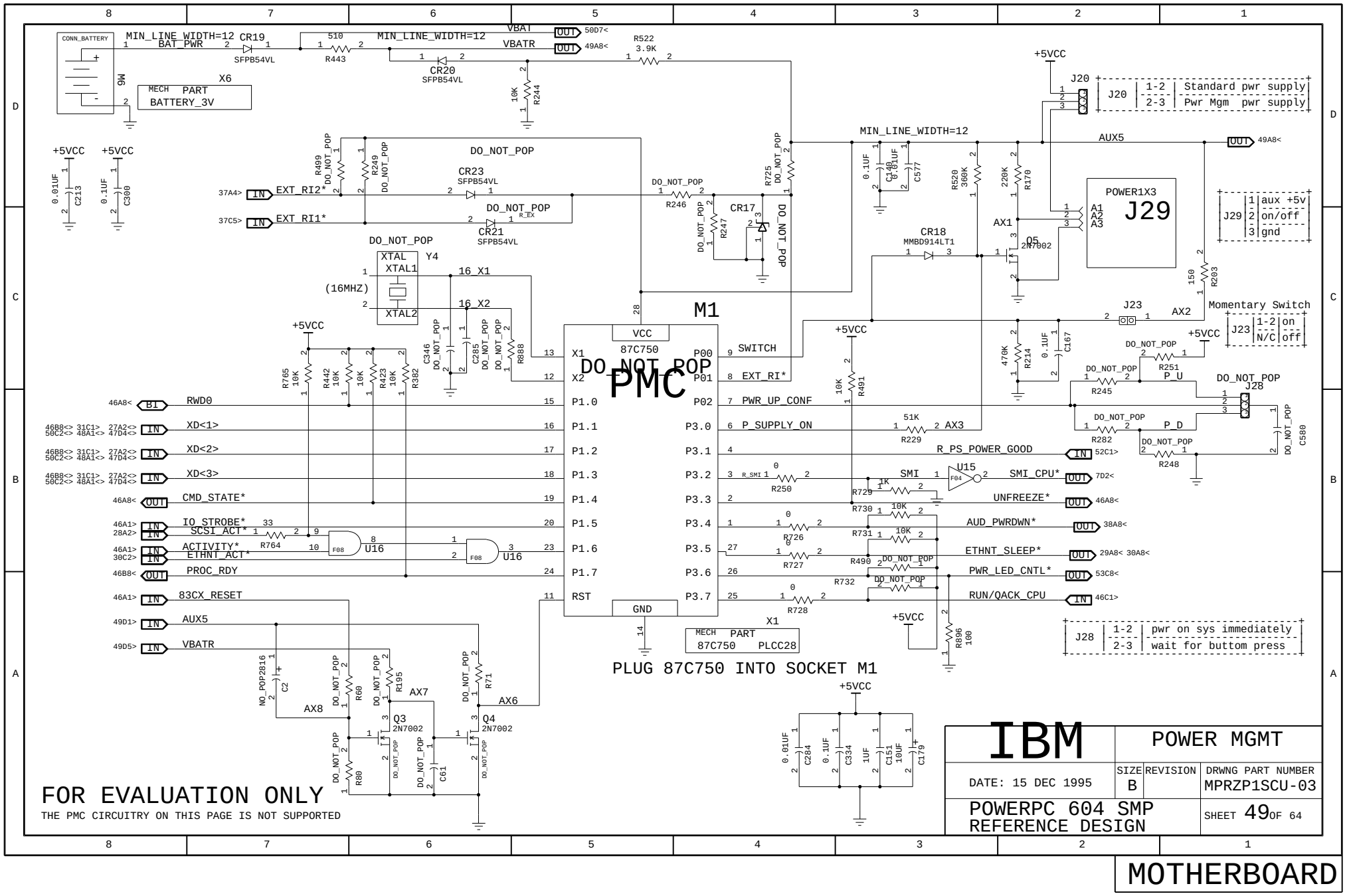
DATE: 15 DEC 1995

SIZE B | REVISION | DRWNG PART NUMBER MPRZP1SCU-03

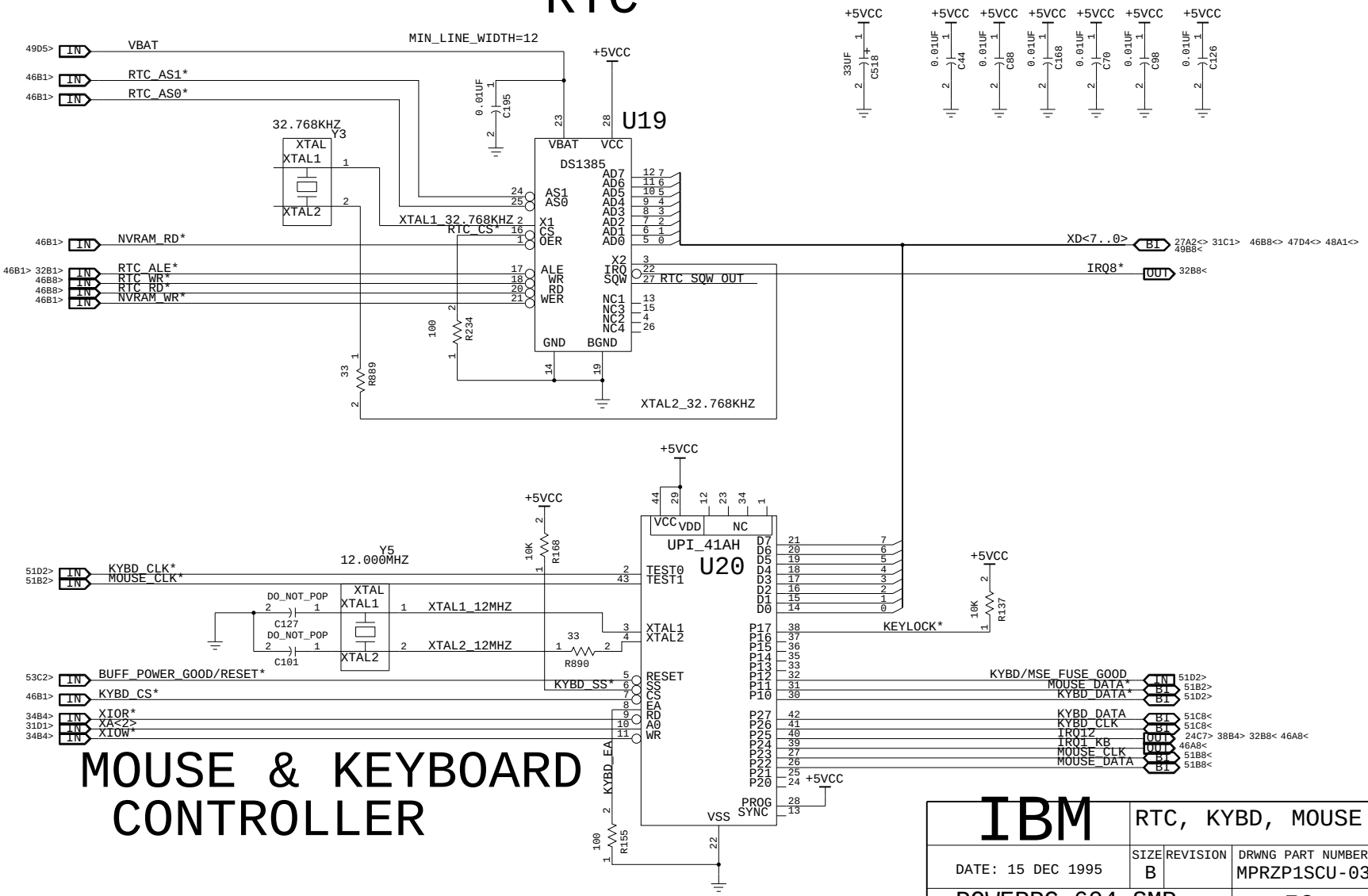
POWERPC 604 SMP
REFERENCE DESIGN

SHEET 48 OF 64

MOTHERBOARD

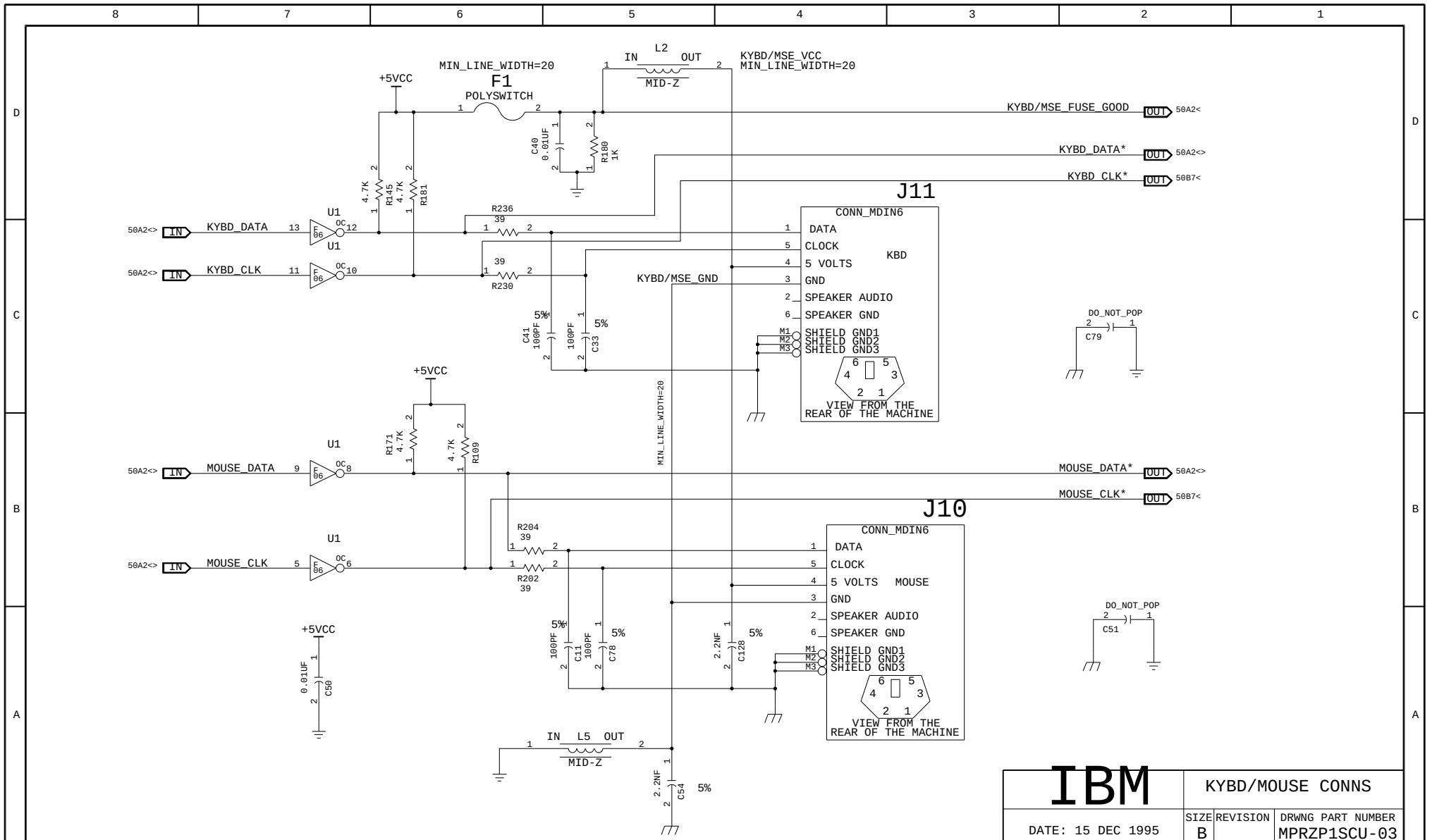

MIN_LINE_WIDTH=12
CR19
SFPB54VL
VBAT
VBATR
R443
CR20
R522
3.9K
R244
X6
MECH PART
BATTERY_3V
+5VCC
J20
AUX5
POWER1X3
J29
R499
R249
CR23
CR17
CR21
R725
R246
R247
R520
360K
R170
220K
AX1
Q5
2N7002
CR18
MMBD914LT1
R203
150
J23
AX2
Momentary Switch
J28
R251
P_U
R245
P_D
R282
R248
R491
10K
R214
470K
R229
51K
AX3
R250
SMI
U15
SMI_CPU*
UNFREEZE*
AUD_PWRDWN*
ETHNT_SLEEP*
PWR_LED_CNTL*
RUN/QACK_CPU
R729
R730
R731
R726
R727
R732
R728
R490
R896
100
XTAL
Y4
XTAL1
XTAL2
(16MHZ)
16_X1
16_X2
M1
87C750
PMC
VCC
GND
X1
MECH PART
87C750 PLCC28
P00 SWITCH
P01 EXT_RI*
P02 PWR_UP_CONF
P3.0 P_SUPPLY_ON
P3.1 R_PS_POWER_GOOD
P3.2 SMI
P3.3 UNFREEZE*
P3.4 AUD_PWRDWN*
P3.5 ETHNT_SLEEP*
P3.6 PWR_LED_CNTL*
P3.7 RUN/QACK_CPU
P1.0 RWD0
P1.1 XD<1>
P1.2 XD<2>
P1.3 XD<3>
P1.4 CMD_STATE*
P1.5 IO_STROBE*
P1.6 ACTIVITY*
P1.7 PROC_RDY
RST 83CX_RESET
SCSI_ACT*
ETHNT_ACT*
AUX5
VBATR
R765
R442
R423
R382
R808
R764
U16
AX8
AX7
AX6
Q3
2N7002
Q4
2N7002
R60
R195
R71
R80
C61
C2
C213
C300
C346
C285
C577
C140
C167
C580
C284
C334
C151
C179
J20 | 1-2 | Standard pwr supply
J20 | 2-3 | Pwr Mgm pwr supply
J29 | 1 | aux +5v
J29 | 2 | on/off
J29 | 3 | gnd
J23 | 1-2 | on
J23 | N/C | off
J28 | 1-2 | pwr on sys immediately
J28 | 2-3 | wait for buttom press
DO_NOT_POP
PLUG 87C750 INTO SOCKET M1
FOR EVALUATION ONLY
THE PMC CIRCUITRY ON THIS PAGE IS NOT SUPPORTED
IBM
POWER MGMT
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 49 OF 64
MOTHERBOARD

RTC



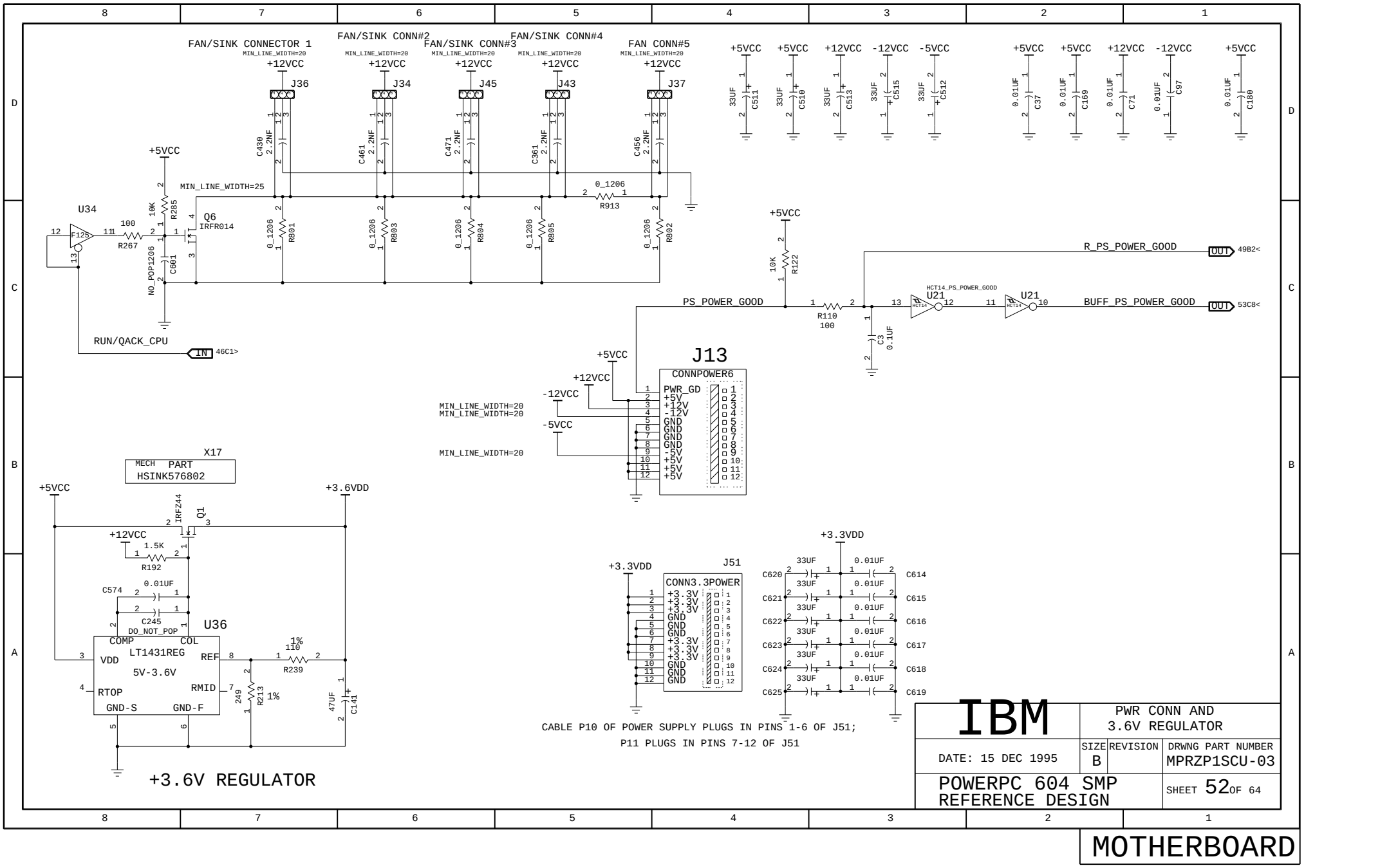
IBM	RTC, KYBD, MOUSE		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 50 OF 64		

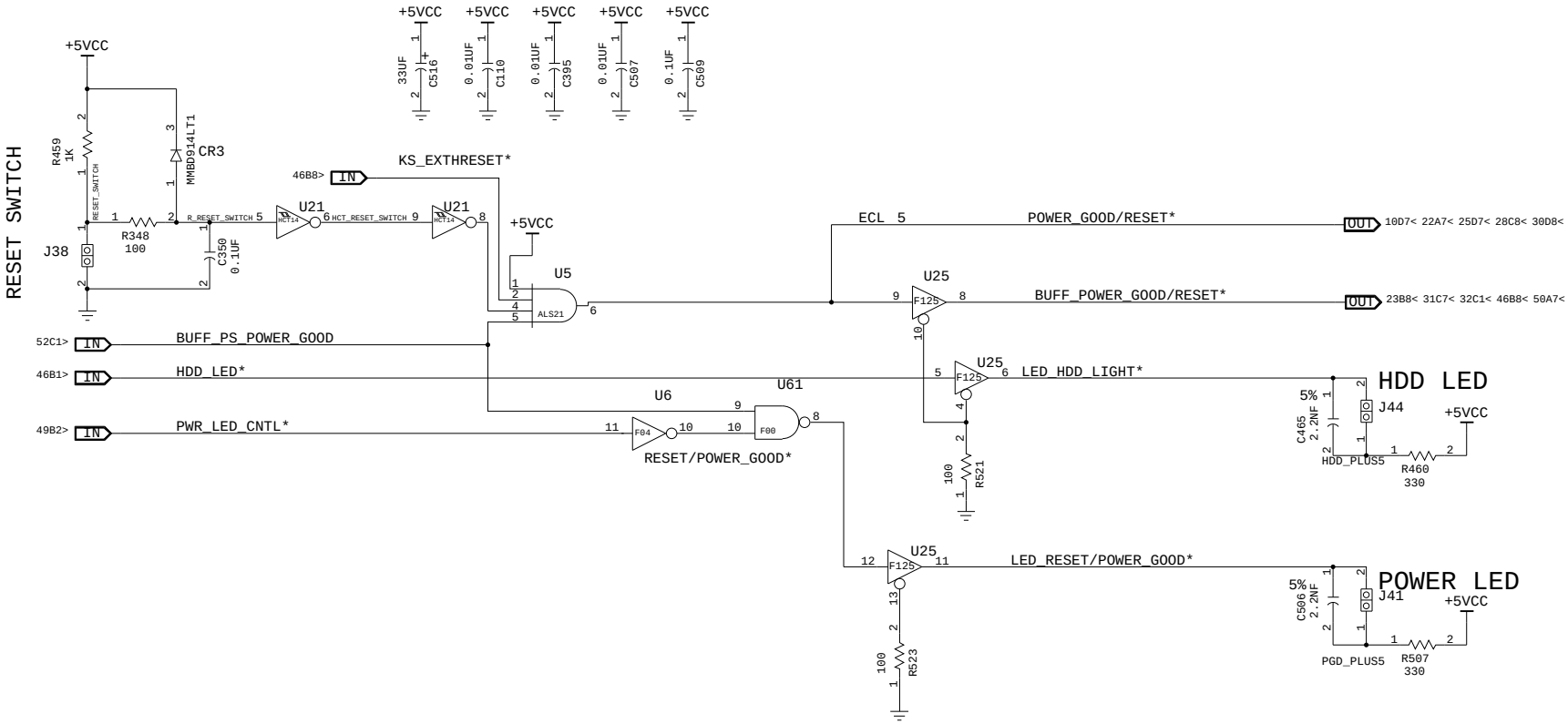
MOTHERBOARD



IBM	KYBD/MOUSE CONNS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 51 OF 64

MOTHERBOARD


FAN/SINK CONNECTOR 1
FAN/SINK CONN#2
FAN/SINK CONN#3
FAN/SINK CONN#4
FAN CONN#5
J36
J34
J45
J43
J37
+12VCC
+5VCC
MIN_LINE_WIDTH=20
MIN_LINE_WIDTH=25
U34
Q6
IRFR014
R285
R267
C601
R801
R803
R804
R805
R802
R913
RUN/QACK_CPU
46C1>
R122
R110
C3
U21
HCT14_PS_POWER_GOOD
PS_POWER_GOOD
R_PS_POWER_GOOD
BUFF_PS_POWER_GOOD
49B2<
53C8<
J13
CONNPOWER6
PWR_GD
+5V
+12V
-12V
GND
-5V
X17
MECH PART
HSINK576802
+3.6VDD
Q1
IRFZ44
U36
LT1431REG
COMP
COL
VDD
REF
RTOP
RMID
GND-S
GND-F
5V-3.6V
R192
R239
R213
C574
C245
DO_NOT_POP
C141
J51
CONN3.3POWER
+3.3VDD
+3.6V REGULATOR
CABLE P10 OF POWER SUPPLY PLUGS IN PINS 1-6 OF J51;
P11 PLUGS IN PINS 7-12 OF J51
IBM
PWR CONN AND
3.6V REGULATOR
DATE: 15 DEC 1995
SIZE B
REVISION
DRWNG PART NUMBER
MPRZP1SCU-03
POWERPC 604 SMP
REFERENCE DESIGN
SHEET 52 OF 64
MOTHERBOARD

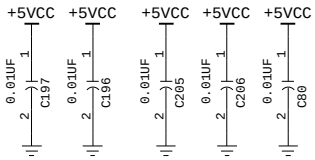


IBM	PANEL INDICATORS AND CONTROLS		
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN	SHEET 53 OF 64		

MOTHERBOARD

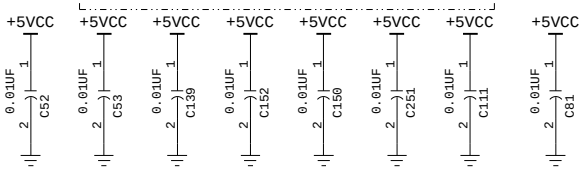
EMC CAPS

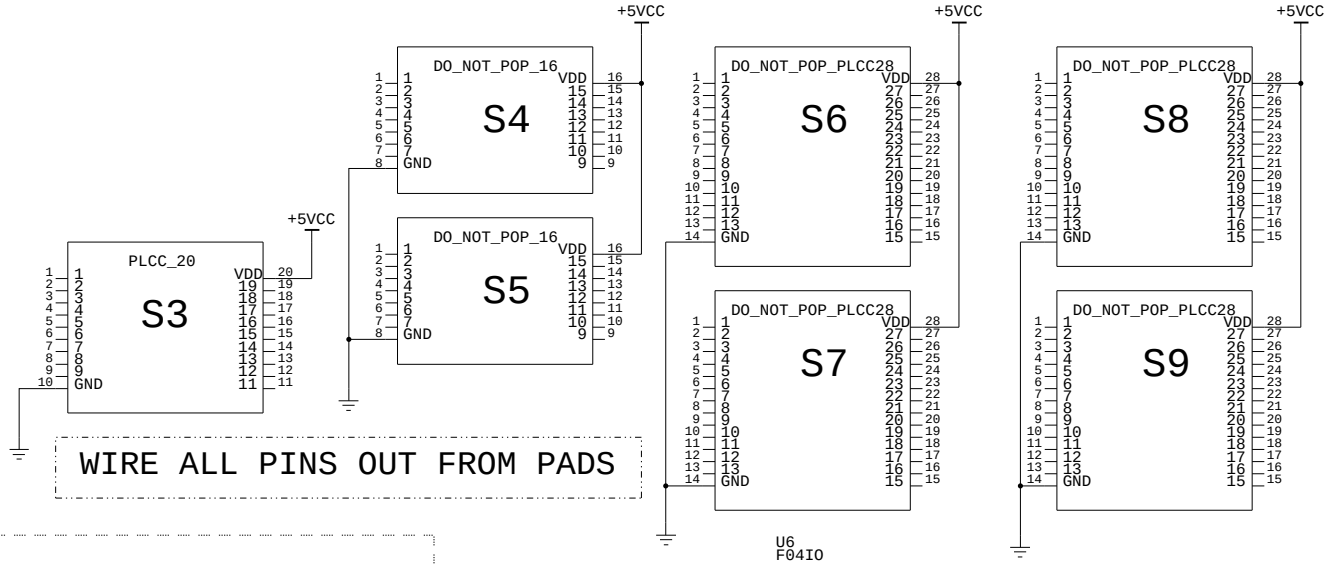
AT LEAST ONE CAP FOR EVERY SQUARE INCH OF BOARD SPACE



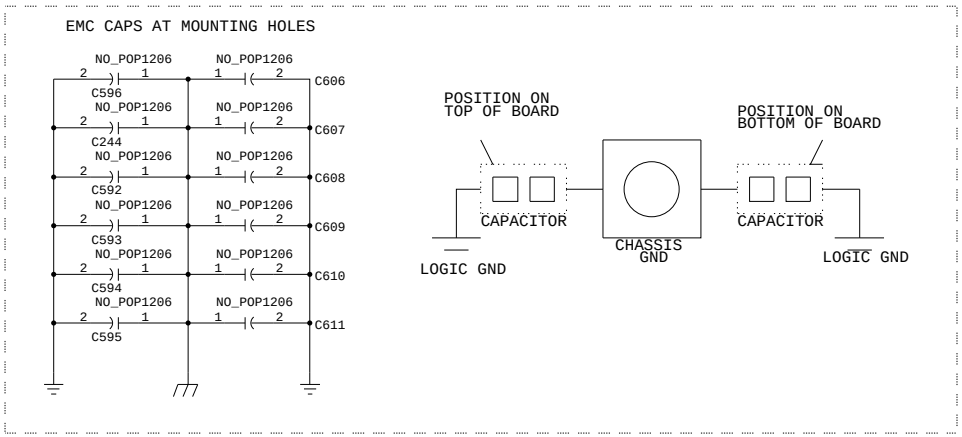
DECOUPLING CAPS

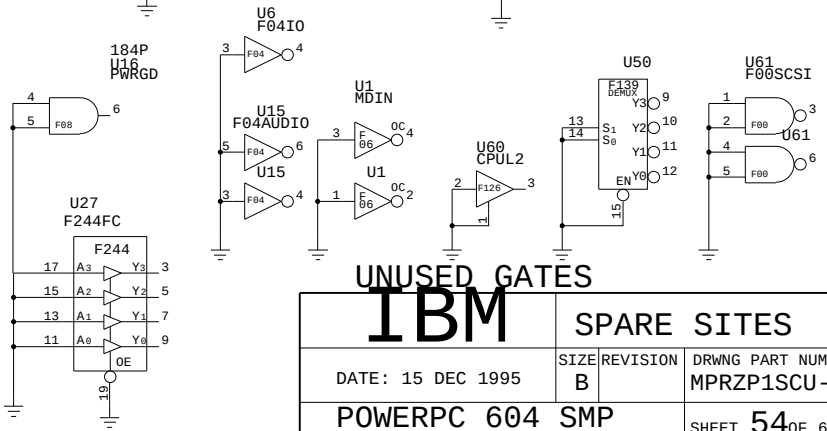
ONE PER VCC PIN ON SPARES





WIRE ALL PINS OUT FROM PADS





IBM

SPARE SITES

DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 54 OF 64

MOTHERBOARD

```
      *** Signal Cross-Reference ***
         --- for the entire design --

+5VA            38C2> 40B3< 40D3< 41A3< 41C2< 41D3<
                43D4<
+5VA_4403       21C5
+5VF            38D5> 39A3< 39B3< 39B5< 39B6<
1.843MHZ_PMAN_CLK 46A5> 20A8<
14.3181MHZ      32D7> 24C7<
16_X1           49C6
16_X2           49C6
20.00MHZ_XTAL1  30C5
20.00MHZ_XTAL2  30C5
24MHZ_SUPERIO   35D7
83CX_RESET      46A1> 49A8<
663_BCLK        20B1> 11A5<
663_CPU_PAR_ERR * 11C1> 10C7<
663_MEM_ERR *   11C1> 10C7<
663_SBE *       11C1> 10C7<
664_BCLK        20C1> 10D7<
664_PCICLK      21C1> 12B6<
970COM_FRZ *    20A6<
970EXT_FB       20A6<
970FRZ_STROBE   20A6<
970MR/3ST *     20B6<
4403_BCLK       20A1> 21C7<
4403_FBCLK      21C6
4403_FBCLK_R    21B6
AACK *          6D2<> 10C1<>
ABB *           6D2<> 33A7< 33C7<
ACTIVITY *      46A1> 49B8<
AOS_RR_MMRS     10C1> 11A5<
ARTRY *         6D2<> 10C1<>
AUD_PWRDWN *    49B2> 38A8<
AUD_REFFLT      38A4
AUD_VREF        38A4
AUX5            49D1> 49A8<
AUX_RTN         42A5
AX1             49C3
AX2             49C1
AX3             49B3
AX6             49A6
AX7             49A6
AX8             49A7
A_CPU1_ <31..0> 6B8<> 33C3<> 10B7<
A_CPU2_ <31..0> 6C2<> 19A6<
BAT_PWR         49D8
BG_CPU1 *       10D1> 33C3> 6C8< 7A8<
BG_CPU2 *       10D1> 33C3> 6C2< 7A5<
BITX            32C2
BR_CPU1 *       6D8> 7A8> 10D7< 33B7<
BR_CPU2 *       6D2> 7A5> 10D7< 33B7<
BUFF_POWER_GOOD/RESET * 53C2> 23B8< 31C7< 32C1<
                46B8< 50A7<
BUFF_PS_POWER_GOOD 52C1> 53C8<
C2P_WRL_OPEN    11B6
CACHE_PD_RD *   46B1> 47A4<
CI *            6A4
CKSTP_CPU1 *    7B5> 9D6<
CKSTP_CPU2 *    7B2> 9D6<
CKSTP_ESP *     9C8
CLKO            43B3> 38C8<
CMD_STATE *     49B8> 46A8<
CONN_SER1_GND   37C3
CONN_SER2_GND   37B3
CPU1_PD <3..0>  7C5> 8D8< 47C4<
CPU2_PD <3..0>  7C2> 8D8< 47B4<
CPU_DATA_OE *   11B6
CPU_FREQ_CFG <3..0> 8D4> 7A2<
CPU_RDL_OPEN    11B6
CRS_C2PWXS      11B6
CTS1 *          37C7> 35B8<
CTS2 *          37A7> 35B8<
DBB *           5D3<> 33A7< 33C7<
DBB_P1TR        5D6
DBG *           10C1> 5D2<
DCD1 *          37D7> 35B8<
DCD2 *          37B7> 35B8<
DENSITY_RD *    46B1> 36A7<
DPAL_PCICLK     21C1> 33B7<
DPE_60X *       7A2> 10C7<
DP_CPU1_ <7..0> 5A8<> 13C6<>
DP_CPU2_ <7..0> 5A2<> 18A2<>
DRAM_PD_RD *    46B1> 48A8<
DRTRY *         7C5
DRVMOD0_CPU1    7B8
DRVMOD0_CPU2    7B2
DRVMOD1_CPU1    7B8
DRVMOD1_CPU2    7B2
DSR1 *          37C7> 35B8<
DSR2 *          37A7> 35B8<
DTR1 *          35B1> 37C7<
DTR2 *          35B8> 37A7<
DUAL_CTRL_REF   11B6
D_CPU1_ <63..0> 5C8<> 13D6<>
D_CPU2_ <63..0> 5C2<> 18B2<>
EA <1..0>       38B2<> 43C7<
ECC_LE_SEL      11B6
ECP0 *          46C1> 36D7<
ECP1 *          46C1> 36D7<
ECP3 *          46C1> 36D7<
ECP5 *          46C1> 36D7<
ED <7..0>       38B2<> 43D7<>
ENCDCS0         32B1> 46C8<
ENCDCS1         32B1> 46C8<
ENCDCS2         32B1> 46C8<
ENCDCSEN *      32C1> 46C8<
EN_Y2_2VIA      28C8<
EQP_PRSNT_RD *  46B1> 47D8<
EREAD *         38A2> 43C7<
ERESET *        38A2> 43A7<
ETHNT_ACT *     30C2> 49B8<
ETHNT_PCICLK    21C1> 30D8<
ETHNT_SLEEP *   49B2> 29A8< 30A8<
EWRITE *        38A2> 43C7<
EXT_CTS1 *      37C5
EXT_CTS2 *      37A6
EXT_DCD1 *      37D5
EXT_DCD2 *      37B6
EXT_DSR1 *      37C5
EXT_DSR2 *      37A6
EXT_DTR1 *      37C5
EXT_DTR2 *      37A5
EXT_L_CD        42C7
EXT_RI *        49C4
EXT_RI1 *       37C5> 49C7<
EXT_RI2 *       37A4> 49D7<
EXT_RTS1 *      37C5
EXT_RTS2 *      37A5
EXT_R_CD        42B7
EXT_SCSI_GND    29A3
EXT_SCSI_GND24  29A1> 28D8<
EXT_SIN1        37C5
EXT_SIN2        37A6
EXT_SOUT1 *     37C5
EXT_SOUT2 *     37A5
EXT_TERM_PWR    29C3
FC_MEMW *       31B4
FC_PCIPERR *    31B6
FC_RTCAS        32B3
FC_SUSREQ *     31A6
FDD_DEN1        36A6
FDD_DEN2        36A6
FDD_DEN3        36A6
FDD_DEN4        36A6
FDD_DENSEL      36B6
FD_MTR_EN *     46B1> 35B1<
FLASH_WE_A18    27C5
FLOPPY <?..?>   35A1<> 36A2<>
FPAL_PCICLK     21C1>
FPGA_CCLK       23C5
FPGA_DIN        23C5
FRD *           32D1> 27A7<
FRZ_DATA        46A1> 20A8<
FWR *           32D1> 27A7<
GAME_CONN_GND   44C2
GBL *           6A3<> 10C1>
HALT/QREQ_CPU1A 7B5> 9B4<
HALT/QREQ_CPU1B 8B7> 9B4<
HALT/QREQ_CPU2A 7B2> 9B4<
HALT/QREQ_CPU2B 8A7> 9B4<
HALT_CPU1       9B1> 46C1<
HALT_CPU2       9B1> 46C1<
HCT14_PS_POWER_GOOD 52C3
HCT_RESET_SWITCH 53C7
HDD_LED *       46B1> 53C8<
HDD_PLUS5       53B2
HEAD_GND        39B2
HEAD_LEFT       39B2
HEAD_RIGHT      39B2
HFCS0 *         46B1>
HFCS1 *         46B1>
HPREQ *         31A6
HRESET_CPU1A *  9D2> 7D5<
HRESET_CPU1A_KS * 46D1> 9D6<
HRESET_CPU1B *  9D2> 8B7<
HRESET_CPU1B_KS * 46C1> 9C6<
HRESET_CPU2A *  9D2> 7D2<
HRESET_CPU2A_KS * 46C1> 9C6<
HRESET_CPU2B *  9C2> 8A7<
HRESET_CPU2B_KS * 46C1> 9C6<
HRESET_ESP *    9C5
IDEIRQP         46B8<
IDENT/PDACK *   36C2> 35C8<
IGN_PCI_AD31    12B6
INIT_CPU1A_MPIC * 23B2> 9C4<
INIT_CPU1B_MPIC * 23B2> 9B4<
INIT_CPU2A_MPIC * 23B2> 9B4<
INIT_CPU2B_MPIC * 23C2> 9B4<
INT_664 *       10D1> 22B7<
INT_CPU1A *     22A3> 7D5<
INT_CPU1B *     22A3> 8B7<
INT_CPU2A *     22A3> 7D2<
INT_CPU2B *     22A3> 8A7<
INT_ETHNT *     30A8<> 22B7<
INT_SCSI *      28A2> 22B7<
INT_SCSI_ACK *  29C7
INT_SCSI_ATN *  29C7
INT_SCSI_BSY *  29C7
INT_SCSI_CD *   29C7
INT_SCSI_GND24  29B8> 28D8<
INT_SCSI_IO *   29C7
INT_SCSI_MSG *  29C7
INT_SCSI_REQ *  29C7
INT_SCSI_RESET * 29C7
INT_SCSI_SEL *  29C7
INT_SIO         32B8> 22A7<
INT_SLOT1 *     25C2> 22A7<
INT_SLOT2 *     25C2> 22A7<
INT_SLOT3 *     25C2> 22A7<
INT_SLOT4 *     25C2> 22B7<
IO_STROBE *     46A1> 49B8<
IRQ1            46B1> 32B8<
IRQ1_KB         50A2> 46A8<
IRQ3            25B1> 35C1> 32B8<
IRQ4            25B1> 35D1> 32B8<
IRQ5            25B1> 35D1> 38B4> 32B8<
IRQ6            25B1> 35D1> 32B8<
IRQ7            25B1> 35D1> 38B4> 32B8<
IRQ8 *          50C2> 32B8<
IRQ9            25B1> 38B4> 32B8<
IRQ10           25B1> 32B8<
IRQ11           25B1> 38B4> 32B8<
IRQ12           24C7> 38B4> 50A2> 32B8< 46A8<
IRQ13           28B2> 32B8<
IRQ14           25B1> 38B4> 32B8<
IRQ15           25B1> 28A2> 32B8<
ISA_0WS *       24D7<> 31A2> 35C1>
ISA_AEN         24D7<> 32C6> 35C8< 38C7<
ISA_BALE        24C7<> 31B2>
ISA_CLK         31A2> 24A7< 46C8<
ISA_DACK0 *     32C7> 24C7< 36D7< 38A8<
ISA_DACK1 *     32C7> 24D7< 36D7< 38A8<
ISA_DACK2 *     32C7> 24D7< 35C8<
ISA_DACK3 *     32C7> 24D7< 36D7< 38A8<
ISA_DACK5 *     32C7> 24D7< 36D7<
ISA_DACK6 *     32C7> 24D7<
ISA_DACK7 *     32C7> 24D7<
ISA_DRQ0        24C7> 36D2> 38A2> 32C6<
ISA_DRQ1        24C7> 36D2> 38A2> 32C6<
ISA_DRQ2        24C7> 35C1> 32C6<
ISA_DRQ3        24C7> 36D2> 38A2> 32C6<
ISA_DRQ5        24C7> 36D2> 32C6<
ISA_DRQ6        24C7> 32C6<
ISA_DRQ7        24C7> 32C6<
ISA_IOCHCK *    25C1> 32A8<
ISA_IOCHRDY     24D7<> 31A2<> 35C1> 46A1> 38C7<
ISA_IOCS16 *    24C7> 31A2<> 35C8<
ISA_IOR *       24A7<> 31B2<> 34B6< 35C8< 38C7<
ISA_IOW *       24D7<> 31B2<> 34B6< 35C8< 38C7<
ISA_LA <23..17> 24A7<> 31C1<> 27A7< 27B7<
ISA_MASTER *    24C7> 31A2>
ISA_MEMCS16 *   24C7<> 31A2<>
ISA_MEMR *      24A7<> 31B2<>
ISA_MEMW *      24A7<> 31B2<>
ISA_REFRESH *   31A2> 24C7<
ISA_RESET       31A1> 25C1< 35C8<
ISA_RESET *     31A1> 38A8<
ISA_SBHE *      24B7<> 31A2>
ISA_SMEMR *     31B2> 24D7<
ISA_SMEMW *     31B2> 24D7<
ISA_TC          32C6> 24C7< 35C8<
JOYSTICK <7..0> 38C2<> 44B8>
KCE0 *          11C6
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IBM			
DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 55 OF 64

MOTHERBOARD

```
KCE1 *          11C6
KCE2 *          11C6
KCE3 *          11C6
KCE4 *          11C6
KCE5 *          11C6
KCE6 *          11C6
KCE7 *          11C6
KEYLOCK *       50A3
KMA <11..0>     11D4> 12C8<
KMWE0 *         11D4> 12C2<
KMWE1 *         11D4> 12C2<
KRE0 *          11C6
KRE1 *          11C6
KRE2 *          11C6
KRE3 *          11C6
KRE4 *          11C6
KRE5 *          11C6
KRE6 *          11C6
KRE7 *          11D6
KS_EXTHRESET *  46B8> 53D7<
KYBD/MSE_FUSE_GOOD 51D2> 50A2<
KYBD/MSE_GND    51C5
KYBD/MSE_VCC    51D4
KYBD_CLK        50A2<> 51C8<
KYBD_CLK *      51D2> 50B7<
KYBD_CS *       46B1> 50A7<
KYBD_DATA       50A2<> 51C8<
KYBD_DATA *     50A2<> 51D2>
KYBD_EA         50A4
KYBD_SS *       50A5
K_AACK *        10C4
K_ARTRY *       10C4
K_BGCPU1 *      10D1> 33C7<
K_BGCPU2 *      10D1> 33C7<
K_BRCPU1 *      33B3> 10C7<
K_BRCPU2 *      33B3> 10C7<
K_DBG *         10C4
K_GBL *         10C4
K_INTCPU *      10D4
K_MCP *         10D4
K_PCIFRAME *    12B2> 33B3>
K_PCIREQ *      10C4
K_SHD *         10C4
K_SRAMADS       10B4
K_SRAMALE *     10B4
K_SRAMCNTEN *   10B4
K_SRAM_WE *     10B4
K_TA *          10C4
K_TAGWE *       10B4
K_TBST *        10C6
K_TEA *         10D4
K_TS *          10C6
K_XATS *        10C6
L+R_MIC_OUT     41B1> 42A8<
L2_CLAIM *      7A2> 10B7<
L2_CONF *       6A3> 46C1>
L2_DIS *        46C1> 7A8< 19B2<
L2_FLUSH *      46C1> 7A2<
L2_INH *        46C1> 7A2<
L2_PD_CPU1 <1..0> 7C5> 7D5> 46A8<> 47D4<
L2_PD_CPU2 <1..0> 7C2> 7D2> 46A8<> 47B4<
L2_WT_ *        7B2> 46C1>
LED_HDD_LIGHT * 53C4
LED_RESET/POWER_GOOD * 53B4
LINE_OUT_RTN    39C3
L_AUX2          42B1> 38A8<
```

```
L_CD            42C5
L_FM            43C1> 38A8<
L_LINE          40D1> 38A8<
L_MIC           41C2> 38A8<
L_MODEM         42B4
L_MOD_OUT       39D2> 42A8<
L_OUT           38A2> 39D8>
MASK_BG1        33B7
MASK_BG2        33A7
MASK_BG3        33A7
MA_A <11..0>    12D2> 14B7< 15B7<
MA_B <11..0>    12D2> 16B7< 17B7<
MCE <7..0> *    11D4> 14C7< 15C7< 16C7< 17C7<
MCP_CPU1A *     10D1> 7C5<
MCP_CPU1B *     10D1> 8B7<
MCP_CPU2A *     10D1> 7C2<
MCP_CPU2B *     10D1> 8A7<
MC_663_BCLK     20B4
MC_664_BCLK     20C4
MC_4403_BCLK    20A4
MC_BCLK_SPARE   20B4
MC_PROC1_BCLK0  20C4
MC_PROC1_BCLK1  20C4
MC_PROC1_BCLK2  20D4
MC_PROC2_BCLK0  20B4
MC_PROC2_BCLK1  20C4
MC_PROC2_BCLK2  20C4
MC_SRAM_BCLK0   20A4
MC_SRAM_BCLK1   20B4
MC_SRAM_BCLK2   20B4
MC_SRAM_BCLK3   20B4
MC_TAG_BCLK     20A4
MD <63..0>      13D6<> 14A7<> 15A7<> 16A7<> 17A7<>
MDP <7..0>      13D6<> 14A7<> 15A7<> 16A7<> 17A7<>
MEM_ACK *       32D6>
MEM_BE <3..0>   11B6 11C6
MEM_DATA_OE *   11B6
MEM_RD_SMPL     11B6
MEM_REQ *       31A7> 32D6<
MEM_WRL_OPEN    11B6
MIDI_IN         44A7> 38A8<
MIDI_OUT        38A2> 44A7>
MIN             41B1> 38A8<
MOUSE_CLK       50A2<> 51B8<
MOUSE_CLK *     51B2> 50B7<
MOUSE_DATA      50A2<> 51B8<
MOUSE_DATA *    50A2<> 51B2>
MPC970_REFSEL   8D4> 20B8<
MPD <31..0>     14D2> 15D2> 16D2> 17D2> 48D8<
MPIC_PCICLK     21C1> 22D7<
MRE <7..0> *    11D4> 14C7< 14D7< 15D7< 16C7< 16D7<
                17D7<
MWE_A0 *        12D2> 14C7< 15C7<
MWE_A1 *        12D2> 14D7< 15D7<
MWE_B0 *        12D2> 16C7< 17C7<
MWE_B1 *        12D2> 16D7< 17D7<
MWS_P2MRXS      11B6
M_OUT           38A2> 40B8<
NVRAM_RD *      46B1> 50C7<
NVRAM_WR *      46B1> 50C7<
OCS_OVRIDE      9C5
OSC24MHZ_O      35D8
OSC970_O        20B7
OSC_14.3181MHZ  32D8
OSC_40MHZ       28C7
PAL_BCLK        20B1> 33A7< 33C7<
```

```
PARALLEL <16..0> 35A1<> 36B7<>
PAR_CONN_GND    36B3
PCIGNT_PAL *    31A7> 33B7<
PCI_AD <31..0>  12A7<> 22C7<> 25C7<> 27B7<> 28D2>
                30C8<> 31B7<> 31C7<> 22D7< 25D7<
                28B8< 30A8<
PCI_AD_OE *     11B6
PCI_AD_ROM <31..0> 27C6
PCI_C/BE <3..0> * 12B2<> 22D7<> 25A7<> 28B2<>
                30B8<> 31B7<>
PCI_DEVSEL *    12B2<> 22D7<> 25A7<> 28B2<> 31B7<>
                30A8<
PCI_ETHNT_GNT * 32D6> 12B8< 30A8<
PCI_ETHNT_REQ * 30A8> 32D6<
PCI_EXT_SEL     11B6
PCI_FRAME *     12B2<> 25A7<> 28B2<> 31B7<> 33B3<>
                22D7< 30B7<
PCI_GNT *       31A7> 33B3> 10C7<
PCI_IDSEL <15..1> 22D6 25D6 28B6 30B7 31B6
PCI_IRDY *      12B2<> 25A7<> 28B2<> 31B7<> 11A5<
                22D7< 30B7< 33B7<
PCI_LOCK *      25A7<> 31B7<> 12B6< 30B7<
PCI_OL_OPEN     11B6
PCI_OUT_SEL     11B6
PCI_PAR         12A7<> 22B7<> 25A7<> 28B2<> 31C7<>
                30B7<
PCI_PERR *      12A2<> 22B7<> 25A7<> 28B2<> 31B7<>
                30A8<
PCI_REQ_664 *   10C1> 31A7<
PCI_SCSI_GNT *  32D6> 12B8< 28B8<
PCI_SCSI_REQ *  28B2> 32D6<
PCI_SERR *      12A2<> 22B7<> 25A7<> 28B2> 31B7<>
                30A8<
PCI_SLOT1_GNT * 32D6> 12B8< 25D7<
PCI_SLOT1_PRESENT * 25D7> 47D8<
PCI_SLOT1_REQ * 25D7> 32D6<
PCI_SLOT2_GNT * 32D6> 12B8< 25D7<
PCI_SLOT2_PRESENT * 25D7> 47D8<
PCI_SLOT2_REQ * 25D7> 32D6<
PCI_STOP *      12B2<> 22D7<> 25A7<> 28B2<> 31B7<>
                30B7< 33B7<
PCI_TRDY *      12B2<> 22D7<> 25A7<> 28B2<> 31B7<>
                11A5< 30B7< 33B7<
PDRQ            35C1> 36C7<
PGD_PLUS5       53B2
PLANAR_ID_RD *  46B1> 47A8<
PLL_EN30        21B6
PLL_ENA30       21B6
PLL_FILTER      21B4
PLL_FOUT0       21B4
PLL_FOUT0A      21C5
PLL_FOUT1       21C5
PLL_FOUT1A      21C5
PLL_FOUT2       21C5
PLL_FOUT2A      21C5
PLL_FOUT3       21C5
PLL_FOUT3A      21C5
PLL_GND         30A5
PLL_PWR         30B5
PLL_X2_HFOUT    21B6
PLUS_12V        45C7
POWER_GOOD/RESET * 53C2> 10D7< 22A7< 25D7< 28C8<
                30D8<
PROC1_BCLK <2..0> 20C1> 7B5<
PROC1_PD_RD *   46B1> 47C4<
PROC2_BCLK <2..0> 20C1> 7B2<
```

```
PROC2_PD_RD *   46B1> 47A4<
PROC_RDY        49B8> 46B8<
PS_POWER_GOOD   52C4
PWR_LED_CNTL *  49B2> 53C8<
PWR_UP_CONF     49B4
P_9VA           45C4> 38C1< 39B8< 39D5< 39D8< 41A5<
                41A6< 41B2< 41B3< 41C5< 41C6< 41D6<
                42B3< 42C3<
P_D             49B2
P_SUPPLY_ON     49B4
P_U             49C2
RESET/POWER_GOOD * 53B5
RESET_SWITCH    53C8
RI1 *           37C7> 35B8<
RI2 *           37A7> 35C8<
ROM_CE *        46B1> 27A7<
ROM_LOAD        10C1> 11A5<
ROM_OE *        10C1> 27C7<
ROM_WE *        10C1> 27C7<
RTC_ALE *       32B1> 46B1> 50C7<
RTC_AS0 *       46B1> 50D7<
RTC_AS1 *       46B1> 50D7<
RTC_CS *        50C5
RTC_RD *        46B8> 50C7<
RTC_SQW_OUT     50C4>
RTC_WR *        46B8> 50C7<
RTS1 *          35B1> 37C7<
RTS2 *          35B1> 37A7<
RUN/HALT_ESP    9C8
RUN/QACK_CPU    46C1> 7B2< 49A2< 52C7<
RWD0            49B8<> 46A8<
RX+             30C4
RX-             30C4
R_AUX2          42C1> 38A8<
R_CD            42B5
R_EX            49C5
R_FM            43C1> 38A8<
R_LINE          40C1> 38A8<
R_MIC           41A2> 38A8<
R_MODEM         42C4
R_MOD_OUT       39D2> 42A8<
R_OUT           38A2> 39A8<
R_PS_POWER_GOOD 52C1> 49B2<
R_RESET_SWITCH  53C7
R_SMI           49B4
SA <19..0>      24B7<> 31D2<> 27A7< 35D8< 38B8<
SCS *           38B2> 43C7<
SCSI_40MHZ      28C6
SCSI_ACK *      29C8
SCSI_ACT *      28A2> 49B8<
SCSI_ATN *      29C8
SCSI_BSY *      29C8
SCSI_BUS_CNTL <8..0> 28C8<> 29D8<>
SCSI_CD *       29C8
SCSI_D <8..0>   28B8<> 29D7<>
SCSI_FUSE_GOOD  29A5> 47D8<
SCSI_IO *       29C8
SCSI_MAC_2VIA   28B3>
SCSI_MSG *      29C8
SCSI_PCICLK     21C1> 28B8<
SCSI_REQ *      29C8
SCSI_RESET *    29C8
SCSI_SEL *      29C8
SD <15..0>      24A7<> 25C1<> 31C1<> 36A2> 38B7<>
                35D1<
SELO            8C5
```

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```
SEMAPHORE_ST *  46C2>
SER_CLK         46A1> 47A4<
SER_CLK_EN      46A1> 47A4<
SHD *           6D2<> 10C1>
SIN1            37C7> 35B8<
SIN2            37A7> 35B8<
SINT            38B2> 43A3>
SIO_NMI         32B8> 12B6<
SIO_PCICLK      21C1> 31C7<
SLOT1_PCICLK    21C1> 25C7<
SLOT2_PCICLK    21C1> 25C7<
SMI             49B3
SMI_CPU *       49B2> 7D2<
SOUT1 *         35B1> 37C7<
SOUT2 *         35B1> 37A7<
SP_DATA1        40A4
SP_DATA2        40A3
SRAM_ADS/ADDR0 * 10B1> 19C6<
SRAM_ALE        10B1> 19C6<
SRAM_BCLK <3..0> 20B1> 19D6<
SRAM_CNT_EN/ADDR1 * 10B1> 19C6<
SRAM_OE *       10B1> 19C6< 33A7<
SRAM_PD <3..0>  19B6> 46A8<> 47A4<
SRAM_WE *       10B1> 19C6<
SRESET          32C3
SRESET_CPU1A *  9C1> 7D5<
SRESET_CPU1B *  9B1> 8B7<
SRESET_CPU2A *  9B1> 7D2<
SRESET_CPU2B *  9B1> 8A7<
SRESET_ESP *    9C4
SRESET_SIO *    32C1> 9C4<
SUPERIO_DRV2 *  35C6
SUPERIO_TC      35C6
SUSACK *        31A7> 10D7< 46A8<
SUSREQ_KS *     46A1> 31A7<
SUSSTAT *       32B3
SWITCH          49C4
TA *            10C1<> 5D2< 33A7<
TAG_BCLK        20A1> 19D3<
TAG_CLEAR *     7A2> 10B1> 19C6<
TAG_MATCH       19C6> 10B7<
TAG_VALID       10B1> 19C6<
TAG_WE *        10B1> 19C6<
TBEN_CPU        7B5
TBST *          6A2> 10C8<>
TCK_CPU         9A3> 7C2<
TDI_CPU1        9A5> 7C5<
TDI_CPU2        9A5> 7C2<
TDI_ESP         9A4
TDO_CPU1        7C5> 9A3>
TDO_CPU2        7C2> 9A3>
TDO_ESP         9A4
TEA *           10D1> 5D2<
TERM_PWR        29C5
TIMER2_OUT      32B8> 40A8<
TMS_CPU         9B3> 7C2<
TPI_GND         30B5
TPI_PWR         30B5
TRST_CPU1 *     9C2> 7C5<
TRST_CPU2 *     9C2> 7C2<
TS *            6C2<> 10C8<>
TSIZ <2..0>     6A2> 10C8<>
TT <4..0>       6A2<> 10C8<>
TTL_CLK         20C6
TX+             30D4
TX-             30D4
```

```
UCS5601_DISC    29B4
UCS5601_REG     29B3
UNFREEZE *      49B2> 46A8<
VBAT            49D5> 50D7<
VBATR           49D5> 49A8<
VBB             41A1> 39A8< 39D6< 41A5< 41B3< 41C5<
                42C4<
WT *            6A4
X1_ETHNT        30D5
X2FOUT          21B5
X2_ETHNT        30D5
XA <7..0>       31D1> 46C8< 48B8< 50A7<
XATS *          6C2<> 10C7<
XCTL0           38B2> 40B8<
XD <7..0>       27A2<> 31C1> 46B8<> 47D4<> 48A1<>
                50C2<> 49B8<
XDEN *          32C1> 31B3<
XDIR            32C1> 31B3<
XILINX_PROG_DONE 23C8> 47D8<
XIOR *          34B4> 46B8< 50A7<
XIOW *          34B4> 46B8< 50A7<
XTAL1I_24.576MHZ 38D6
XTAL1O_24.576MHZ 38D6
XTAL1_12MHZ     50B5
XTAL1_32.768KHZ 50C6
XTAL1_MPC970    20C7
XTAL2I_16.934MHZ 38C7
XTAL2O_16.934MHZ 38C7
XTAL2_12MHZ     50A5
XTAL2_32.768KHZ 50B4
XTAL2_MPC970    20C6
XTALI_33.8688MHZ 43C6
XTALO_33.8688MHZ 43B6
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*** Unit Cross-Reference ***
--- for the entire design --

C1	CAPACITOR	20C6
C2	ELCAP	49A7
C3	CAPACITOR	52C3
C4	CAPACITOR	8C3
C5	CAPACITOR	9C8
C6	CAPACITOR	8C3
C7	CAPACITOR	9C2
C8	CAPACITOR	38D8
C9	CAPACITOR	8C3
C10	CAPACITOR	38D8
C11	CAPACITOR	51A5
C12	CAPACITOR	8C1
C13	CAPACITOR	8A3
C14	CAPACITOR	8A1
C15	CAPACITOR	9D3
C16	CAPACITOR	8B3
C17	CAPACITOR	8C3
C18	CAPACITOR	8B3
C19	CAPACITOR	8C3
C20	CAPACITOR	8B3
C21	CAPACITOR	8B1
C22	CAPACITOR	8C1
C23	CAPACITOR	8C3
C24	CAPACITOR	8B1
C25	CAPACITOR	8C1
C26	CAPACITOR	8B1
C27	CAPACITOR	8C1
C28	CAPACITOR	8C1
C29	CAPACITOR	8C1
C30	ELCAP	8B3
C31	ELCAP	8A3
C32	CAPACITOR	20D7
C33	CAPACITOR	51C5
C34	CAPACITOR	20D7
C36	CAPACITOR	41C4
C37	CAPACITOR	52D2
C38	CAPACITOR	20D7
C39	CAPACITOR	23A5
C40	CAPACITOR	51D6
C41	CAPACITOR	51C6
C43	CAPACITOR	44B4
C44	CAPACITOR	50D3
C45	CAPACITOR	46A8
C46	CAPACITOR	23A5
C47	CAPACITOR	40D3
C48	CAPACITOR	41C5
C49	CAPACITOR	44B4
C50	CAPACITOR	51A7
C51	CAPACITOR	51A2
C52	CAPACITOR	54D3
C53	CAPACITOR	54D3
C54	CAPACITOR	51A5
C55	CAPACITOR	20D6
C56	CAPACITOR	26D2
C57	CAPACITOR	26A7
C58	CAPACITOR	30A5
C59	CAPACITOR	30D4
C60	CAPACITOR	42C2
C61	CAPACITOR	49A6
C62	CAPACITOR	20C8
C63	CAPACITOR	23A5
C64	CAPACITOR	26A7
C65	CAPACITOR	30D4
C66	CAPACITOR	40C4
C67	CAPACITOR	41A3
C68	CAPACITOR	42B5
C69	CAPACITOR	42A4
C70	CAPACITOR	50D2
C71	CAPACITOR	52D1
C72	CAPACITOR	26A7
C73	CAPACITOR	40C7
C74	CAPACITOR	41B2
C75	CAPACITOR	42B5
C76	CAPACITOR	44C5
C77	CAPACITOR	44C2
C78	CAPACITOR	51A5
C79	CAPACITOR	51C2
C80	CAPACITOR	54D7
C81	CAPACITOR	54D1
C82	CAPACITOR	26A6
C83	CAPACITOR	30D2
C84	CAPACITOR	40C7
C85	CAPACITOR	42A2
C86	CAPACITOR	42C5
C87	CAPACITOR	44C6
C88	CAPACITOR	50D2
C89	CAPACITOR	26A8
C90	CAPACITOR	26A6
C91	CAPACITOR	30C2
C92	CAPACITOR	30B5
C93	CAPACITOR	39B6
C94	CAPACITOR	40C3
C95	CAPACITOR	42B3
C96	CAPACITOR	44C6
C97	CAPACITOR	52D1
C98	CAPACITOR	50D2
C99	CAPACITOR	26A8
C100	CAPACITOR	26A8
C101	CAPACITOR	50A6
C102	CAPACITOR	33D8
C103	CAPACITOR	36B5
C104	CAPACITOR	36B4
C105	CAPACITOR	38C4
C106	CAPACITOR	39C3
C107	CAPACITOR	42B3
C108	CAPACITOR	44B4
C109	CAPACITOR	44C6
C110	CAPACITOR	53D6
C111	CAPACITOR	54D1
C112	CAPACITOR	26A7
C113	CAPACITOR	26A8
C114	CAPACITOR	30C4
C115	CAPACITOR	30C4
C116	CAPACITOR	36B3
C117	CAPACITOR	36B4
C118	CAPACITOR	36B4
C119	CAPACITOR	37B2
C120	CAPACITOR	37D1
C121	CAPACITOR	38C3
C122	CAPACITOR	39C3
C123	CAPACITOR	42C3
C124	CAPACITOR	44B4
C125	CAPACITOR	18C6
C126	CAPACITOR	50D1
C127	CAPACITOR	50A6
C128	CAPACITOR	51A4
C129	CAPACITOR	26A7
C131	CAPACITOR	36B4
C132	CAPACITOR	36B4
C133	CAPACITOR	37D1
C134	CAPACITOR	38D4
C135	CAPACITOR	40C3
C136	CAPACITOR	42B6
C137	CAPACITOR	42A4
C138	CAPACITOR	44A4
C139	CAPACITOR	54D3
C140	CAPACITOR	49D3
C141	ELCAP	52A6
C142	CAPACITOR	26A7
C143	CAPACITOR	36B4
C144	CAPACITOR	37B1
C145	ELCAP	43C2
C146	CAPACITOR	38D5
C147	CAPACITOR	41A8
C148	CAPACITOR	42A5
C149	CAPACITOR	44A5
C150	CAPACITOR	54D2
C151	CAPACITOR	49A3
C152	CAPACITOR	54D2
C153	CAPACITOR	33D8
C154	CAPACITOR	36B4
C155	CAPACITOR	37C2
C156	CAPACITOR	38D5
C157	CAPACITOR	41A8
C158	CAPACITOR	42A4
C159	CAPACITOR	18C7
C160	CAPACITOR	18D6
C161	CAPACITOR	36B4
C162	CAPACITOR	36B4
C163	CAPACITOR	38A4
C164	CAPACITOR	38D4
C165	CAPACITOR	39B3
C166	CAPACITOR	47A8
C167	CAPACITOR	49C2
C168	CAPACITOR	50D2
C169	CAPACITOR	52D2
C170	CAPACITOR	36B4
C171	CAPACITOR	36B4
C172	CAPACITOR	37A1
C173	ELCAP	43B5
C174	CAPACITOR	18C7
C175	CAPACITOR	38D4
C176	CAPACITOR	39A3
C177	CAPACITOR	47A8
C178	CAPACITOR	18D6
C179	ELCAP	49A3
C180	CAPACITOR	52D1
C181	CAPACITOR	36B4
C182	CAPACITOR	36B5
C183	CAPACITOR	37A1
C184	CAPACITOR	38A4
C185	CAPACITOR	38C6
C186	ELCAP	38A3
C187	CAPACITOR	39A1
C188	CAPACITOR	36B4
C189	CAPACITOR	36B5
C190	CAPACITOR	38A4
C191	CAPACITOR	38C6
C192	CAPACITOR	39C2
C193	CAPACITOR	18C7
C194	CAPACITOR	18D6
C195	CAPACITOR	50D5
C196	CAPACITOR	54D8
C197	CAPACITOR	54D8
C198	CAPACITOR	18C6
C199	CAPACITOR	36B4
C200	CAPACITOR	37B1
C201	CAPACITOR	38C6
C202	CAPACITOR	38A3
C203	CAPACITOR	39A2
C204	CAPACITOR	18D6
C205	CAPACITOR	54D7
C206	CAPACITOR	54D7
C207	CAPACITOR	18C6
C208	CAPACITOR	37A1
C209	CAPACITOR	38A3
C210	CAPACITOR	39C1
C211	CAPACITOR	18D6
C212	CAPACITOR	38C3
C213	CAPACITOR	49C8
C214	ELCAP	8B3
C215	ELCAP	8B3
C216	ELCAP	8B3
C217	ELCAP	8B3
C218	ELCAP	26B7
C219	ELCAP	26A7
C220	ELCAP	8A1
C221	ELCAP	8A3
C222	ELCAP	8B1
C223	ELCAP	8B1
C224	ELCAP	8A1
C225	ELCAP	8B1
C226	ELCAP	8B1
C227	ELCAP	8B1
C228	CAPACITOR	20D6
C229	CAPACITOR	30A4
C230	CAPACITOR	20D6
C231	CAPACITOR	30A4
C232	CAPACITOR	13B7
C233	CAPACITOR	21B6
C234	CAPACITOR	21B4
C235	CAPACITOR	30A4
C236	CAPACITOR	13B6
C237	CAPACITOR	20D7
C238	CAPACITOR	30A4
C239	CAPACITOR	13B6
C240	CAPACITOR	20D6
C241	CAPACITOR	20B3
C242	CAPACITOR	21B4
C243	CAPACITOR	30A4
C244	CAPACITOR	54A8
C245	CAPACITOR	52A8
C246	CAPACITOR	13B6
C247	CAPACITOR	14B2
C248	CAPACITOR	20B3
C249	CAPACITOR	30A5
C250	CAPACITOR	40A4
C251	CAPACITOR	54D2
C252	CAPACITOR	13B6
C253	CAPACITOR	14B2
C254	CAPACITOR	15B2
C255	CAPACITOR	20B3
C256	CAPACITOR	20A3
C257	CAPACITOR	30A5
C258	CAPACITOR	31D8
C260	CAPACITOR	18C6
C261	CAPACITOR	15B2
C262	CAPACITOR	16B2
C263	CAPACITOR	18D7
C264	CAPACITOR	20B3
C265	CAPACITOR	20A3

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C266 CAPACITOR 21C4
C267 CAPACITOR 25A1
C268 CAPACITOR 30A4
C269 CAPACITOR 31C2
C271 CAPACITOR 40A7
C272 CAPACITOR 18C6
C273 CAPACITOR 13B6
C274 CAPACITOR 14B2
C275 CAPACITOR 14C2
C276 CAPACITOR 16B2
C277 CAPACITOR 17B2
C278 CAPACITOR 20A3
C279 CAPACITOR 20C3
C280 CAPACITOR 30A4
C281 CAPACITOR 32C3
C282 CAPACITOR 36C2
C283 CAPACITOR 18D7
C284 CAPACITOR 49A4
C285 CAPACITOR 49C6
C286 CAPACITOR 13A6
C287 CAPACITOR 13B7
C288 CAPACITOR 14B2
C289 CAPACITOR 14C2
C290 CAPACITOR 15B2
C291 CAPACITOR 15C2
C292 CAPACITOR 17B2
C293 CAPACITOR 20C3
C294 CAPACITOR 20B3
C296 CAPACITOR 25A1
C297 CAPACITOR 41D4
C298 CAPACITOR 41A4
C299 CAPACITOR 41B1
C300 CAPACITOR 49C8
C301 CAPACITOR 13A6
C302 CAPACITOR 13B7
C303 CAPACITOR 14C2
C304 CAPACITOR 15B2
C305 CAPACITOR 15C2
C306 CAPACITOR 16B2
C307 CAPACITOR 16C2
C308 CAPACITOR 18D7
C309 CAPACITOR 20A3
C310 CAPACITOR 20C3
C311 CAPACITOR 21C5
C312 CAPACITOR 41B5
C313 CAPACITOR 13A7
C314 CAPACITOR 15C2
C315 CAPACITOR 16B2
C316 CAPACITOR 16C2
C317 CAPACITOR 17B2
C318 CAPACITOR 17C2
C319 CAPACITOR 20B3
C320 CAPACITOR 20C3
C321 CAPACITOR 21C4
C322 CAPACITOR 27A1
C323 CAPACITOR 32A4
C324 CAPACITOR 36B2
C325 CAPACITOR 39C3
C326 CAPACITOR 41C3
C327 ELCAP 38A4
C328 CAPACITOR 44A1
C329 CAPACITOR 13A7
C330 CAPACITOR 14C2
C331 CAPACITOR 16C2
C332 CAPACITOR 17B2
C333 CAPACITOR 17C2

C334 CAPACITOR 49A3
C335 CAPACITOR 20C3
C336 CAPACITOR 29C1
C337 CAPACITOR 32A4
C338 CAPACITOR 35A8
C339 CAPACITOR 37B6
C340 CAPACITOR 39D2
C341 CAPACITOR 39A8
C342 CAPACITOR 40B5
C343 CAPACITOR 40B7
C344 CAPACITOR 41D6
C345 CAPACITOR 41C3
C346 CAPACITOR 49C6
C347 CAPACITOR 13A7
C348 CAPACITOR 15C2
C349 CAPACITOR 17C2
C350 CAPACITOR 53C7
C351 CAPACITOR 20C7
C352 CAPACITOR 29C1
C353 CAPACITOR 29C1
C354 CAPACITOR 32A4
C355 CAPACITOR 37B1
C356 CAPACITOR 37B5
C357 CAPACITOR 39D7
C358 CAPACITOR 40C7
C359 CAPACITOR 41A8
C360 ELCAP 41A1
C361 CAPACITOR 52D5
C362 CAPACITOR 16C2
C363 CAPACITOR 27A1
C364 CAPACITOR 29D1
C365 CAPACITOR 29C1
C366 CAPACITOR 29A3
C367 CAPACITOR 31A3
C368 CAPACITOR 32A5
C369 CAPACITOR 37C1
C370 CAPACITOR 37A4
C371 CAPACITOR 37A3
C372 ELCAP 38D3
C373 CAPACITOR 40A6
C374 CAPACITOR 40B5
C375 CAPACITOR 41A4
C376 CAPACITOR 41B3
C377 CAPACITOR 45C7
C378 CAPACITOR 45C4
C379 CAPACITOR 13A6
C380 CAPACITOR 17C2
C381 CAPACITOR 29D1
C382 CAPACITOR 29C1
C383 CAPACITOR 29B5
C384 CAPACITOR 31D8
C385 CAPACITOR 32A5
C386 CAPACITOR 37A4
C387 CAPACITOR 37A4
C388 CAPACITOR 37B4
C389 CAPACITOR 38C8
C390 CAPACITOR 39B7
C391 CAPACITOR 39A4
C392 ELCAP 39A6
C394 CAPACITOR 13A6
C395 CAPACITOR 53D6
C396 CAPACITOR 29D1
C397 CAPACITOR 29C1
C398 CAPACITOR 29A8
C399 CAPACITOR 31D8
C400 CAPACITOR 32A5

C401 CAPACITOR 35A7
C402 CAPACITOR 37B4
C403 CAPACITOR 37A4
C404 CAPACITOR 38C8
C405 CAPACITOR 39A5
C406 CAPACITOR 41A6
C407 CAPACITOR 41A5
C408 CAPACITOR 46A8
C410 CAPACITOR 13A6
C411 CAPACITOR 27A1
C412 CAPACITOR 29D1
C413 CAPACITOR 29C1
C414 CAPACITOR 31D7
C415 CAPACITOR 32A5
C416 CAPACITOR 37A4
C417 CAPACITOR 37A4
C418 CAPACITOR 37B4
C419 CAPACITOR 39D7
C420 CAPACITOR 39D6
C421 CAPACITOR 39B5
C422 CAPACITOR 41A4
C423 CAPACITOR 29D1
C424 CAPACITOR 29C1
C425 CAPACITOR 29B3
C426 CAPACITOR 31D1
C427 CAPACITOR 32A5
C428 CAPACITOR 39B3
C429 CAPACITOR 46A8
C430 CAPACITOR 52D7
C431 CAPACITOR 29D1
C432 CAPACITOR 29D1
C433 CAPACITOR 29A5
C434 CAPACITOR 35A8
C435 CAPACITOR 37B6
C436 CAPACITOR 37B4
C437 CAPACITOR 39A5
C438 CAPACITOR 46A8
C439 CAPACITOR 29C1
C440 CAPACITOR 29D1
C441 CAPACITOR 29C2
C442 CAPACITOR 37A5
C443 CAPACITOR 39A3
C444 CAPACITOR 39A1
C445 CAPACITOR 29C1
C446 CAPACITOR 29A3
C447 CAPACITOR 29A2
C448 CAPACITOR 29A8
C449 CAPACITOR 37B3
C450 CAPACITOR 39C1
C451 CAPACITOR 39A4
C452 CAPACITOR 39C6
C453 ELCAP 26B7
C454 ELCAP 26B7
C455 ELCAP 26B6
C456 CAPACITOR 52D5
C457 ELCAP 26B6
C458 CAPACITOR 48C8
C459 ELCAP 23A6
C460 ELCAP 26B7
C461 CAPACITOR 52D6
C462 CAPACITOR 38C6
C463 ELCAP 26B7
C464 CAPACITOR 48C7
C465 CAPACITOR 53B2
C466 ELCAP 20D6
C467 CAPACITOR 43C2

C468 CAPACITOR 43C2
C469 ELCAP 30B5
C470 ELCAP 30A5
C471 CAPACITOR 52D6
C472 ELCAP 37A2
C473 ELCAP 38C3
C474 ELCAP 37A2
C475 ELCAP 13B6
C476 ELCAP 27A2
C477 ELCAP 13B5
C478 ELCAP 46A7
C479 ELCAP 13A5
C480 CAPACITOR 8A5
C481 CAPACITOR 48C8
C482 ELCAP 13A5
C483 ELCAP 14B2
C484 ELCAP 31D8
C485 ELCAP 13A6
C486 ELCAP 15B2
C487 ELCAP 31D8
C488 ELCAP 16B2
C489 ELCAP 17B2
C490 ELCAP 35A8
C491 ELCAP 14B2
C492 ELCAP 29B3
C493 ELCAP 15B2
C494 ELCAP 14B2
C495 ELCAP 16B2
C496 ELCAP 15B2
C497 ELCAP 17B2
C498 ELCAP 29A5
C499 ELCAP 14B2
C500 ELCAP 16B2
C501 ELCAP 29A7
C502 ELCAP 15B2
C503 ELCAP 17B2
C504 ELCAP 16B2
C505 ELCAP 17B2
C506 CAPACITOR 53B2
C507 CAPACITOR 53D5
C508 CAPACITOR 48C7
C509 CAPACITOR 53D5
C510 ELCAP 52D4
C511 ELCAP 52D4
C512 ELCAP 52D3
C513 ELCAP 52D3
C514 ELCAP 18C7
C515 ELCAP 52D3
C516 ELCAP 53D6
C517 ELCAP 18C7
C518 ELCAP 50D3
C519 ELCAP 18C8
C520 ELCAP 18D7
C521 ELCAP 18D7
C522 ELCAP 18D8
C523 ELCAP 48C8
C524 ELCAP 41A4
C525 ELCAP 39D6
C526 CAPACITOR 8B5
C527 CAPACITOR 8C5
C528 CAPACITOR 8C7
C529 CAPACITOR 8A5
C530 CAPACITOR 8A5
C531 CAPACITOR 8A5
C532 CAPACITOR 8B5
C533 CAPACITOR 8B5

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MOTHERBOARD

```
C534  CAPACITOR 8A5
C535  ELCAP     8B5
C536  ELCAP     8A5
C537  CAPACITOR 12D8
C538  CAPACITOR 36D8
C539  CAPACITOR 33D7
C540  CAPACITOR 35C8
C541  CAPACITOR 34B4
C542  CAPACITOR 47A8
C543  CAPACITOR 47A8
C544  CAPACITOR 47A8
C545  CAPACITOR 20D4
C546  CAPACITOR 20D4
C547  CAPACITOR 20D4
C548  CAPACITOR 20D3
C549  CAPACITOR 20D3
C550  CAPACITOR 21D8
C551  CAPACITOR 21D7
C552  CAPACITOR 21D7
C553  CAPACITOR 21D7
C554  CAPACITOR 21D7
C555  CAPACITOR 46A8
C556  CAPACITOR 46A7
C557  CAPACITOR 46A7
C558  ELCAP     28A8
C559  CAPACITOR 28A8
C560  CAPACITOR 28A8
C561  CAPACITOR 28A7
C562  CAPACITOR 28A7
C563  CAPACITOR 26D2
C564  CAPACITOR 28A7
C565  CAPACITOR 36C7
C566  CAPACITOR 28A7
C567  CAPACITOR 28C7
C568  CAPACITOR 28A7
C569  CAPACITOR 28A7
C570  CAPACITOR 28A7
C571  CAPACITOR 28A6
C572  ELCAP     45C6
C573  CAPACITOR 45C6
C574  CAPACITOR 52A8
C575  CAPACITOR 30D2
C576  CAPACITOR 30D2
C577  CAPACITOR 49D3
C578  CAPACITOR 29B1
C579  CAPACITOR 29B1
C580  CAPACITOR 49B1
C581  CAPACITOR 23A5
C582  CAPACITOR 23A4
C583  CAPACITOR 23A4
C584  CAPACITOR 23A4
C585  CAPACITOR 23A4
C586  CAPACITOR 23A3
C587  CAPACITOR 26D2
C592  CAPACITOR 54A8
C593  CAPACITOR 54A8
C594  CAPACITOR 54A8
C595  CAPACITOR 54A8
C596  CAPACITOR 54A8
C597  CAPACITOR 12D8
C598  CAPACITOR 36D8
C599  CAPACITOR 12D8
C600  CAPACITOR 12D8
C601  CAPACITOR 52C8
C602  CAPACITOR 36A4
C603  CAPACITOR 30B2
```

```
C604  CAPACITOR 23A3
C605  CAPACITOR 23A3
C606  CAPACITOR 54A7
C607  CAPACITOR 54A7
C608  CAPACITOR 54A7
C609  CAPACITOR 54A7
C610  CAPACITOR 54A7
C611  CAPACITOR 54A7
C612  CAPACITOR 34B4
C613  CAPACITOR 26D2
C614  CAPACITOR 52A3
C615  CAPACITOR 52A3
C616  CAPACITOR 52A3
C617  CAPACITOR 52A3
C618  CAPACITOR 52A3
C619  CAPACITOR 52A3
C620  ELCAP     52A4
C621  ELCAP     52A4
C622  ELCAP     52A4
C623  ELCAP     52A4
C624  ELCAP     52A4
C625  ELCAP     52A4
C626  ELCAP     27C2
C627  CAPACITOR 27C2
C628  CAPACITOR 27C2
C629  CAPACITOR 27C2
C704  CAPACITOR 43C2
C706  CAPACITOR 43B7
C707  CAPACITOR 43B6
C709  CAPACITOR 43B2 43C2
C712  CAPACITOR 43B5 43B6
C713  CAPACITOR 43B5
C714  CAPACITOR 43B5
C715  CAPACITOR 20D5
C716  CAPACITOR 20D4
C811  CAPACITOR 45A8
C812  CAPACITOR 45A8
C813  CAPACITOR 45A8
C814  CAPACITOR 11A5
CR1   1N5817    29A6
CR2   LED_A     30B3
CR3   MMBD914LT1 53D7
CR4   SER_DIODE 41A3
CR5   SER_DIODE 41D3
CR6   MMBD914LT1 45C6
CR7   SER_DIODE 39C4
CR8   SER_DIODE 41C2
CR9   SER_DIODE 41D5
CR10  SER_DIODE 41A5
CR11  SER_DIODE 40D2
CR12  SER_DIODE 40B2
CR13  SER_DIODE 41B4
CR14  SER_DIODE 39A4
CR15  SER_DIODE 39B4
CR16  SER_DIODE 39C4
CR17  ZENER     49C4
CR18  MMBD914LT1 49C3
CR19  SFPB54VL  49D7
CR20  SFPB54VL  49D6
CR21  SFPB54VL  49C6
CR22  MMBD914LT1 36C7
CR23  SFPB54VL  49D6
F1    POLYSWITCH 51D6
F2    POLYSWITCH 29A6
F3    POLYSWITCH 44D3
J0    CONN_SIMM72 14D5
```

```
J1    CONN_SIMM72 14D4
J2    CONN_SIMM72 15D5
J3    CONN_SIMM72 15D4
J4    CONN_SIMM72 16D5
J5    CONN_SIMM72 16D4
J6    CONN_SIMM72 17D5
J7    CONN_SIMM72 17D3
J8    CONNCPU256 5D6 6D7 7D6 8C4
J9    CONNCPU256 5D4 6D5 7D3 8C2
J10   CONN_MDIN6 51B3
J11   CONN_MDIN6 51D3
J12   CONN_L2   18D4 19D4
J13   CONNPOWER6 52C4
J14   CONN_PCI2X120 24D4 25C2 25D5 26D4
J15   CONN_BERG2X12 8B6
J16   CONN_BERG2X12 8A6
J17   CONN_BERG1X2 8C6
J18   CONN_ESP  9C6
J19   CONNSCSI50X 29D1
J20   CONN_BERG1X3 49D2
J21   RJ45S     30D1
J22   CDROM_CONN 42C8
J23   CONN_BERG1X2 49C2
J25   CONN_PARALLEL25 36C2
J26   CONN_SERIAL 37D2
J27   CONNSER9I 37B2
J28   CONN_BERG1X3 49B1
J29   POWER1X3  49C2
J30   CONN_BERG1X3 21B4
J31   CONN_BERG1X2 40B2
J32   CONNSCSI50I 29D5
J33   CONN_BERG2X8 44D3
J34   CONN_BERG1X3 52D6
J35   CONN_BERG1X3 32C1
J36   CONN_BERG1X3 52D7
J37   CONN_BERG1X3 52D4
J38   CONN_BERG1X2 53C8
J39   CONN_BERG1X2 40A3
J40   HSJ1453   40D8
J41   CONN_BERG1X2 53B2
J42   CONN_FLOPPY34 36B7
J43   CONN_BERG1X3 52D5
J44   CONN_BERG1X2 53C2
J45   CONN_BERG1X3 52D6
J46   HSJ1453   41B8
J47   HSJ1453   39C1
J48   HSJ1453   39B1
J49   2X4BERG   42A6
J50   CONN33POWER6 26D1
J51   CONN3-3POWER 52A4
J81   CONN_BERG2X3 9A4
L1    FERITE    29A4
L2    FERITE    51D5
L3    FERITE    30C2
L4    FERITE    30C2
L5    FERITE    51A5
L6    FERITE    30D2
L7    FERITE    30D2
L8    FERITE    44D4
L9    INDUCTOR  29C8
L10   INDUCTOR  29B7
L11   FERITE    44D2
L12   FERITE    42B7
L13   INDUCTOR  29D7
L14   FERITE    44A3
L15   INDUCTOR  29D7
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L16   FERITE    44A3
L17   INDUCTOR  29D7
L18   INDUCTOR  29C8
L19   INDUCTOR  29D7
L20   INDUCTOR  29C8
L21   INDUCTOR  29D7
L22   INDUCTOR  29C8
L23   INDUCTOR  29D7
L24   INDUCTOR  29C8
L25   INDUCTOR  29D7
L26   INDUCTOR  29C8
L27   FERITE    38D3
L28   INDUCTOR  29D7
L29   INDUCTOR  29C8
L30   INDUCTOR  29D7
L31   INDUCTOR  29C8
L32   INDUCTOR  29C8
L33   CHOKE3    40D5
L34   CHOKE3    41B6
L35   CHOKE3    39C3
L36   CHOKE3    39B3
L37   FERITE    21C4
L38   FERITE    37C2
L39   FERITE    29A4
L40   FERITE    29C3
L41   FERITE    29C3
L42   FERITE    37B2
L43   FERITE    36B4
L44   INDUCTOR  38D2
L45   FERITE    20D4
L46   FERITE    20D4
L47   FERITE    41B7
L48   FERITE    41B7
L49   FERITE    41B7
L50   FERITE    40D6
L51   FERITE    40D6
L52   FERITE    40C6
L53   FERITE    39C2
L54   FERITE    39C2
L55   FERITE    39C2
L56   FERITE    39B2
L57   FERITE    39B2
L58   FERITE    39B2
M1    87C750    49C4
M2    PAL16L8   9C2
M3    PAL16L8   9D3
M4    XC17000   23B6
M5    XC17000   23B5
M6    CONN_BATTERY 49D8
M8    PAL20L8   8D5
M9    PLCC32ROMSKT 27B4
M10   DIP4      20C7
M11   PALCE16V8 33D5
M12   PAL22V10  33C5
M13   KEYSTONE  46D4
M14   PLCC32ROMSKT 27D4
M16   ST93CS46  30B2
M18   PALCE16V8 33A5
Q1    IRFZ44    52B7
Q3    2N7002    49A6
Q4    2N7002    49A6
Q5    2N7002    49C2
Q6    IRFR014   52C7
R1    RESISTOR  5D3
R2    RESISTOR  23C3
R3    RESISTOR  23C3
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R4	RESISTOR	23B3
R5	RESISTOR	23B3
R6	RESISTOR	30C5
R7	RESISTOR	7D4
R8	RESISTOR	7B8
R9	RESISTOR	23B3
R10	RESISTOR	30C5
R11	RESISTOR	7C8
R12	RESISTOR	7D7
R13	RESISTOR	30C5
R14	RESISTOR	47B8
R15	RESISTOR	6D4
R16	RESISTOR	6B4
R17	RESISTOR	7C8
R18	RESISTOR	33A6
R19	RESISTOR	7D7
R20	RESISTOR	7A4
R21	RESISTOR	47C8
R22	RESISTOR	5C3
R23	RESISTOR	6D4
R24	RESISTOR	6D3
R25	RESISTOR	7C8
R26	RESISTOR	7A5
R27	RESISTOR	7B8
R28	RESISTOR	7A8
R29	RESISTOR	9B5
R30	RESISTOR	5A6
R31	RESISTOR	6D4
R32	RESISTOR	6D3
R33	RESISTOR	7A5
R34	RESISTOR	7B5
R35	RESISTOR	7B6
R36	RESISTOR	9B4
R37	RESISTOR	47B8
R38	RESISTOR	5A6
R39	RESISTOR	6D3
R40	RESISTOR	7B3
R41	RESISTOR	7A5
R42	RESISTOR	7B6
R43	RESISTOR	9B4
R44	RESISTOR	47B7
R45	RESISTOR	5A6
R46	RESISTOR	7B3
R47	RESISTOR	7A5
R48	RESISTOR	7C8
R49	RESISTOR	9D4
R50	RESISTOR	44A5
R51	RESISTOR	47B7
R52	RESISTOR	5B5
R53	RESISTOR	6D3
R54	RESISTOR	6B3
R55	RESISTOR	7A3
R56	RESISTOR	7B4
R57	RESISTOR	9C3
R58	RESISTOR	9C3
R59	RESISTOR	47B7
R60	RESISTOR	49A6
R61	RESISTOR	5B5
R62	RESISTOR	6D3
R63	RESISTOR	6B3
R64	RESISTOR	7B8
R65	RESISTOR	30A7
R66	RESISTOR	7A8
R67	RESISTOR	7B4
R68	RESISTOR	9D4
R69	RESISTOR	9C3

R70	RESISTOR	47B7
R71	RESISTOR	49A6
R72	RESISTOR	5D3
R73	RESISTOR	5B5
R74	RESISTOR	6A4
R75	RESISTOR	6B3
R76	RESISTOR	7A8
R77	RESISTOR	9D4
R78	RESISTOR	9C3
R79	RESISTOR	47B7
R80	RESISTOR	49A6
R81	RESISTOR	5D3
R82	RESISTOR	5B5
R83	RESISTOR	7A4
R84	RESISTOR	9D4
R85	RESISTOR	9C3
R86	RESISTOR	7D4
R87	RESISTOR	9D4
R88	RESISTOR	9C3
R89	RESISTOR	5A6
R90	RESISTOR	9D5
R91	RESISTOR	9C3
R92	RESISTOR	9D5
R93	RESISTOR	9C3
R94	RESISTOR	9D5
R95	RESISTOR	9C3
R96	RESISTOR	9C3
R97	RESISTOR	20C4
R98	RESISTOR	30C5
R99	RESISTOR	11C6
R100	RESISTOR	30C4
R101	RESISTOR	11C6
R102	RESISTOR	11C6
R103	RESISTOR	20C4
R104	RESISTOR	11C6
R105	RESISTOR	11C8
R106	RESISTOR	11C6
R107	RESISTOR	22B4
R108	RESISTOR	41C3
R109	RESISTOR	51B6
R110	RESISTOR	52C3
R111	RESISTOR	6A4
R112	RESISTOR	11C6
R113	RESISTOR	22D6
R114	RESISTOR	22B4
R115	RESISTOR	41C6
R116	RESISTOR	42C4
R117	RESISTOR	11C6
R118	RESISTOR	20C4
R119	RESISTOR	22B4
R120	RESISTOR	42C4
R121	RESISTOR	44B4
R122	RESISTOR	52C4
R123	RESISTOR	6C6
R124	RESISTOR	6A4
R125	RESISTOR	11D6
R126	RESISTOR	20C4
R127	RESISTOR	20C4
R128	RESISTOR	22B4
R129	RESISTOR	40C3
R130	RESISTOR	41A6
R131	RESISTOR	42B3
R132	RESISTOR	42B6
R133	RESISTOR	44B4
R134	RESISTOR	44C4
R135	RESISTOR	44D6

R136	RESISTOR	47B6
R137	RESISTOR	50B2
R138	RESISTOR	6C6
R139	RESISTOR	6C6
R140	RESISTOR	6A3
R141	RESISTOR	22B4
R142	RESISTOR	30B3
R143	RESISTOR	44D6
R144	RESISTOR	47C8
R145	RESISTOR	51D6
R146	RESISTOR	6C6
R147	RESISTOR	6C6
R148	RESISTOR	6A3
R149	RESISTOR	22B4
R150	RESISTOR	22B4
R151	RESISTOR	33B6
R152	RESISTOR	40C4
R153	RESISTOR	41A4
R154	RESISTOR	47C7
R155	RESISTOR	50A4
R156	RESISTOR	6C6
R157	RESISTOR	6C6
R158	RESISTOR	6D7
R159	RESISTOR	28B3
R160	RESISTOR	30B3
R161	RESISTOR	33B6
R162	RESISTOR	31B4
R163	RESISTOR	40D4
R164	RESISTOR	41D4
R165	RESISTOR	42A4
R166	RESISTOR	47C7
R167	RESISTOR	38B8
R168	RESISTOR	50B5
R169	RESISTOR	38B8
R170	RESISTOR	49D2
R171	RESISTOR	51B6
R172	RESISTOR	6C6
R173	RESISTOR	6D7
R174	RESISTOR	28A3
R175	RESISTOR	30C4
R176	RESISTOR	39C4
R177	RESISTOR	42B6
R178	RESISTOR	42A5
R179	RESISTOR	47C7
R180	RESISTOR	51D5
R181	RESISTOR	51D6
R182	RESISTOR	6C6
R183	RESISTOR	22B4
R184	RESISTOR	23C3
R185	RESISTOR	30A5
R186	RESISTOR	42B4
R187	RESISTOR	42C6
R188	RESISTOR	42A5
R189	RESISTOR	43B6
R190	RESISTOR	43C4
R191	RESISTOR	47C6
R192	RESISTOR	52A8
R193	RESISTOR	46A5
R194	RESISTOR	29C7
R195	RESISTOR	49A6
R196	RESISTOR	6C6
R197	RESISTOR	48D6
R198	RESISTOR	34C5
R199	RESISTOR	42A5
R200	RESISTOR	43B5
R201	RESISTOR	47C7

R202	RESISTOR	51B6
R203	RESISTOR	49C1
R204	RESISTOR	51B6
R205	RESISTOR	6C6
R206	RESISTOR	39B6
R207	RESISTOR	42D3
R208	RESISTOR	42A5
R209	RESISTOR	29A6
R210	RESISTOR	44B4
R211	RESISTOR	44D5
R212	RESISTOR	47C7
R213	RESISTOR	52A7
R214	RESISTOR	49C2
R215	RESISTOR	6C6
R216	RESISTOR	11C6
R217	RESISTOR	24D3
R218	RESISTOR	30A1
R219	RESISTOR	42B6
R220	RESISTOR	43A3
R221	RESISTOR	44D6
R222	RESISTOR	47D2
R223	RESISTOR	24D4
R224	RESISTOR	30C3
R225	RESISTOR	48D6
R226	RESISTOR	41A8
R227	RESISTOR	39A4
R228	RESISTOR	43B4
R229	RESISTOR	49B3
R230	RESISTOR	51C6
R231	RESISTOR	33A6
R232	RESISTOR	5D6
R233	RESISTOR	24D4
R234	RESISTOR	50C5
R235	RESISTOR	44A5
R236	RESISTOR	51D6
R237	RESISTOR	24A3
R238	RESISTOR	39C4
R239	RESISTOR	52A7
R240	RESISTOR	38D4
R241	RESISTOR	38C6
R242	RESISTOR	38B3
R243	RESISTOR	44A6
R244	RESISTOR	49D5
R245	RESISTOR	49B2
R246	RESISTOR	49C5
R247	RESISTOR	49C4
R248	RESISTOR	49B1
R249	RESISTOR	49D6
R250	RESISTOR	49B4
R251	RESISTOR	49C1
R252	RESISTOR	10C3
R253	RESISTOR	10C3
R254	RESISTOR	10C7
R255	RESISTOR	11C6
R256	RESISTOR	10C3
R257	RESISTOR	10D7
R258	RESISTOR	11C6
R259	RESISTOR	12D8
R260	RESISTOR	11C6
R261	RESISTOR	12D8
R262	RESISTOR	12D8
R263	RESISTOR	30C3
R264	RESISTOR	11C6
R265	RESISTOR	12D8
R266	RESISTOR	11C6
R267	RESISTOR	52C8

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B		MPRZP1SCU-03

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MOTHERBOARD

R268	RESISTOR	11A3
R269	RESISTOR	12B5
R270	RESISTOR	20B4
R271	RESISTOR	24B3
R272	RESISTOR	32B6
R273	RESISTOR	11C6
R274	RESISTOR	12D7
R275	RESISTOR	11A2
R276	RESISTOR	20B4
R277	RESISTOR	21C3
R278	RESISTOR	24B4
R279	RESISTOR	24C3
R280	RESISTOR	30D5
R281	RESISTOR	32B6
R282	RESISTOR	49B2
R283	RESISTOR	11C6
R284	RESISTOR	12D7
R285	RESISTOR	52C8
R286	RESISTOR	28B3
R287	RESISTOR	29B5
R288	RESISTOR	12B5
R289	RESISTOR	20A4
R290	RESISTOR	21B6
R291	RESISTOR	21C3
R292	RESISTOR	21C3
R293	RESISTOR	24B4
R294	RESISTOR	24C3
R295	RESISTOR	25B2
R296	RESISTOR	30D5
R297	RESISTOR	32B6
R298	RESISTOR	32C5
R299	RESISTOR	41B5
R300	RESISTOR	44D5
R301	RESISTOR	35C8
R302	RESISTOR	10C6
R303	RESISTOR	28C6
R304	RESISTOR	29B5
R305	RESISTOR	12D7
R306	RESISTOR	12D7
R307	RESISTOR	12D6
R308	RESISTOR	20A4
R309	RESISTOR	20B6
R310	RESISTOR	21B6
R311	RESISTOR	21C3
R312	RESISTOR	21C3
R313	RESISTOR	24C2
R314	RESISTOR	24C4
R315	RESISTOR	25C3
R316	RESISTOR	25D4
R317	RESISTOR	31A4
R318	RESISTOR	32B6
R319	RESISTOR	32C5
R320	RESISTOR	28C7
R321	RESISTOR	29D7
R322	RESISTOR	32B2
R323	RESISTOR	44C5
R324	RESISTOR	27B6
R325	RESISTOR	10D3
R327	RESISTOR	12D6
R328	RESISTOR	12D6
R329	RESISTOR	20A4
R330	RESISTOR	20B6
R331	RESISTOR	21B6
R332	RESISTOR	21C3
R333	RESISTOR	24C2
R334	RESISTOR	28B7

R335	RESISTOR	25A3
R336	RESISTOR	25B4
R337	RESISTOR	31A4
R338	RESISTOR	32D2
R339	RESISTOR	32C2
R340	RESISTOR	36A5
R341	RESISTOR	40A4
R342	RESISTOR	40A7
R343	RESISTOR	44C5
R344	RESISTOR	10D6
R345	RESISTOR	12D6
R346	RESISTOR	12D6
R347	RESISTOR	11A6
R348	RESISTOR	53C8
R349	RESISTOR	20A6
R350	RESISTOR	20C6
R351	RESISTOR	20B6
R352	RESISTOR	21C3
R353	RESISTOR	24C2
R354	RESISTOR	25D4
R355	RESISTOR	25A3
R356	RESISTOR	25B4
R357	RESISTOR	31B4
R358	RESISTOR	40C3
R359	RESISTOR	44C5
R360	RESISTOR	38B7
R361	RESISTOR	12D5
R362	RESISTOR	11C8
R363	RESISTOR	11A5
R364	RESISTOR	38B7
R365	RESISTOR	20B4
R366	RESISTOR	20A6
R367	RESISTOR	20C7
R368	RESISTOR	20C6
R369	RESISTOR	21C3
R370	RESISTOR	24C2
R371	RESISTOR	25D3
R372	RESISTOR	25B3
R373	RESISTOR	25B4
R374	RESISTOR	32C6
R375	RESISTOR	40B6
R376	RESISTOR	40A7
R377	RESISTOR	40A2
R378	RESISTOR	41C5
R379	RESISTOR	48D6
R380	RESISTOR	10D3
R381	RESISTOR	10D4
R382	RESISTOR	49B6
R383	RESISTOR	19B3
R384	RESISTOR	20C4
R385	RESISTOR	20B4
R386	RESISTOR	48D6
R387	RESISTOR	21C3
R388	RESISTOR	24C2
R389	RESISTOR	25D3
R390	RESISTOR	25B3
R391	RESISTOR	25B5
R392	RESISTOR	31A6
R393	RESISTOR	31A4
R394	RESISTOR	32C5
R395	RESISTOR	35B3
R396	RESISTOR	40A2
R397	RESISTOR	41A5
R398	RESISTOR	41B4
R399	RESISTOR	31B6
R400	RESISTOR	38B7

R401	RESISTOR	48D6
R402	RESISTOR	10D3
R403	RESISTOR	20B4
R404	RESISTOR	20B6
R405	RESISTOR	21B4
R406	RESISTOR	24C2
R407	RESISTOR	25D4
R408	RESISTOR	25B3
R409	RESISTOR	25B3
R410	RESISTOR	31B4
R411	RESISTOR	31D2
R412	RESISTOR	31A6
R413	RESISTOR	32D5
R414	RESISTOR	32C5
R415	RESISTOR	32D7
R416	RESISTOR	34B5
R417	RESISTOR	35B3
R418	RESISTOR	38D2
R419	RESISTOR	40B7
R420	RESISTOR	40A7
R421	RESISTOR	41A4
R422	RESISTOR	41B2
R423	RESISTOR	49B6
R424	RESISTOR	47D3
R425	RESISTOR	10D7
R426	RESISTOR	10D3
R427	RESISTOR	7B8
R428	RESISTOR	20B4
R429	RESISTOR	20A7
R430	RESISTOR	24C3
R431	RESISTOR	25D4
R432	RESISTOR	25B4
R433	RESISTOR	27A5
R434	RESISTOR	31B4
R435	RESISTOR	34C5
R436	RESISTOR	31A6
R437	RESISTOR	35B3
R438	RESISTOR	35C2
R439	RESISTOR	38D2
R440	RESISTOR	40B7
R441	RESISTOR	41C4
R442	RESISTOR	49B7
R443	RESISTOR	49D7
R444	RESISTOR	10B3
R445	RESISTOR	10D3
R446	RESISTOR	25D4
R447	RESISTOR	25B4
R448	RESISTOR	27A5
R449	RESISTOR	34B4
R450	RESISTOR	32B7
R451	RESISTOR	32A5
R452	RESISTOR	35B3
R453	RESISTOR	35D6
R454	RESISTOR	35C2
R455	RESISTOR	35A3
R456	RESISTOR	38A3
R457	RESISTOR	41D6
R458	RESISTOR	41B2
R459	RESISTOR	53D8
R460	RESISTOR	53B2
R461	RESISTOR	10D3
R462	RESISTOR	25D4
R463	RESISTOR	25B4
R464	RESISTOR	27A6
R465	RESISTOR	32B7
R466	RESISTOR	48D6

R467	RESISTOR	32C6
R468	RESISTOR	35B3
R469	RESISTOR	35D6
R470	RESISTOR	35A3
R471	RESISTOR	36C7
R472	RESISTOR	39C3
R473	RESISTOR	38B7
R474	RESISTOR	10D3
R475	RESISTOR	10D3
R476	RESISTOR	25B4
R477	RESISTOR	27B6
R478	RESISTOR	32B7
R479	RESISTOR	32C7
R480	RESISTOR	32C5
R481	RESISTOR	35B3
R482	RESISTOR	35D6
R483	RESISTOR	35B4
R484	RESISTOR	36C7
R485	RESISTOR	36C7
R486	RESISTOR	35A2
R487	RESISTOR	38C7
R488	RESISTOR	39D3
R489	RESISTOR	39A8
R490	RESISTOR	49B3
R491	RESISTOR	49B3
R492	RESISTOR	27B6
R493	RESISTOR	31A4
R494	RESISTOR	32B6
R495	RESISTOR	32B7
R496	RESISTOR	32C6
R497	RESISTOR	35B3
R498	RESISTOR	35D6
R499	RESISTOR	49D7
R500	RESISTOR	36C7
R501	RESISTOR	35A2
R502	RESISTOR	39D7
R503	RESISTOR	41A5
R504	RESISTOR	36C6
R505	RESISTOR	38B7
R506	RESISTOR	33A6
R507	RESISTOR	53B2
R508	RESISTOR	36C6
R509	RESISTOR	38B7
R510	RESISTOR	31B4
R511	RESISTOR	32B5
R512	RESISTOR	32C6
R513	RESISTOR	35B3
R514	RESISTOR	35B3
R515	RESISTOR	35D7
R516	RESISTOR	35B6
R517	RESISTOR	39B7
R518	RESISTOR	39B4
R519	RESISTOR	41A2
R520	RESISTOR	49D3
R521	RESISTOR	53B4
R522	RESISTOR	49D5
R523	RESISTOR	53B4
R524	RESISTOR	48D3
R525	RESISTOR	19C4
R526	RESISTOR	47A3
R527	RESISTOR	31A4
R528	RESISTOR	32B5
R529	RESISTOR	35B3
R530	RESISTOR	35B3
R531	RESISTOR	35C7
R532	RESISTOR	35B2

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MOTHERBOARD

R533	RESISTOR	39B3
R534	RESISTOR	41C4
R535	RESISTOR	41A2
R536	RESISTOR	41B5
R537	RESISTOR	45C5
R538	RESISTOR	47C3
R539	RESISTOR	48D3
R540	RESISTOR	47B3
R541	RESISTOR	32B5
R542	RESISTOR	35B3
R543	RESISTOR	35B6
R544	RESISTOR	35C7
R545	RESISTOR	35A2
R546	RESISTOR	35B2
R547	RESISTOR	39D6
R548	RESISTOR	39B5
R549	RESISTOR	45C5
R550	RESISTOR	32B6
R551	RESISTOR	35B2
R552	RESISTOR	35B2
R553	RESISTOR	39A3
R554	RESISTOR	41B5
R555	RESISTOR	41A3
R556	RESISTOR	35D7
R557	RESISTOR	35B2
R558	RESISTOR	36A6
R559	RESISTOR	39A5
R560	RESISTOR	41C3
R561	RESISTOR	7C5
R562	RESISTOR	36C6
R563	RESISTOR	35A2
R564	RESISTOR	36B5
R565	RESISTOR	36A5
R566	RESISTOR	35A2
R567	RESISTOR	35D8
R568	RESISTOR	36A5
R569	RESISTOR	39A6
R570	RESISTOR	36A5
R571	RESISTOR	39A6
R572	RESISTOR	39B6
R573	RESISTOR	7C5
R574	RESISTOR	7A8
R575	RESISTOR	7C5
R576	RESISTOR	7A7
R577	RESISTOR	7A8
R578	RESISTOR	7A8
R579	RESISTOR	7A8
R580	RESISTOR	7A8
R581	RESISTOR	7A8
R582	RESISTOR	8C6
R583	RESISTOR	8C6
R584	RESISTOR	8C6
R585	RESISTOR	48D6
R586	RESISTOR	38C6
R587	RESISTOR	20B6
R588	RESISTOR	6C6
R589	RESISTOR	6C6
R590	RESISTOR	6C6
R591	RESISTOR	6C6
R592	RESISTOR	6C6
R593	RESISTOR	6B6
R594	RESISTOR	6B6
R595	RESISTOR	6B6
R596	RESISTOR	6B6
R597	RESISTOR	6B6
R598	RESISTOR	6B6

R599	RESISTOR	6B6
R600	RESISTOR	6B6
R601	RESISTOR	6B6
R602	RESISTOR	6B6
R603	RESISTOR	6B6
R604	RESISTOR	6B6
R605	RESISTOR	6B6
R606	RESISTOR	6B6
R607	RESISTOR	6B6
R608	RESISTOR	5C5
R609	RESISTOR	5C5
R610	RESISTOR	5C5
R611	RESISTOR	5C5
R612	RESISTOR	5C5
R613	RESISTOR	5C5
R614	RESISTOR	5C5
R615	RESISTOR	5C5
R616	RESISTOR	5C5
R617	RESISTOR	5C5
R618	RESISTOR	5C5
R619	RESISTOR	5C5
R620	RESISTOR	5C5
R621	RESISTOR	5C5
R622	RESISTOR	5C5
R623	RESISTOR	5C5
R624	RESISTOR	5C5
R625	RESISTOR	5C5
R626	RESISTOR	5C5
R627	RESISTOR	5C5
R628	RESISTOR	5C5
R629	RESISTOR	5C5
R630	RESISTOR	5C5
R631	RESISTOR	5B5
R632	RESISTOR	5B5
R633	RESISTOR	5B5
R634	RESISTOR	5B5
R635	RESISTOR	5B5
R636	RESISTOR	5B5
R637	RESISTOR	5B5
R638	RESISTOR	5B5
R639	RESISTOR	5B5
R640	RESISTOR	5B5
R641	RESISTOR	5B5
R642	RESISTOR	5B5
R643	RESISTOR	5B5
R644	RESISTOR	5B5
R645	RESISTOR	5B5
R646	RESISTOR	5B5
R647	RESISTOR	5A5
R648	RESISTOR	5A5
R649	RESISTOR	5A5
R650	RESISTOR	5A5
R651	RESISTOR	5A5
R652	RESISTOR	5A5
R653	RESISTOR	5A5
R654	RESISTOR	5A5
R655	RESISTOR	5A5
R656	RESISTOR	5A5
R657	RESISTOR	5A5
R658	RESISTOR	5A5
R659	RESISTOR	5A5
R660	RESISTOR	5A5
R661	RESISTOR	5A5
R662	RESISTOR	5A5
R663	RESISTOR	5A5
R664	RESISTOR	5A5

R665	RESISTOR	5A5
R666	RESISTOR	5A5
R667	RESISTOR	5A5
R668	RESISTOR	5A5
R669	RESISTOR	5A5
R670	RESISTOR	5A5
R671	RESISTOR	5A5
R672	RESISTOR	25D6
R673	RESISTOR	25D6
R674	RESISTOR	25D4
R675	RESISTOR	25D3
R676	RESISTOR	31B7
R677	RESISTOR	36C6
R678	RESISTOR	33B6
R679	RESISTOR	33B6
R680	RESISTOR	33B6
R681	RESISTOR	33B6
R682	RESISTOR	30A7
R683	RESISTOR	31A6
R684	RESISTOR	10C7
R685	RESISTOR	32D5
R686	RESISTOR	34C5
R687	RESISTOR	10C6
R688	RESISTOR	10C6
R689	RESISTOR	10C6
R690	RESISTOR	10C6
R691	RESISTOR	10C6
R692	RESISTOR	10C6
R693	RESISTOR	10C6
R694	RESISTOR	10C6
R695	RESISTOR	36C6
R696	RESISTOR	36C6
R697	RESISTOR	31A6
R698	RESISTOR	23D5
R699	RESISTOR	32B7
R700	RESISTOR	36C6
R701	RESISTOR	7B8
R702	RESISTOR	10C7
R703	RESISTOR	7A6
R704	RESISTOR	20B6
R705	RESISTOR	20A6
R706	RESISTOR	7A5
R707	RESISTOR	7A4
R708	RESISTOR	19B3
R709	RESISTOR	19B3
R710	RESISTOR	7A4
R711	RESISTOR	10D4
R712	RESISTOR	10B3
R713	RESISTOR	10C3
R714	RESISTOR	10C3
R715	RESISTOR	10B3
R716	RESISTOR	10B3
R717	RESISTOR	10B3
R718	RESISTOR	21B6
R719	RESISTOR	36C6
R720	RESISTOR	36C6
R721	RESISTOR	36C6
R722	RESISTOR	36C5
R723	RESISTOR	36C5
R724	RESISTOR	36C5
R725	RESISTOR	49D4
R726	RESISTOR	49B4
R727	RESISTOR	49B4
R728	RESISTOR	49A4
R729	RESISTOR	49B3
R730	RESISTOR	49B3

R731	RESISTOR	49B3
R732	RESISTOR	49A3
R733	RESISTOR	28A2
R736	RESISTOR	31A7
R737	RESISTOR	20B7
R738	RESISTOR	10C3
R739	RESISTOR	11A6
R740	RESISTOR	34B4
R741	RESISTOR	12D5
R742	RESISTOR	12D5
R743	RESISTOR	12D5
R744	RESISTOR	12D5
R745	RESISTOR	12D5
R746	RESISTOR	12D5
R747	RESISTOR	12D4
R748	RESISTOR	12D4
R749	RESISTOR	12D4
R750	RESISTOR	12D4
R751	RESISTOR	12D3
R752	RESISTOR	12D3
R753	RESISTOR	12D3
R754	RESISTOR	12D3
R755	RESISTOR	12D3
R756	RESISTOR	12D3
R757	RESISTOR	12D3
R758	RESISTOR	12D2
R759	RESISTOR	12C2
R761	RESISTOR	33C6
R762	RESISTOR	33C6
R763	RESISTOR	33C6
R764	RESISTOR	49B7
R765	RESISTOR	49B7
R766	RESISTOR	11A5
R767	RESISTOR	31A4
R768	RESISTOR	47C3
R769	RESISTOR	47B3
R770	RESISTOR	33C6
R771	RESISTOR	33C6
R772	RESISTOR	33C4
R773	RESISTOR	33C4
R774	RESISTOR	33C4
R775	RESISTOR	33B5
R776	RESISTOR	33B5
R777	RESISTOR	48D6
R778	RESISTOR	48D5
R779	RESISTOR	48D5
R780	RESISTOR	48D5
R781	RESISTOR	48D5
R782	RESISTOR	48D5
R783	RESISTOR	48D5
R784	RESISTOR	48D5
R785	RESISTOR	48D5
R786	RESISTOR	48D5
R787	RESISTOR	48D5
R788	RESISTOR	48D4
R789	RESISTOR	48D4
R790	RESISTOR	48D4
R791	RESISTOR	48D4
R792	RESISTOR	48D4
R793	RESISTOR	48D4
R794	RESISTOR	48D4
R795	RESISTOR	48D4
R796	RESISTOR	48D4
R797	RESISTOR	48D4
R798	RESISTOR	48D3
R799	RESISTOR	48D3

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POWERPC 604 SMP REFERENCE DESIGN			SHEET 63 OF 64

MOTHERBOARD

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R800  RESISTOR  10C3
R801  RESISTOR  52C7
R802  RESISTOR  52C4
R803  RESISTOR  52C6
R804  RESISTOR  52C6
R805  RESISTOR  52C5
R806  RESISTOR  46B4
R807  RESISTOR  32A5
R808  RESISTOR  27B6
R809  RESISTOR  27B6
R810  RESISTOR  27B6
R811  RESISTOR  27C6
R812  RESISTOR  27B6
R813  RESISTOR  27B6
R814  RESISTOR  27B5
R815  RESISTOR  27B5
R816  RESISTOR  27D5
R817  RESISTOR  27B5
R818  RESISTOR  12B5
R819  RESISTOR  27B5
R820  RESISTOR  27B5
R821  RESISTOR  27B5
R822  RESISTOR  27B5
R823  RESISTOR  27C4
R824  RESISTOR  27B4
R825  RESISTOR  27B4
R826  RESISTOR  32B3
R827  RESISTOR  27B4
R828  RESISTOR  32D3
R829  RESISTOR  32D3
R830  RESISTOR  27B4
R831  RESISTOR  32B2
R832  RESISTOR  27B3
R833  RESISTOR  27B3
R834  RESISTOR  27B3
R835  RESISTOR  27B3
R836  RESISTOR  27B3
R837  RESISTOR  27B3
R838  RESISTOR  27B3
R839  RESISTOR  27B2
R840  RESISTOR  19B3
R841  RESISTOR  31A4
R842  RESISTOR  25D5
R843  RESISTOR  7A8
R845  RESISTOR  46B6
R846  RESISTOR  19C4
R847  RESISTOR  25D5
R848  RESISTOR  19C4
R849  RESISTOR  19C3
R850  RESISTOR  19C3
R851  RESISTOR  27B4
R852  RESISTOR  27B4
R853  RESISTOR  32C2
R854  RESISTOR  32C2
R855  RESISTOR  31A7
R856  RESISTOR  34C5
R857  RESISTOR  34C5
R858  RESISTOR  19C5
R859  RESISTOR  19B5
R860  RESISTOR  19B5
R861  RESISTOR  34C6
R862  RESISTOR  33B5
R863  RESISTOR  33B5
R864  RESISTOR  33A5
R884  RESISTOR  12B3
R885  RESISTOR  12C3
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```
R886  RESISTOR  20C6
R887  RESISTOR  43B6
R888  RESISTOR  49C5
R889  RESISTOR  50C6
R890  RESISTOR  50A5
R891  RESISTOR  31A7
R892  RESISTOR  33B5
R893  RESISTOR  33D5
R894  RESISTOR  33C5
R895  RESISTOR  33B5
R896  RESISTOR  49A3
R897  RESISTOR  32C3
R898  RESISTOR  11B6
R899  RESISTOR  11A6
R900  RESISTOR  30A1
R901  RESISTOR  33A6
R902  RESISTOR  33A5
R903  RESISTOR  7C8
R904  RESISTOR  7C8
R905  RESISTOR  7C5
R906  RESISTOR  7C5
R907  RESISTOR  5D7
R908  RESISTOR  20B6
R909  RESISTOR  23C3
R910  RESISTOR  23C3
R911  RESISTOR  33A5
R912  RESISTOR  46B6
R913  RESISTOR  52C5
R914  RESISTOR  33C6
S3    DO_NOT_POP_PLCC20 54B6
S4    DO_NOT_POP_16 54C4
S5    DO_NOT_POP_16 54C4
S6    DO_NOT_POP_PLCC28 54C3
S7    DO_NOT_POP_PLCC28 54B3
S8    DO_NOT_POP_PLCC28 54C2
S9    DO_NOT_POP_PLCC28 54B2
T1    E_XFORM   30D3
U1    F06       51B7 51C7 51D7 54A3
U2    AM79C970  30D5
U3    IBM82664  10D5 11D7 12C3 13A7
U4    IBM82663V2 11C3 12B5 13C7 13D2 13D4
U5    ALS21     12B6 53C6
U6    F04       28B3 32C2 35C7 36B6 53C5 54B3
U7    F244      31D2 31D3
U8    CS4232    38C4
U10   MPIC      22D5 23D3
U11   F07       44A6 44A6 44B1
U12   NCR53C810 28D4
U13   ABT244    12D6
U14   UC5601    29B4
U15   F04       38A6 38B7 49B3 54A3
U16   F08       38A6 49B6 54A4
U18   TL084     39A7 39D6 42B3 42C3
U19   DS1385    50D4
U20   8042H     50B4
U21   HCT14     31A2 31A3 52C2 52C3 53C6 53C7
U22   F157      8D6
U23   F244      47A2 47D6
U24   ABT244    12D4 12D5
U25   F125      32C2 53B4 53C4
U26   MPC970    20C5
U27   F244      36A4 54A4
U28   F244      47C2 47D2
U29   F244      47B6 47C6
U30   S4403     21C5
U32   82378_82376 31D4 32A7 32D3
```

```
U33   PC87332   35D5
U34   F125      35C2 46A3 52C8
U35   LM317     45D6
U36   LT1431REG 52A7
U37   LM78M05   38C2
U38   TL084     41A4 41B3 41B5 41C4
U39   TDA7052   40A5
U40   TDA1308T  39A5 39B5
U42   ABT244    12D3 12D4
U43   F125      36D4 36D4 36D5
U44   F125      36D5 36D6
U45   F244      34B5 34C5
U46   SN75C185  37B6
U47   SN75C185  37D6
U50   F139      48B7 54B2
U51   YMF289S   43D5
U52   F244      48A6 48B6
U53   F244      48C6
U54   F244      48C5
U55   F245      31C3
U56   F244      47B2 47C2
U57   YAC516E   43C3
U58   F244      48A5 48B5
U59   ABT244    12D7 12D8
U60   F126      47A3 47B3 47C3 54A2
U61   F00       29B5 53C5 54A1 54B1
X1    PART      49A4
X2    PART      9B2
X3    PART      9C3
X6    PART      49D7
X7    EMC_PAD   45B8
X8    PART      8D5
X9    PART      27D3
X10   EMC_PAD   45B8
X13   PART      46D4
X16   PART      30B2
X17   PART      52B7
X19   PART      20C8
Y1    OSCILLATOR 28C7
Y2    XTAL      38D7
Y3    XTAL      50D6
Y4    XTAL      49C6
Y5    XTAL      50B6
Y6    OSCILLATOR 32D8
Y7    OSCILLATOR 46A6
Y8    CRYSTAL   20D8
Y9    OSCILLATOR 35D8
Y10   XTAL      30D4
Y11   CRYSTAL   43C7
Y12   XTAL      38C7
Y13   XTAL      20D7
Y15   XTAL      43C7
```

IBM

DATE: 15 DEC 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP1SCU-03
POWERPC 604 SMP REFERENCE DESIGN			SHEET 64 OF 64

MOTHERBOARD

PowerPC 604
CHEETAH0 CPU
CARD SCHEMATICS

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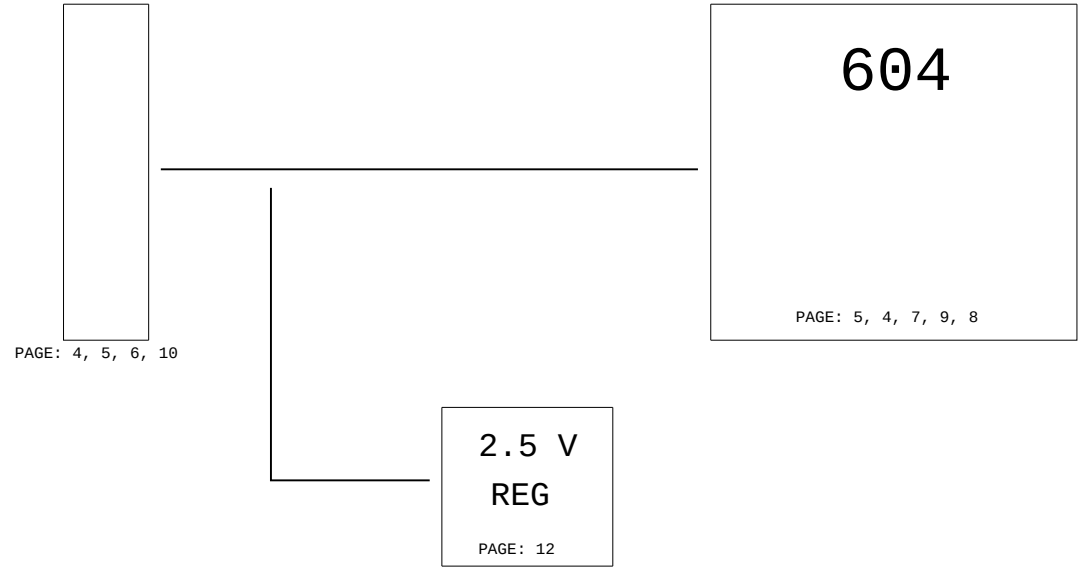
IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD			SHEET 1 OF 15

CPU

CARD EDGE CONNECTOR



PAGE NUMBERS IN ORDER OF SECTION NUMBERS

IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 2 OF 15		

CPU

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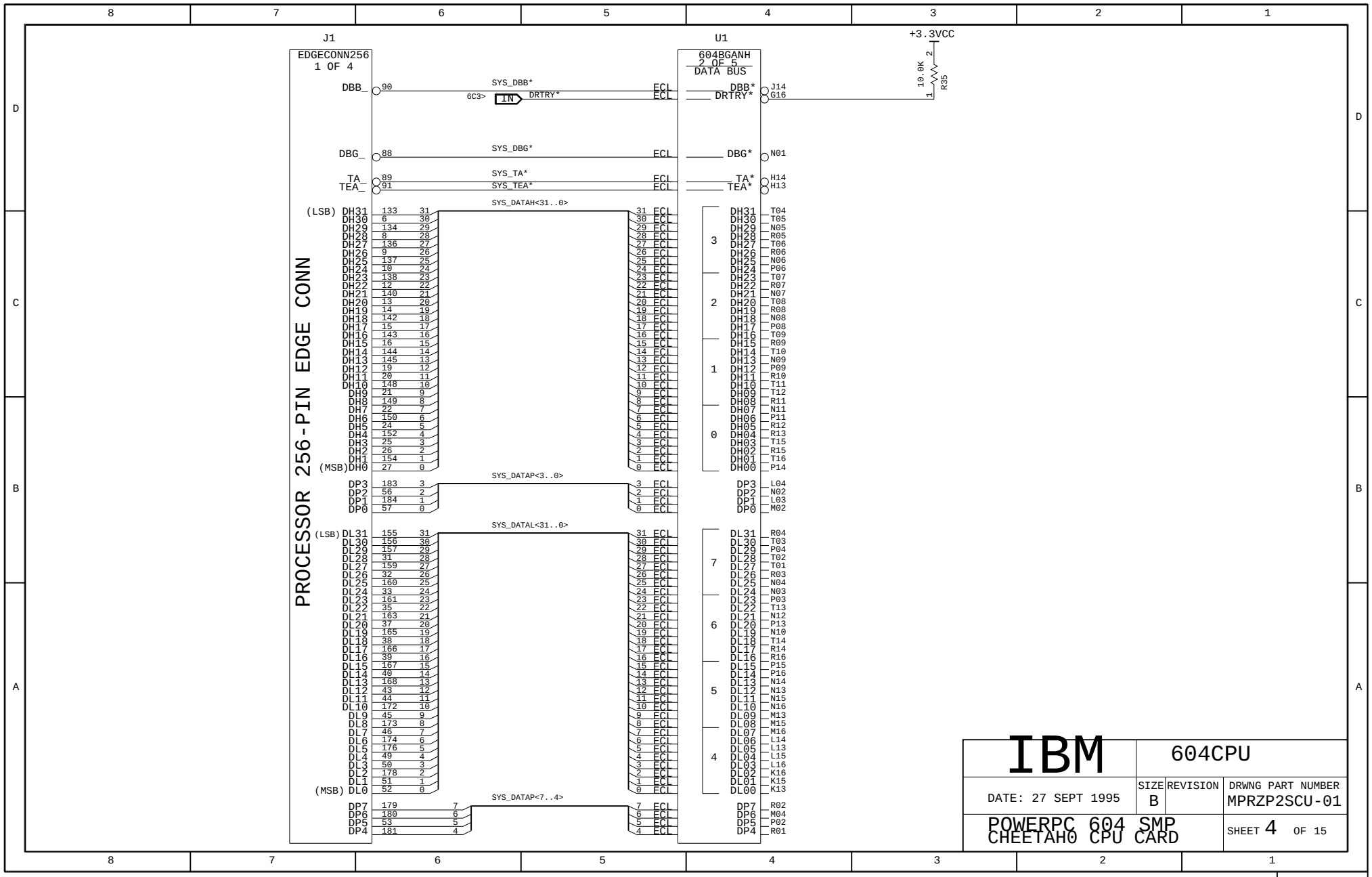
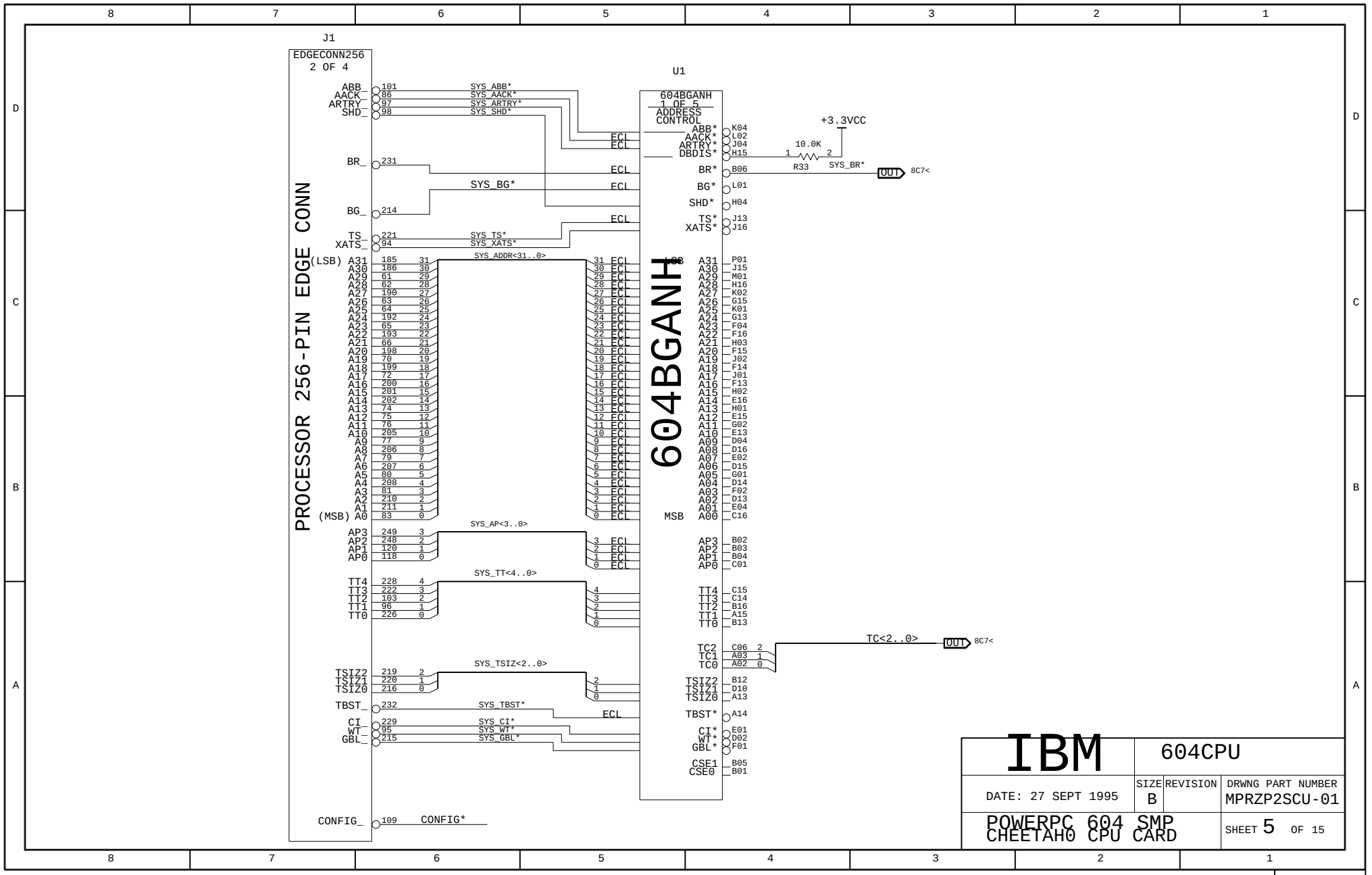
IBM			604CPU	
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01	
POWERPC 604 SMP CHEETAH0 CPU CARD			SHEET 3 OF 15	

CPU



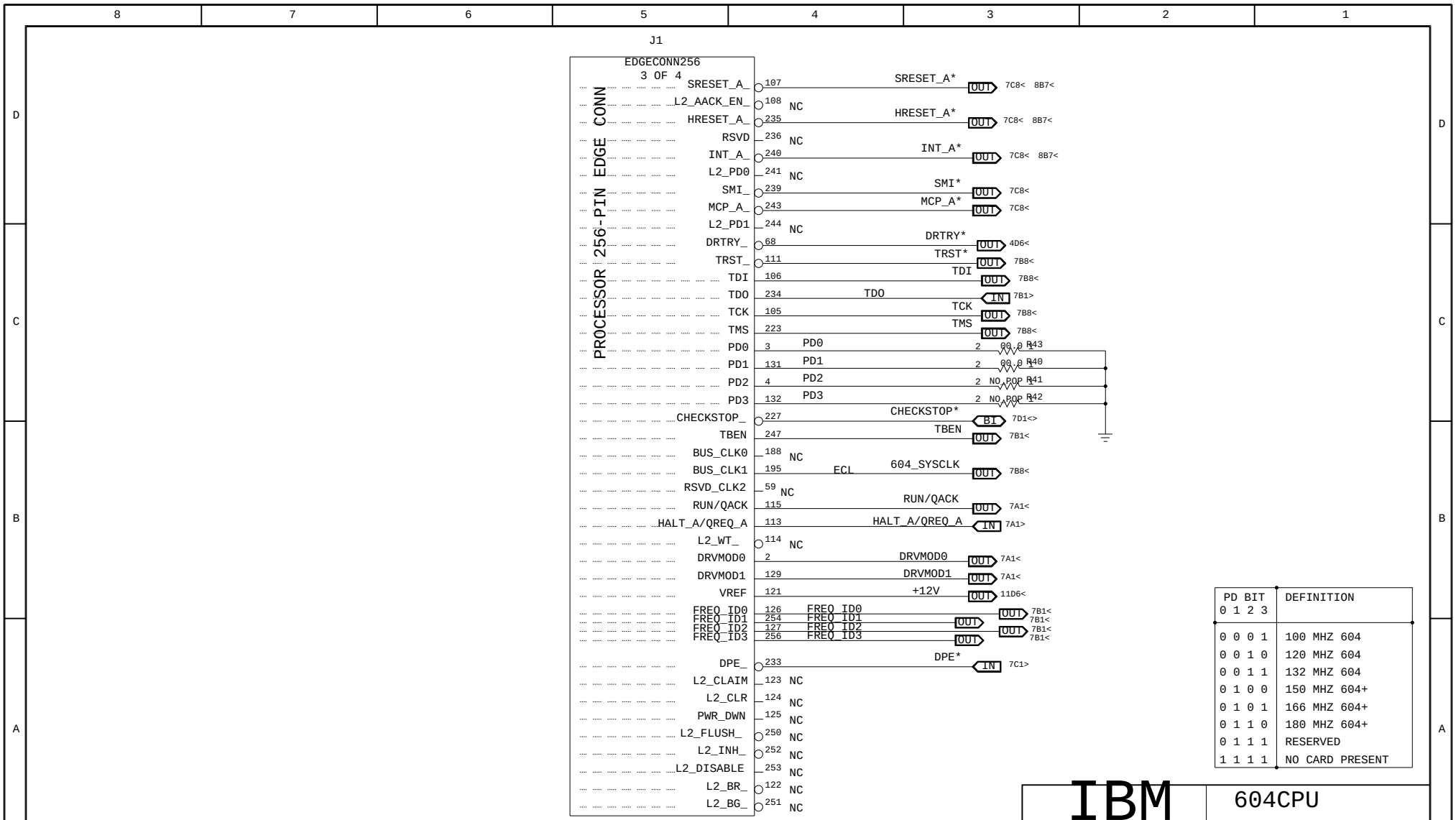
IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 4 OF 15		

CPU



IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 5 OF 15		

CPU



PD BIT 0 1 2 3	DEFINITION
0 0 0 1	100 MHZ 604
0 0 1 0	120 MHZ 604
0 0 1 1	132 MHZ 604
0 1 0 0	150 MHZ 604+
0 1 0 1	166 MHZ 604+
0 1 1 0	180 MHZ 604+
0 1 1 1	RESERVED
1 1 1 1	NO CARD PRESENT

IBM

604CPU

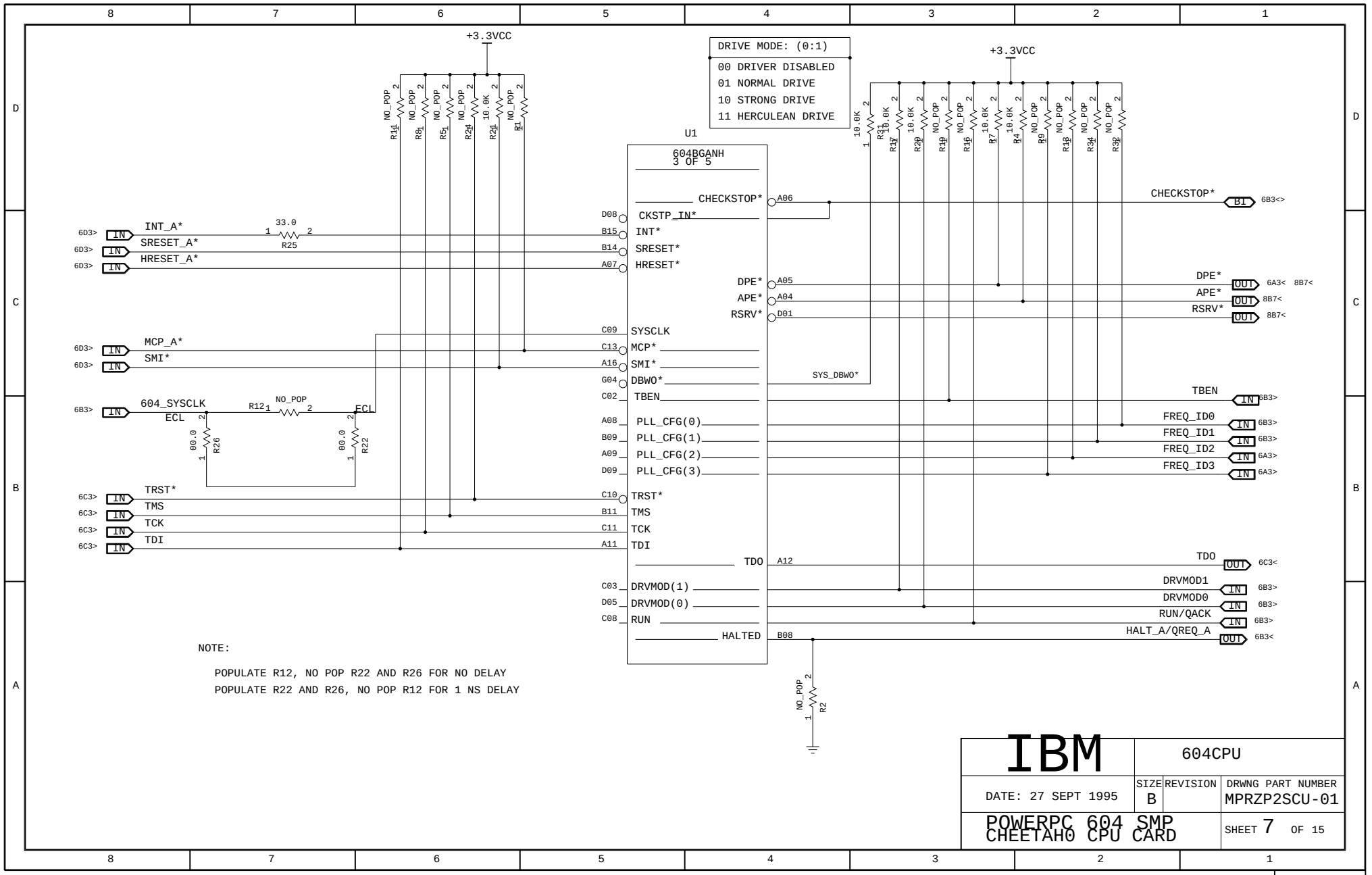
DATE: 27 SEPT 1995

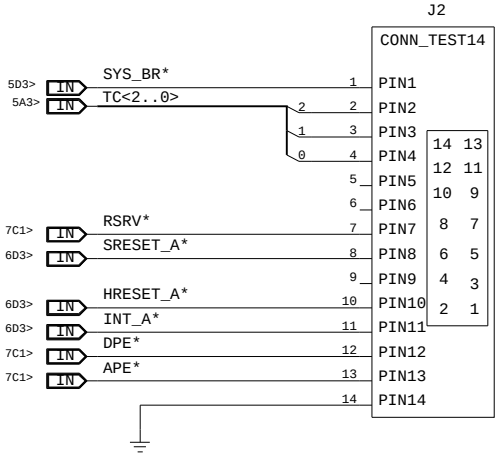
SIZE B | REVISION | DRWNG PART NUMBER MPRZP2SCU-01

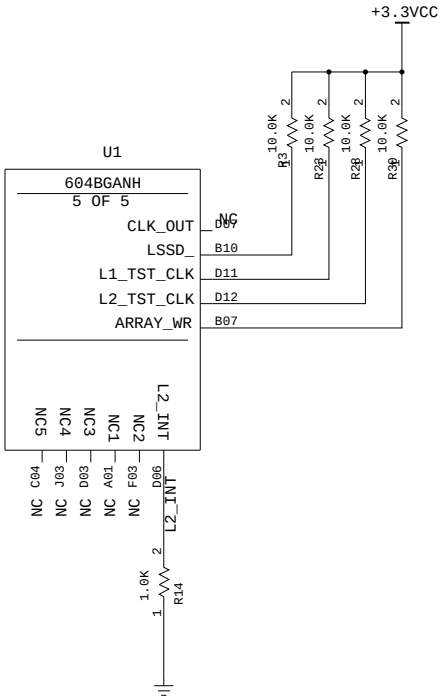
POWERPC 604 SMP CHEETAH0 CPU CARD

SHEET 6 OF 15

CPU

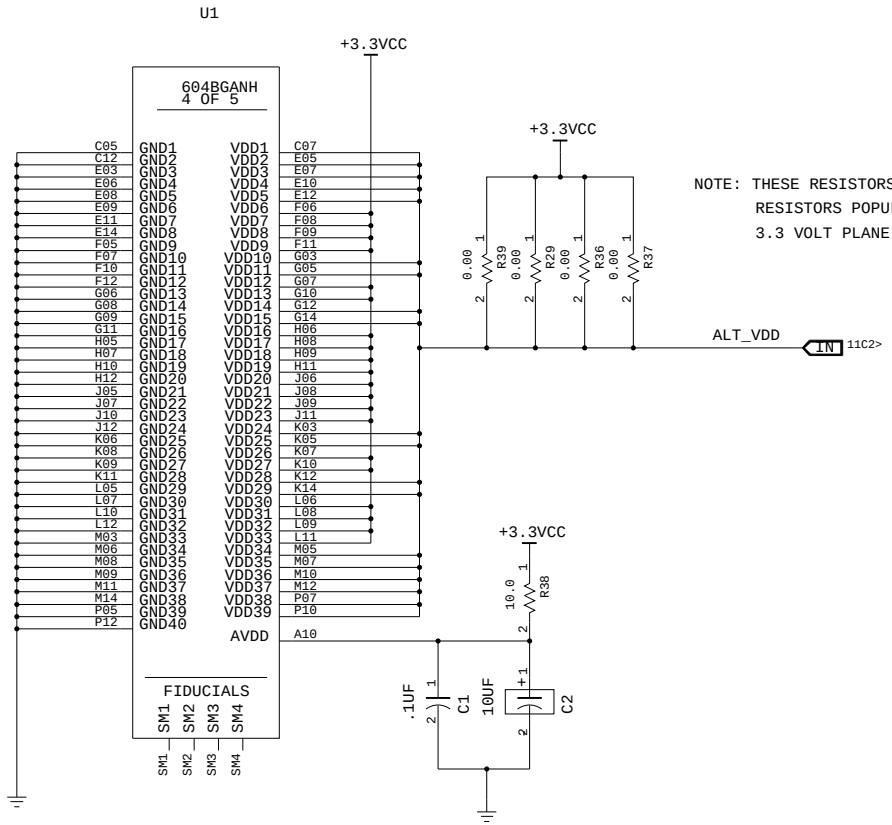

+3.3VCC
DRIVE MODE: (0:1)
00 DRIVER DISABLED
01 NORMAL DRIVE
10 STRONG DRIVE
11 HERCULEAN DRIVE
U1
604BGANH
3 OF 5
CHECKSTOP*
CKSTP_IN*
INT*
SRESET*
HRESET*
DPE*
APE*
RSRV*
SYSCLK
MCP*
SMI*
DBWO*
TBEN
PLL_CFG(0)
PLL_CFG(1)
PLL_CFG(2)
PLL_CFG(3)
TRST*
TMS
TCK
TDI
TDO
DRVMOD(1)
DRVMOD(0)
RUN
HALTED
INT_A*
SRESET_A*
HRESET_A*
MCP_A*
SMI*
604_SYSCLK
ECL
TRST*
TMS
TCK
TDI
CHECKSTOP*
DPE*
APE*
RSRV*
TBEN
FREQ_ID0
FREQ_ID1
FREQ_ID2
FREQ_ID3
TDO
DRVMOD1
DRVMOD0
RUN/QACK
HALT_A/QREQ_A
SYS_DBWO*
NOTE:
POPULATE R12, NO POP R22 AND R26 FOR NO DELAY
POPULATE R22 AND R26, NO POP R12 FOR 1 NS DELAY
IBM
604CPU
DATE: 27 SEPT 1995
SIZE B
REVISION
DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD
SHEET 7 OF 15
CPU





IBM			604CPU	
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01	
POWERPC 604 SMP CHEETAH0 CPU CARD			SHEET 8 OF 15	

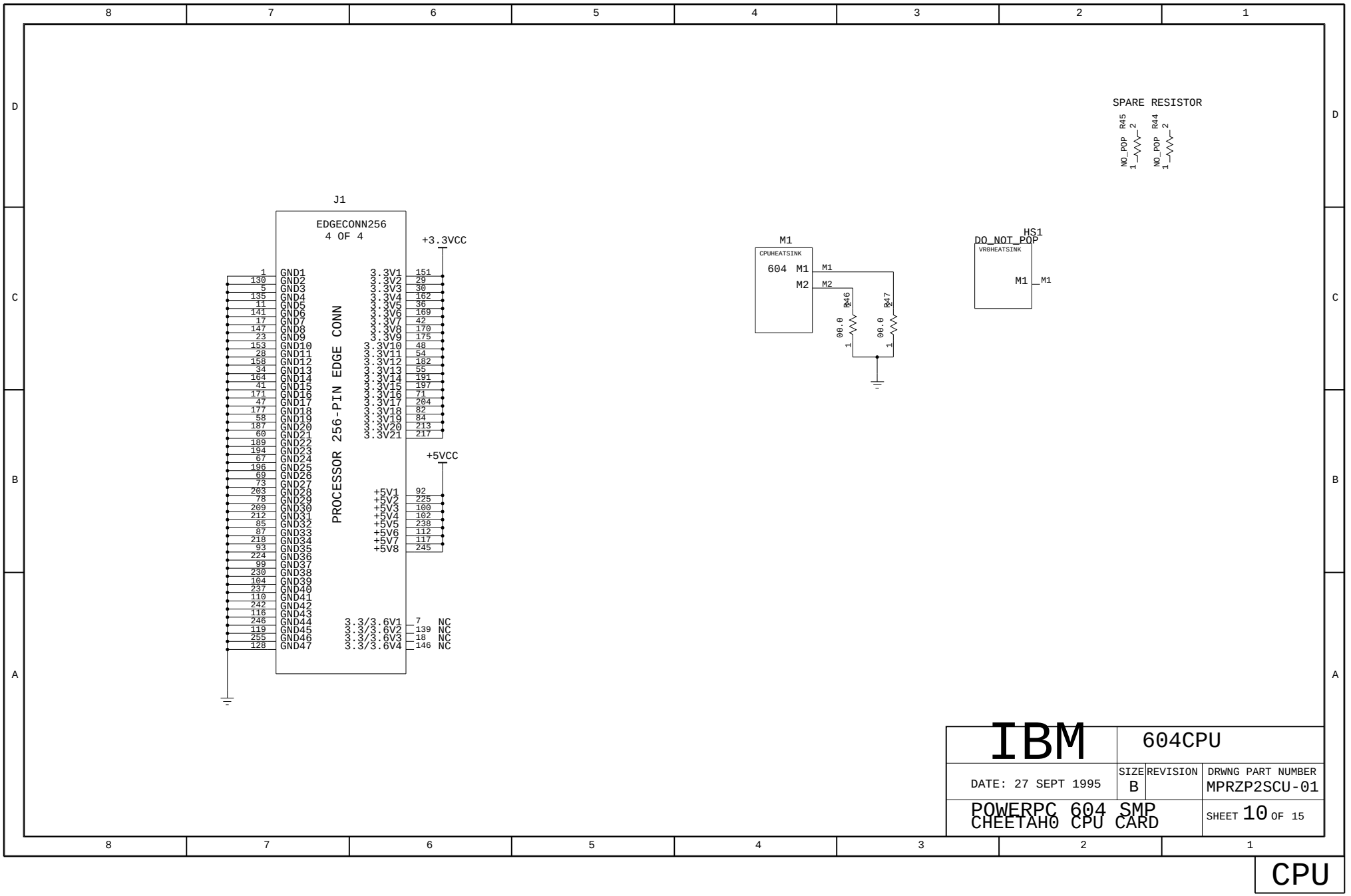
CPU



NOTE: THESE RESISTORS NOT POPULATED FOR 604+.
RESISTORS POPULATED FOR 604 TYING
3.3 VOLT PLANE TO ALT_VDD PLANE.

IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 9 OF 15		

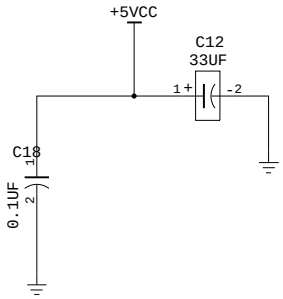
CPU

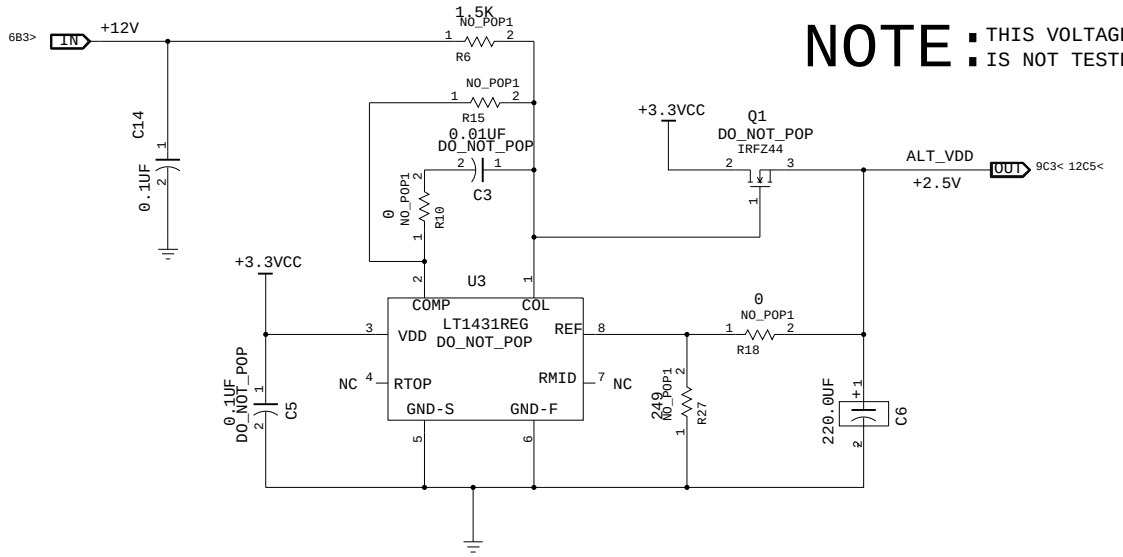


IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 10 OF 15		

CPU

BULK DECOUPLING CAPS





NOTE: VOLTAGE REGULATOR PARTS POPULATED FOR 604+

AND NOT POPULATED FOR 604 (EXCEPT C6).

NOTE: THIS VOLTAGE REGULATOR CIRCUIT IS NOT TESTED AND SUPPORTED.

IBM	604CPU		
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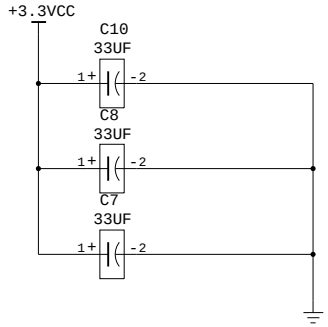
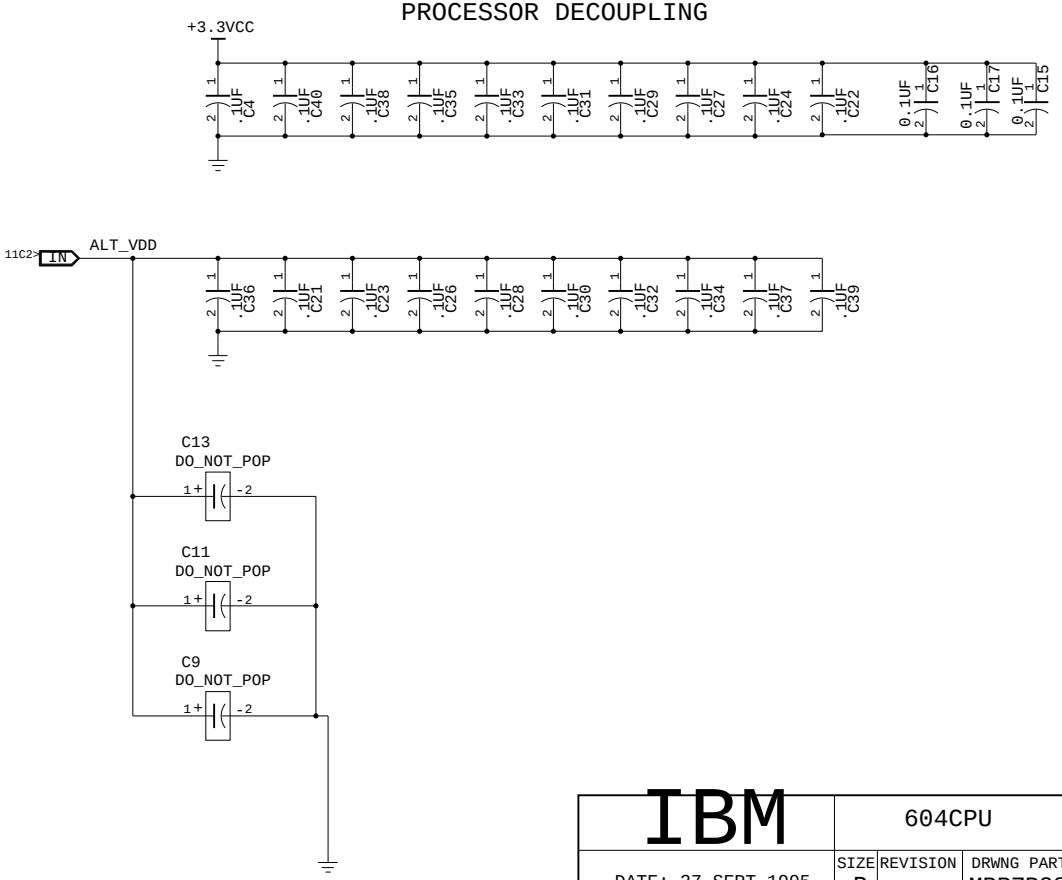
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 11 OF 15		

CPU

BULK DECOUPLING FOR PROCESSOR



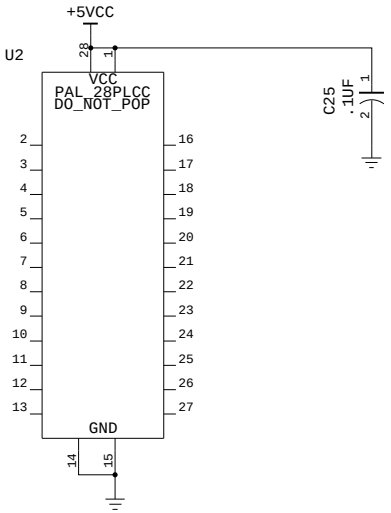
PROCESSOR DECOUPLING



IBM	604CPU		
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD	SHEET 12 OF 15		

CPU

SPARE PAL



IBM			604CPU	
DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01	
POWERPC 604 SMP CHEETAH0 CPU CARD			SHEET 13 OF 15	

CPU

*** Signal Cross-Reference ***
--- for the entire design --

+12V	6B3> 11D6<
604_SYSCLK	6B3> 7B8<
ALT_VDD	11C2> 9C3< 12C5<
APE *	7C1> 8B7<
CHECKSTOP *	6B3<> 7D1<>
CONFIG *	5A6>
DPE *	7C1> 6A3< 8B7<
DRTRY *	6C3> 4D6<
DRVMOD0	6B3> 7A1<
DRVMOD1	6B3> 7A1<
FREQ_ID0	6B3> 7B1<
FREQ_ID1	6B3> 7B1<
FREQ_ID2	6A3> 7B1<
FREQ_ID3	6A3> 7B1<
HALT_A/QREQ_A	7A1> 6B3<
HRESET_A *	6D3> 7C8< 8B7<
INT_A *	6D3> 7C8< 8B7<
L2_INT	8B3
MCP_A *	6D3> 7C8<
PD0	6C4
PD1	6C4
PD2	6C4
PD3	6C4
RSRV *	7C1> 8B7<
RUN/QACK	6B3> 7A1<
SMI *	6D3> 7C8<
SRESET_A *	6D3> 7C8< 8B7<
SYS_AACK *	5D6
SYS_ABB *	5D6
SYS_ADDR <31..0>	5C6
SYS_AP <3..0>	5B6
SYS_ARTRY *	5D6
SYS_BG *	5D6
SYS_BR *	5D3> 8C7<
SYS_CI *	5A6
SYS_DATAH <31..0>	4D6
SYS_DATAL <31..0>	4B6
SYS_DATAP <7..0>	4A6 4B6
SYS_DBB *	4D6
SYS_DBG *	4D6
SYS_DBWO *	7C4
SYS_GBL *	5A6
SYS_SHD *	5D6
SYS_TA *	4D6
SYS_TBST *	5A6
SYS_TEA *	4D6
SYS_TS *	5C6
SYS_TSIZ <2..0>	5A6
SYS_TT <4..0>	5B6
SYS_WT *	5A6
SYS_XATS *	5C6
TBEN	6B3> 7B1<
TC <2..0>	5A3> 8C7<
TCK	6C3> 7B8<
TDI	6C3> 7B8<
TDO	7B1> 6C3<
TMS	6C3> 7B8<
TRST *	6C3> 7B8<

IBM

DATE: 27 SEPT 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP2SCU-01
POWERPC 604 SMP CHEETAH0 CPU CARD			SHEET 14 OF 15

CPU

*** Unit Cross-Reference ***
--- for the entire design --

C1	CAP	9A4
C2	CAPPLUS	9A4
C3	CAP	11C4
C4	CAP	12C4
C5	CAP	11B5
C6	CAPPLUS	11B2
C7	CAPPLUS	12C7
C8	CAPPLUS	12C7
C9	CAPPLUS	12A4
C10	CAPPLUS	12C7
C11	CAPPLUS	12B4
C12	CAPPLUS	11C7
C13	CAPPLUS	12B4
C14	CAP	11C6
C15	CAP	12C1
C16	CAP	12C1
C17	CAP	12C1
C18	CAP	11B8
C21	CAP	12B4
C22	CAP	12C2
C23	CAP	12B4
C24	CAP	12C2
C25	CAP	13C6
C26	CAP	12B3
C27	CAP	12C2
C28	CAP	12B3
C29	CAP	12C3
C30	CAP	12B3
C31	CAP	12C3
C32	CAP	12B3
C33	CAP	12C3
C34	CAP	12B2
C35	CAP	12C3
C36	CAP	12B4
C37	CAP	12B2
C38	CAP	12C4
C39	CAP	12B2
C40	CAP	12C4
HS1	VR0HEATSINK	10C2
J1	EDGECONN256	4D7 5D7 6D5 10D7
J2	CONN_TEST14	8C6
M1	CPUHEATSINK	10C4
Q1	IRFZ44A	11D3
R1	RESISTOR	7D5
R2	RESISTOR	7A4
R3	RESISTOR	8C3
R4	RESISTOR	7D2
R5	RESISTOR	7D6
R6	RESISTOR	11D4
R7	RESISTOR	7D3
R8	RESISTOR	7D6
R9	RESISTOR	7D2
R10	RESISTOR	11C4
R11	RESISTOR	7D6
R12	RESISTOR	7B7
R13	RESISTOR	7D2
R14	RESISTOR	8A3
R15	RESISTOR	11D4
R16	RESISTOR	7D3
R17	RESISTOR	7D3
R18	RESISTOR	11C3
R19	RESISTOR	7D3
R20	RESISTOR	7D3
R21	RESISTOR	7D6
R22	RESISTOR	7B6
R23	RESISTOR	8C2
R24	RESISTOR	7D6
R25	RESISTOR	7C7
R26	RESISTOR	7B7
R27	RESISTOR	11B3
R28	RESISTOR	8C2
R29	RESISTOR	9C4
R30	RESISTOR	8C2
R31	RESISTOR	7D3
R32	RESISTOR	7D2
R33	RESISTOR	5D4
R34	RESISTOR	7D2
R35	RESISTOR	4D3
R36	RESISTOR	9C4
R37	RESISTOR	9C4
R38	RESISTOR	9B4
R39	RESISTOR	9C4
R40	RESISTOR	6C3
R41	RESISTOR	6C3
R42	RESISTOR	6C3
R43	RESISTOR	6C3
R44	RESISTOR	10D2
R45	RESISTOR	10D2
R46	RESISTOR	10C3
R47	RESISTOR	10C3
U1	604BGANH	4D4 5D5 7D5 8C3 9D5
U2	PAL_28PLCC	13D8
U3	LT1431REG	11C4

IBM

DATE: 27 SEPT 1995

SIZE: B

REVISION:

DRWNG PART NUMBER: MPRZP2SCU-01

POWERPC 604 SMP
CHEETAH0 CPU CARD

SHEET 15 OF 15

CPU

POWERPC 604 SMP RISER CARD SCHEMATICS

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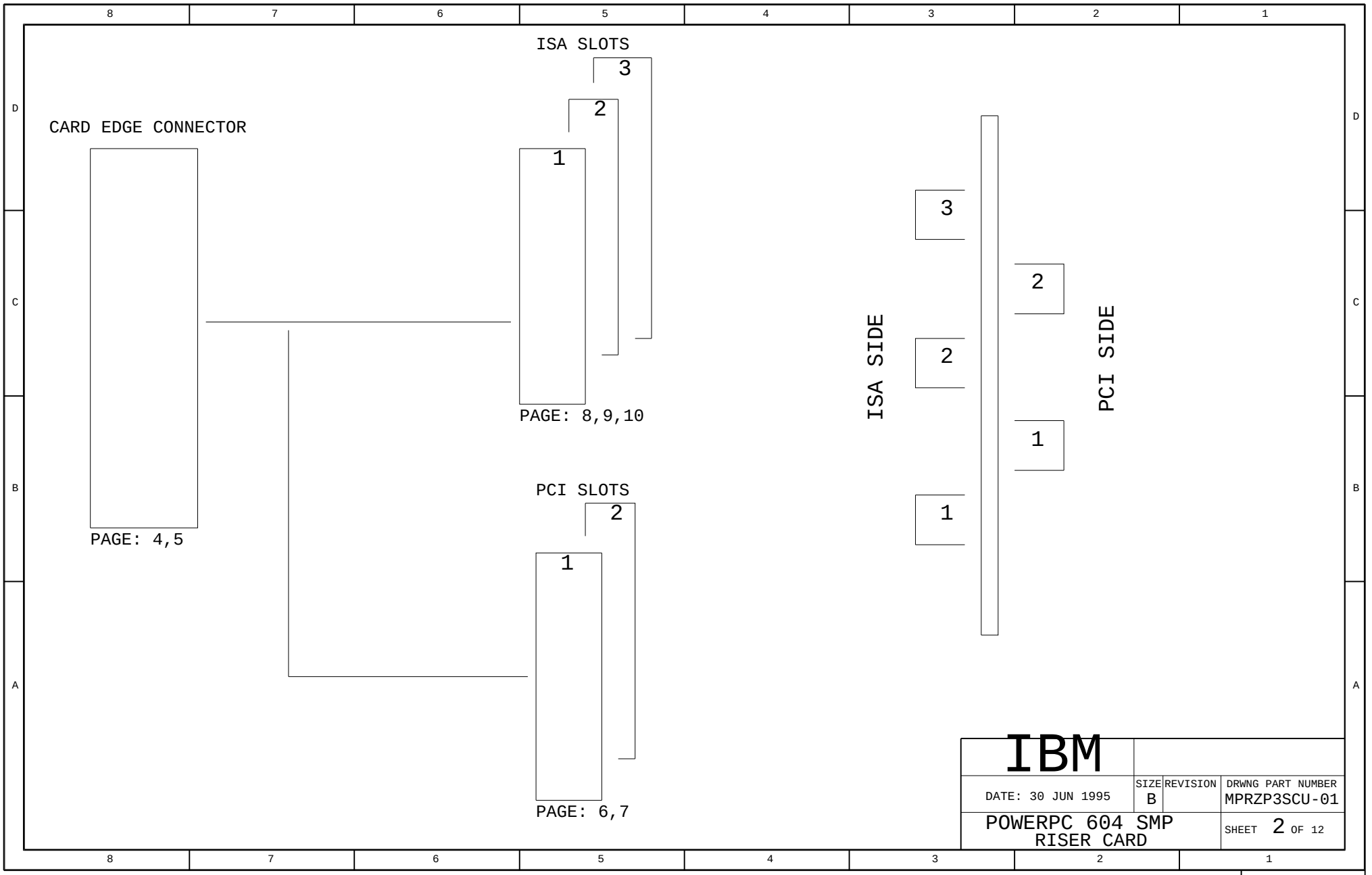
IBM			
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
POWERPC 604 SMP RISER CARD			SHEET 1 OF 12

RISER



IBM			
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
POWERPC 604 SMP RISER CARD			SHEET 2 OF 12

RISER

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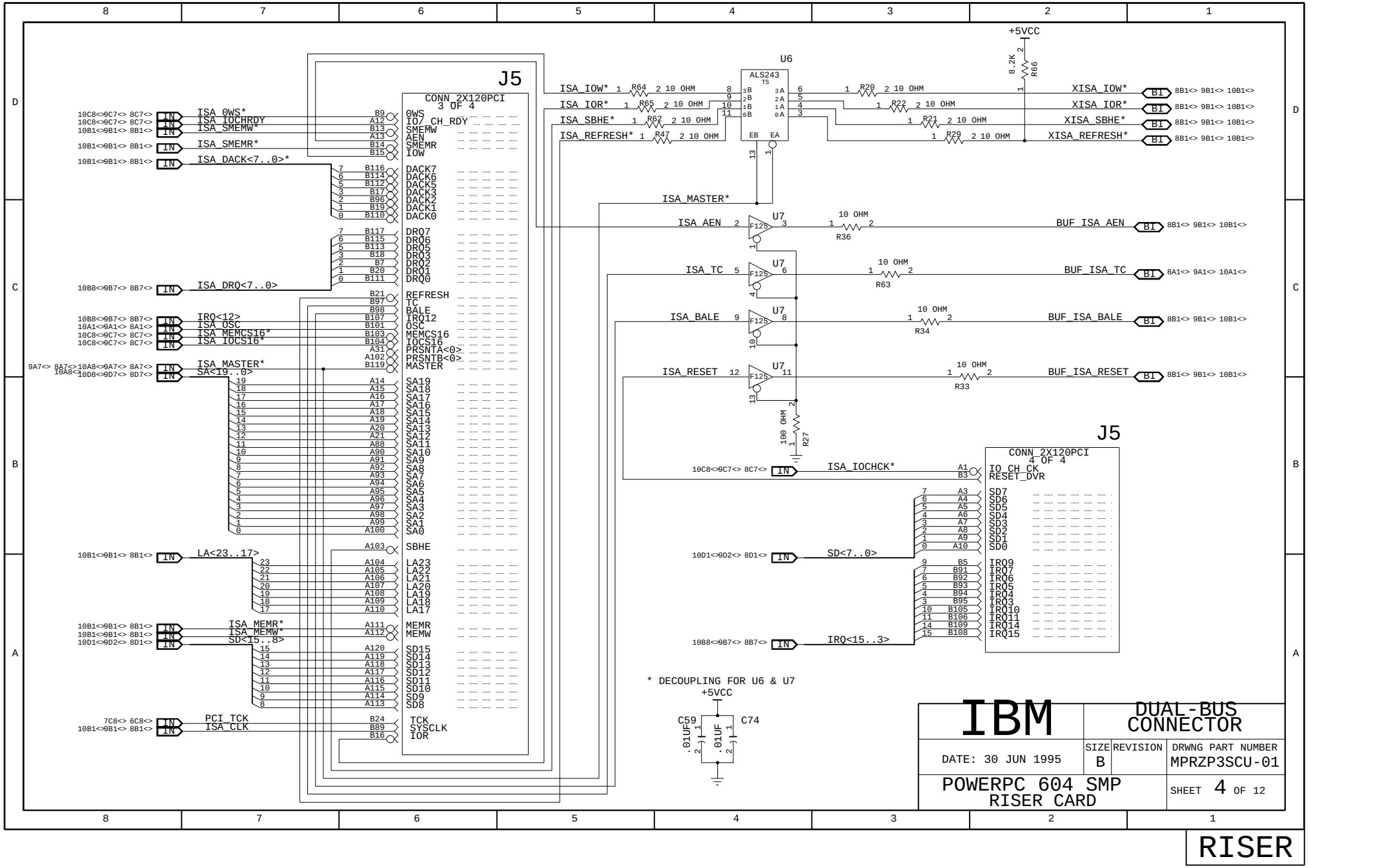
IBM

DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
POWERPC 604 SMP RISER CARD			SHEET 3 OF 12

RISER

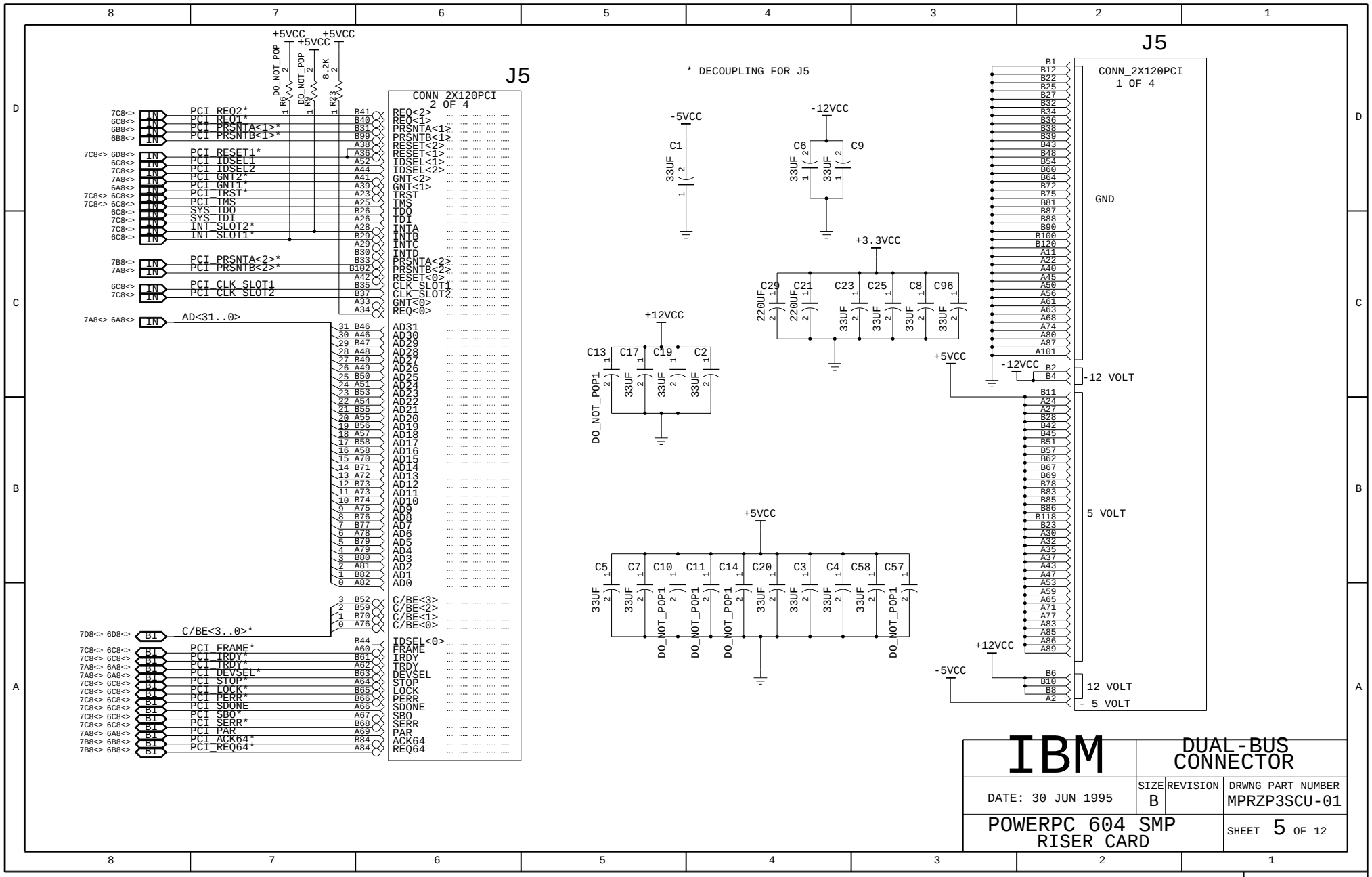


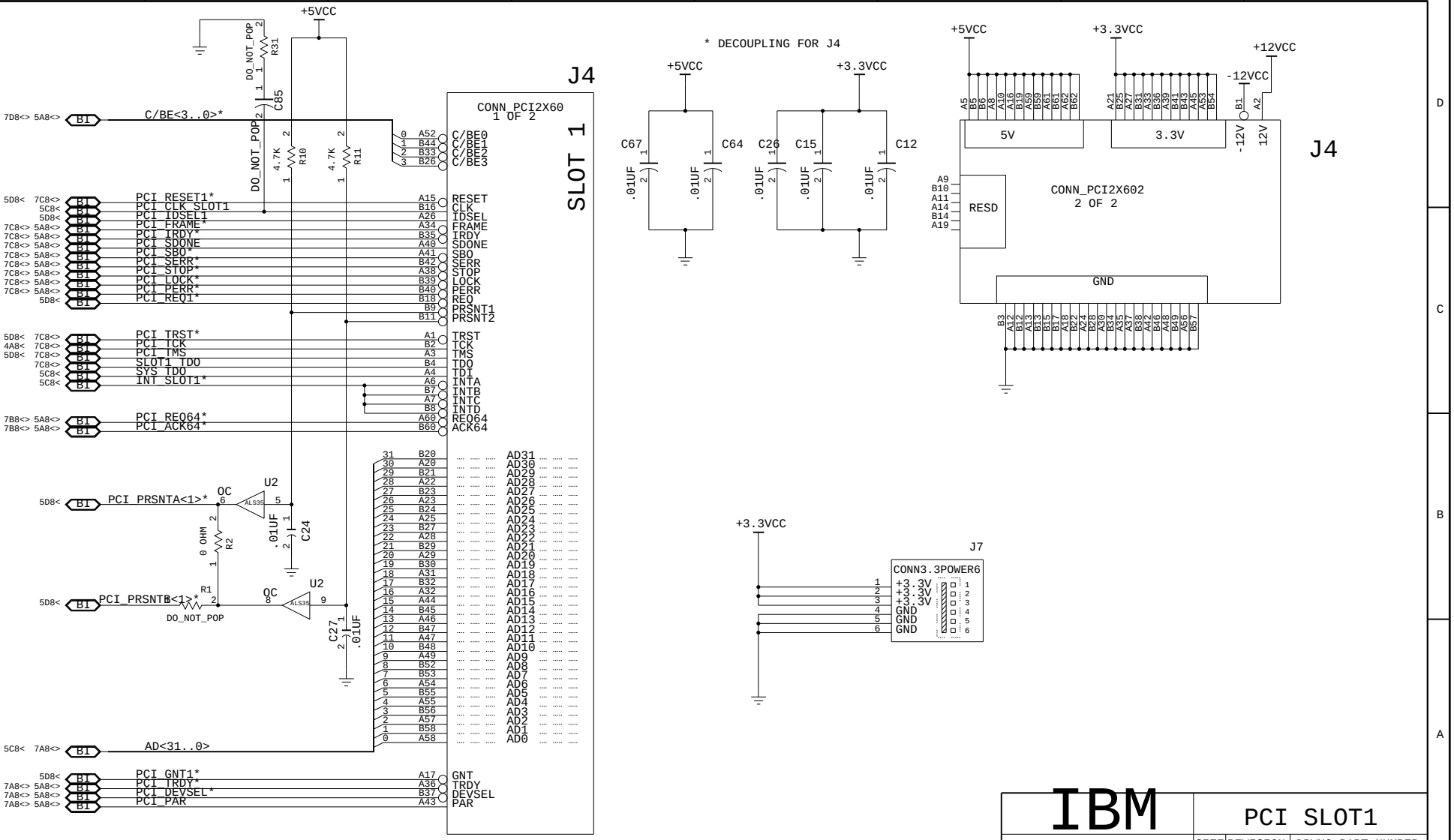
IBM

DUAL-BUS CONNECTOR

DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
POWERPC 604 SMP RISER CARD			SHEET 4 OF 12

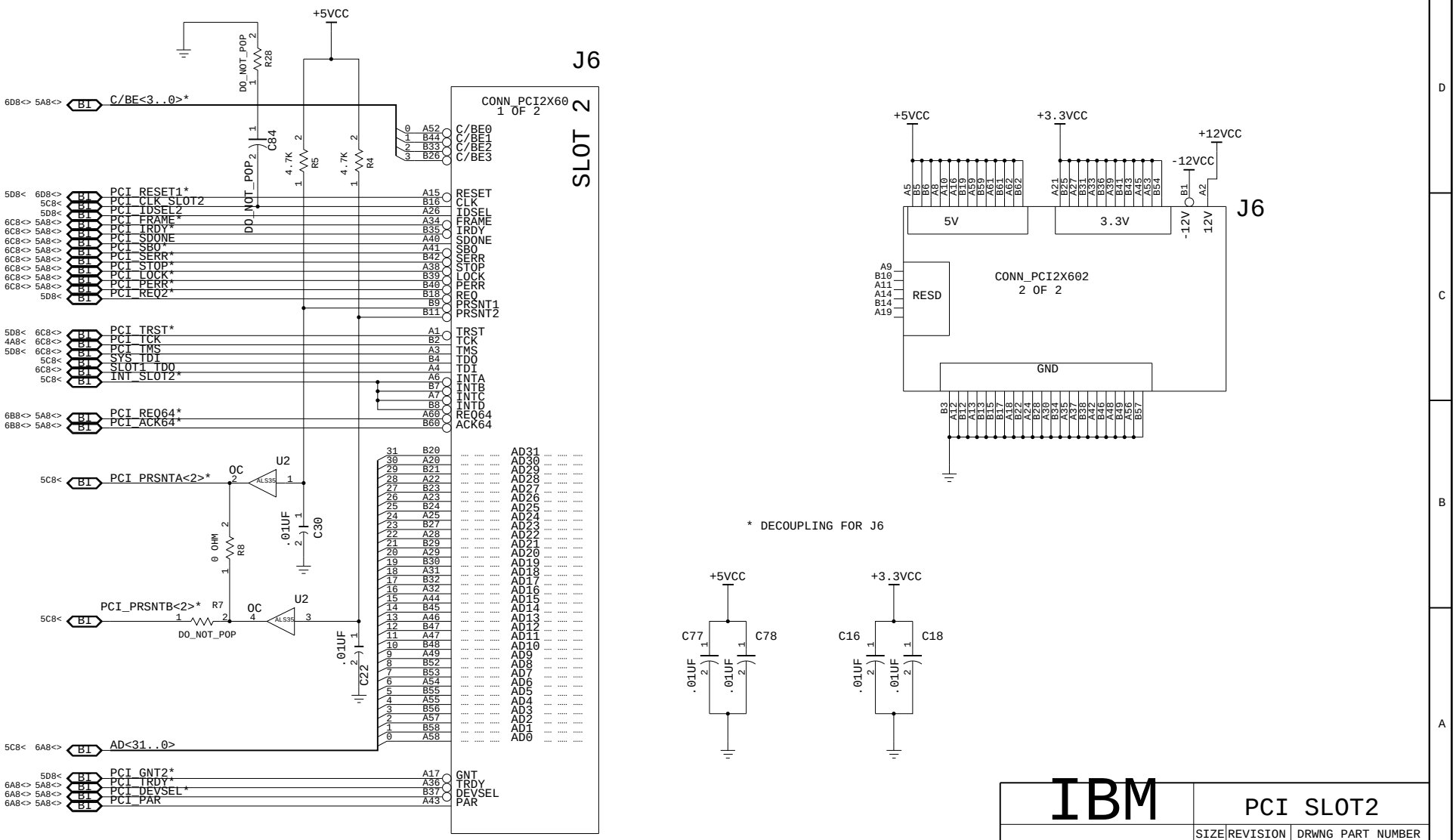
RISER


J5
CONN_2X120PCI
2 OF 4
J5
CONN_2X120PCI
1 OF 4
* DECOUPLING FOR J5
+5VCC
-5VCC
+12VCC
-12VCC
+3.3VCC
DO_NOT_POP
8.2K
PCI_REQ2*
PCI_REQ1*
PCI_PRSNTA<1>*
PCI_PRSNTB<1>*
PCI_RESET1*
PCI_IDSEL1
PCI_IDSEL2
PCI_GNT2*
PCI_GNT1*
PCI_TRST*
PCI_TMS
SYS_TDO
SYS_TDI
INT_SLOT2*
INT_SLOT1*
PCI_PRSNTA<2>*
PCI_PRSNTB<2>*
PCI_CLK_SLOT1
PCI_CLK_SLOT2
AD<31..0>
C/BE<3..0>*
PCI_FRAME*
PCI_IRDY*
PCI_TRDY*
PCI_DEVSEL*
PCI_STOP*
PCI_LOCK*
PCI_PERR*
PCI_SDONE
PCI_SBO*
PCI_SERR*
PCI_PAR
PCI_ACK64*
PCI_REQ64*
GND
-12 VOLT
5 VOLT
12 VOLT
- 5 VOLT
IBM
DUAL-BUS
CONNECTOR
DATE: 30 JUN 1995
SIZE B
REVISION
DRWNG PART NUMBER
MPRZP3SCU-01
POWERPC 604 SMP
RISER CARD
SHEET 5 OF 12
RISER



IBM	PCI SLOT1		
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
POWERPC 604 SMP RISER CARD	SHEET 6 OF 12		

RISER



IBM			PCI SLOT2
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
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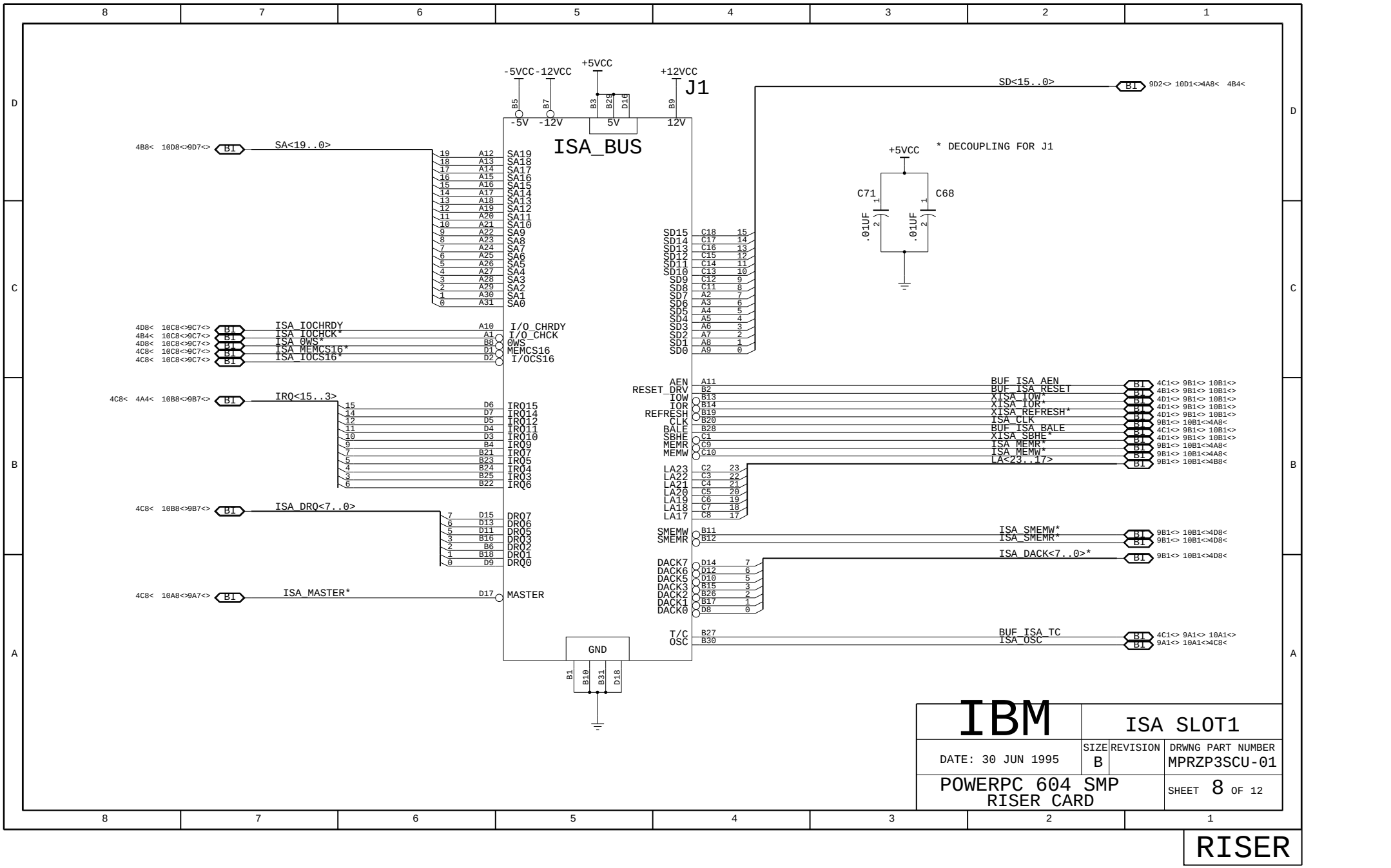
RISER



IBM	ISA SLOT1		
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
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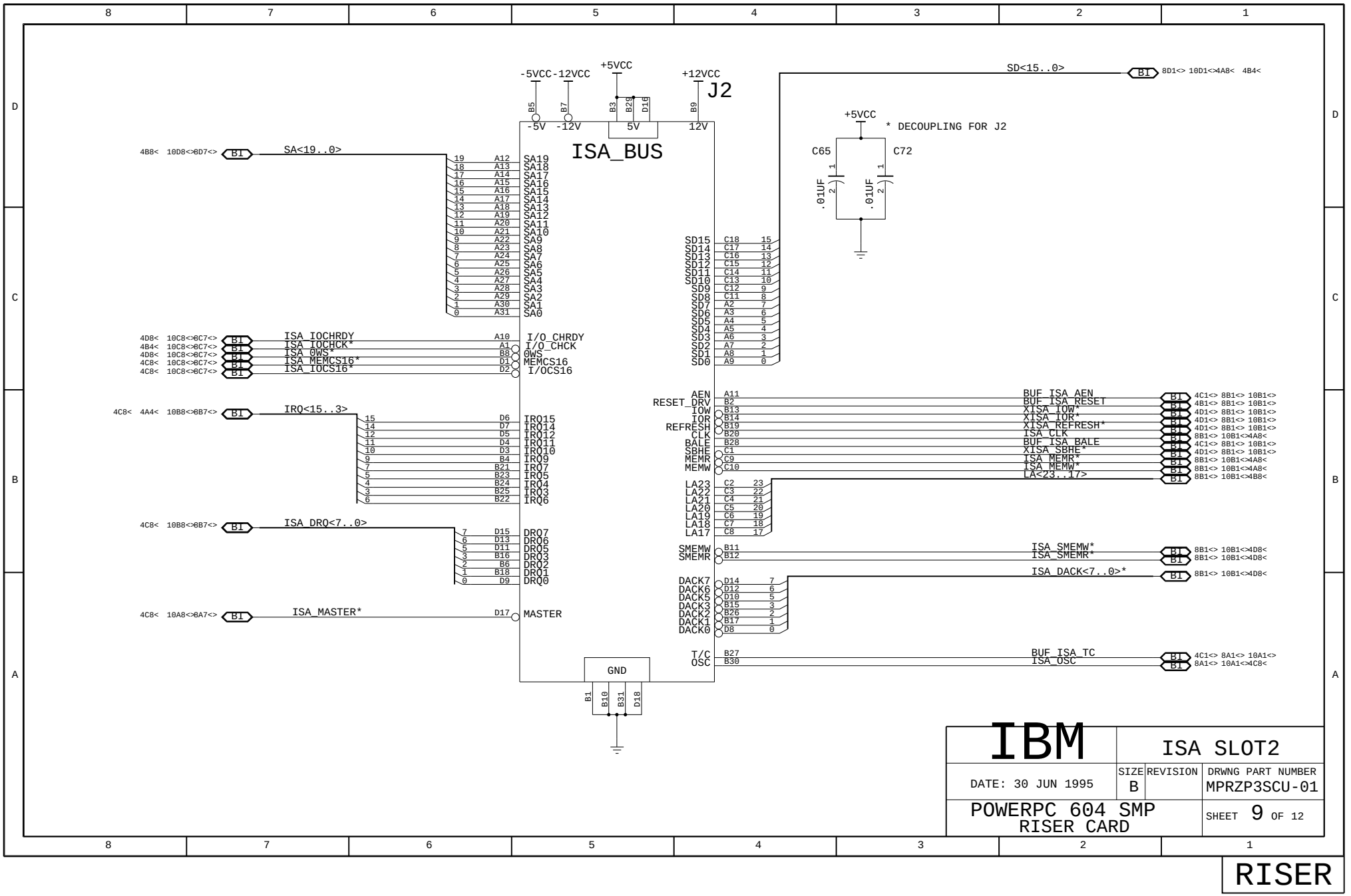

IBM	ISA SLOT2		
DATE: 30 JUN 1995	SIZE B	REVISION	DRWNG PART NUMBER MPRZP3SCU-01
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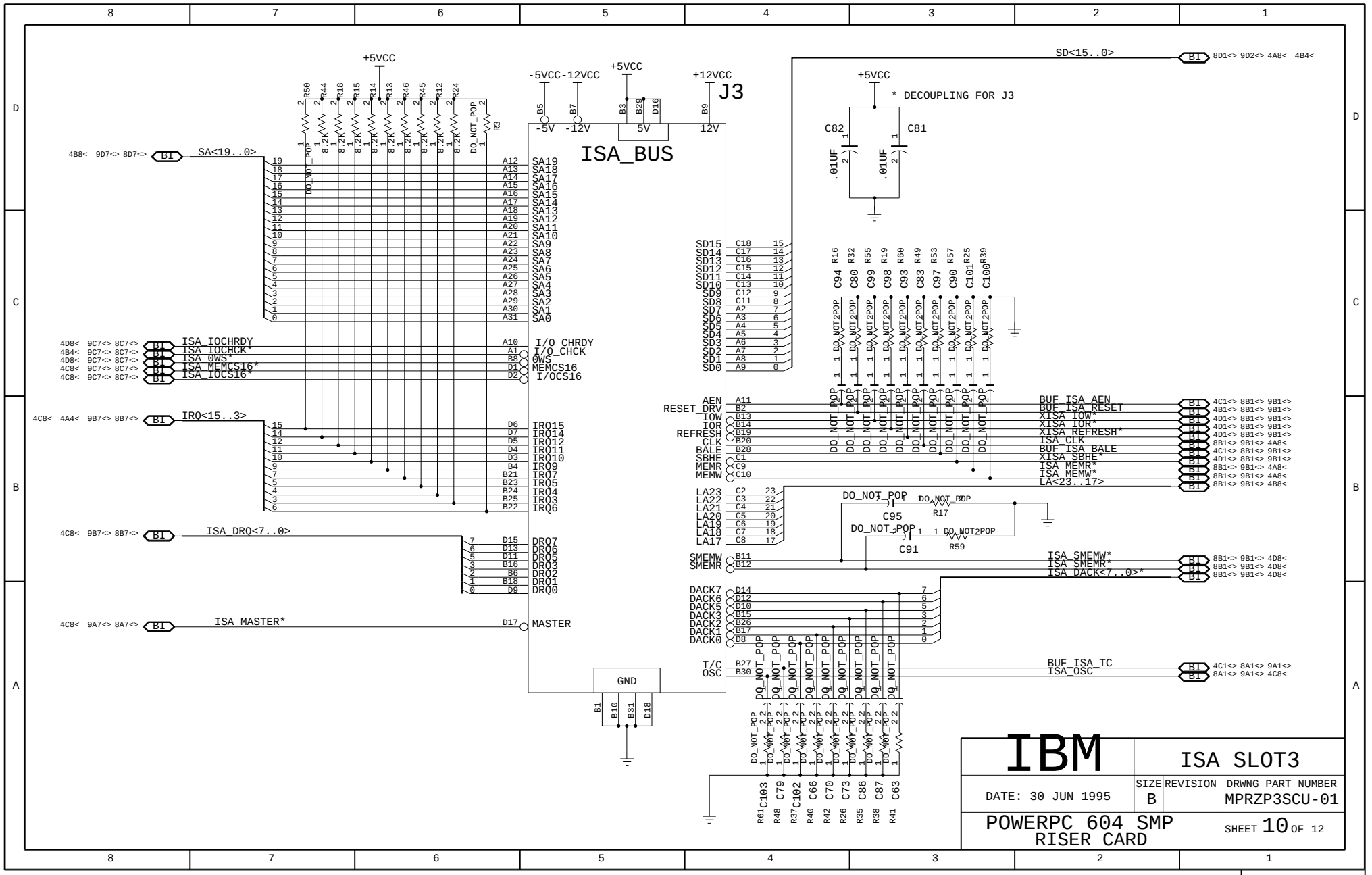
RISER


J3
ISA_BUS
+5VCC
-5VCC
-12VCC
+12VCC
-5V
-12V
5V
12V
* DECOUPLING FOR J3
SD<15..0>
SA<19..0>
IRQ<15..3>
ISA_DRQ<7..0>
ISA_MASTER*
ISA_IOCHRDY
ISA_IOCHCK*
ISA_0WS*
ISA_MEMCS16*
ISA_IOCS16*
I/O_CHRDY
I/O_CHCK
0WS
MEMCS16
I/OCS16
MASTER
AEN
RESET_DRV
IOW
IOR
REFRESH
CLK
BALE
SBHE
MEMR
MEMW
LA23
LA22
LA21
LA20
LA19
LA18
LA17
SMEMW
SMEMR
DACK7
DACK6
DACK5
DACK3
DACK2
DACK1
DACK0
T/C
OSC
BUF_ISA_AEN
BUF_ISA_RESET
XISA_IOW*
XISA_IOR*
XISA_REFRESH*
ISA_CLK
BUF_ISA_BALE
XISA_SBHE*
ISA_MEMR*
ISA_MEMW*
LA<23..17>
ISA_SMEMW*
ISA_SMEMR*
ISA_DACK<7..0>*
BUF_ISA_TC
ISA_OSC
GND
DO_NOT_POP
.01UF
C82
C81
C95
C91
R17
R59
IBM
ISA SLOT3
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*** Signal Cross-Reference ***
--- for the entire design --

```
AD <31..0>      6A8<> 7A8<> 5C8<
BUF_ISA_AEN     4C1<> 8B1<> 9B1<> 10B1<>
BUF_ISA_BALE    4C1<> 8B1<> 9B1<> 10B1<>
BUF_ISA_RESET   4B1<> 8B1<> 9B1<> 10B1<>
BUF_ISA_TC      4C1<> 8A1<> 9A1<> 10A1<>
C/BE <3..0> *   5A8<> 6D8<> 7D8<>
INT_SLOT1 *     6C8<> 5C8<
INT_SLOT2 *     7C8<> 5C8<
IRQ <15..3>     8B7<> 9B7<> 10B8<> 4A4< 4C8<
ISA_0WS *       8C7<> 9C7<> 10C8<> 4D8<
ISA_AEN         4C4
ISA_BALE        4C4
ISA_CLK         8B1<> 9B1<> 10B1<> 4A8<
ISA_DACK <7..0> * 8B1<> 9B1<> 10B1<> 4D8<
ISA_DRQ <7..0>  8B7<> 9B7<> 10B8<> 4C8<
ISA_IOCHCK *    8C7<> 9C7<> 10C8<> 4B4<
ISA_IOCHRDY     8C7<> 9C7<> 10C8<> 4D8<
ISA_IOCS16 *    8C7<> 9C7<> 10C8<> 4C8<
ISA_IOR *       4D5
ISA_IOW *       4D5
ISA_MASTER *    8A7<> 9A7<> 10A8<> 4C8<
ISA_MEMCS16 *   8C7<> 9C7<> 10C8<> 4C8<
ISA_MEMR *      8B1<> 9B1<> 10B1<> 4A8<
ISA_MEMW *      8B1<> 9B1<> 10B1<> 4A8<
ISA_OSC         8A1<> 9A1<> 10A1<> 4C8<
ISA_REFRESH *   4D5
ISA_RESET       4B4
ISA_SBHE *      4D5
ISA_SMEMR *     8B1<> 9B1<> 10B1<> 4D8<
ISA_SMEMW *     8B1<> 9B1<> 10B1<> 4D8<
ISA_TC          4C4
LA <23..17>     8B1<> 9B1<> 10B1<> 4B8<
PCI_ACK64 *     5A8<> 6B8<> 7B8<>
PCI_CLK_SLOT1   6C8<> 5C8<
PCI_CLK_SLOT2   7C8<> 5C8<
PCI_DEVSEL *    5A8<> 6A8<> 7A8<>
PCI_FRAME *     5A8<> 6C8<> 7C8<>
PCI_GNT1 *      6A8<> 5D8<
PCI_GNT2 *      7A8<> 5D8<
PCI_IDSEL1      6C8<> 5D8<
PCI_IDSEL2      7C8<> 5D8<
PCI_IRDY *      5A8<> 6C8<> 7C8<>
PCI_LOCK *      5A8<> 6C8<> 7C8<>
PCI_PAR         5A8<> 6A8<> 7A8<>
PCI_PERR *      5A8<> 6C8<> 7C8<>
PCI_PRSNTA <2..1> * 6B8<> 7B8<> 5C8< 5D8<
PCI_PRSNTB <2..1> * 6B8<> 7A8<> 5C8< 5D8<
PCI_REQ1 *      6C8<> 5D8<
PCI_REQ2 *      7C8<> 5D8<
PCI_REQ64 *     5A8<> 6B8<> 7B8<>
PCI_RESET1 *    6D8<> 7C8<> 5D8<
PCI_SBO *       5A8<> 6C8<> 7C8<>
PCI_SDONE       5A8<> 6C8<> 7C8<>
PCI_SERR *      5A8<> 6C8<> 7C8<>
PCI_STOP *      5A8<> 6C8<> 7C8<>
PCI_TCK         6C8<> 7C8<> 4A8<
PCI_TMS         6C8<> 7C8<> 5D8<
PCI_TRDY *      5A8<> 6A8<> 7A8<>
PCI_TRST *      6C8<> 7C8<> 5D8<
SA <19..0>      8D7<> 9D7<> 10D8<> 4B8<
SD <15..0>      8D1<> 9D2<> 10D1<> 4A8< 4B4<
SLOT1_TDO       6C8<> 7C8<>
SYS_TDI         7C8<> 5C8<
SYS_TDO         6C8<> 5C8<
XISA_IOR *      4D1<> 8B1<> 9B1<> 10B1<>
XISA_IOW *      4D1<> 8B1<> 9B1<> 10B1<>
XISA_REFRESH *  4D1<> 8B1<> 9B1<> 10B1<>
XISA_SBHE *     4D1<> 8B1<> 9B1<> 10B1<>
```

IBM

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*** Unit Cross-Reference ***
--- for the entire design --

C1	CAP	5D5
C2	CAP	5C4
C3	CAP	5B4
C4	CAP	5B4
C5	CAP	5B5
C6	CAP	5D4
C7	CAP	5B5
C8	CAP	5C3
C9	CAP	5D4
C10	CAP	5B5
C11	CAP	5B5
C12	CAP	6D3
C13	CAP	5C5
C14	CAP	5B4
C15	CAP	6D4
C16	CAP	7A4
C17	CAP	5C5
C18	CAP	7A3
C19	CAP	5C5
C20	CAP	5B4
C21	CAP	5C4
C22	CAP	7A6
C23	CAP	5C4
C24	CAP	6B7
C25	CAP	5C3
C26	CAP	6D4
C27	CAP	6A6
C29	CAP	5C4
C30	CAP	7B6
C57	CAP	5B3
C58	CAP	5B4
C59	CAP	4A4
C63	CAP	10A3
C64	CAP	6D4
C65	CAP	9D4
C66	CAP	10A4
C67	CAP	6D5
C68	CAP	8D3
C70	CAP	10A4
C71	CAP	8D3
C72	CAP	9D3
C73	CAP	10A4
C74	CAP	4A4
C77	CAP	7A5
C78	CAP	7A4
C79	CAP	10A4
C80	CAP	10C3
C81	CAP	10D3
C82	CAP	10D4
C83	CAP	10C3
C84	CAP	7D7
C85	CAP	6D7
C86	CAP	10A3
C87	CAP	10A3
C90	CAP	10C3
C91	CAP	10B3
C93	CAP	10C3
C94	CAP	10C4
C95	CAP	10B3
C96	CAP	5C3
C97	CAP	10C3
C98	CAP	10C3
C99	CAP	10C3
C100	CAP	10C3
C101	CAP	10C3
C102	CAP	10A4
C103	CAP	10A4
J1	ISA_BUS	8D4
J2	ISA_BUS	9D4
J3	ISA_BUS	10D4
J4	CONN_PCI2X60	6D1 6D5
J5	CONN_2X120PCI	4B2 4D5 5D1 5D6
J6	CONN_PCI2X60	7C2 7D5
J7	CONN33POWER6	6B3
R1	RESISTOR	6B7
R2	RESISTOR	6B7
R3	RESISTOR	10D6
R4	RESISTOR	7D6
R5	RESISTOR	7D7
R6	RESISTOR	5D7
R7	RESISTOR	7B7
R8	RESISTOR	7B7
R9	RESISTOR	5D7
R10	RESISTOR	6D7
R11	RESISTOR	6D6
R12	RESISTOR	10D6
R13	RESISTOR	10D6
R14	RESISTOR	10D6
R15	RESISTOR	10D6
R16	RESISTOR	10C4
R17	RESISTOR	10B3
R18	RESISTOR	10D7
R19	RESISTOR	10C3
R20	RESISTOR	4D3
R21	RESISTOR	4D3
R22	RESISTOR	4D3
R23	RESISTOR	5D7
R24	RESISTOR	10D6
R25	RESISTOR	10C3
R26	RESISTOR	10A4
R27	RESISTOR	4B4
R28	RESISTOR	7D7
R29	RESISTOR	4D3
R31	RESISTOR	6D7
R32	RESISTOR	10C3
R33	RESISTOR	4B3
R34	RESISTOR	4C3
R35	RESISTOR	10A3
R36	RESISTOR	4C3
R37	RESISTOR	10A4
R38	RESISTOR	10A3
R39	RESISTOR	10C3
R40	RESISTOR	10A4
R41	RESISTOR	10A3
R42	RESISTOR	10A4
R44	RESISTOR	10D7
R45	RESISTOR	10D6
R46	RESISTOR	10D6
R47	RESISTOR	4D4
R48	RESISTOR	10A4
R49	RESISTOR	10C3
R50	RESISTOR	10D7
R53	RESISTOR	10C3
R55	RESISTOR	10C3
R57	RESISTOR	10C3
R59	RESISTOR	10B3
R60	RESISTOR	10C3
R61	RESISTOR	10A4
R62	RESISTOR	4D5
R63	RESISTOR	4C3
R64	RESISTOR	4D5
R65	RESISTOR	4D5
R66	RESISTOR	4D2
U2	ALS35	6B7 7B7
U6	ALS243	4D4
U7	F125	4C4

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Section 22
Data Sheets

This section contains data sheets on selected components. IBM does not recommend the use of components from any particular manufacturer (other than IBM). The following data sheets are included as reference material only. Third party material is reproduced and included by permission of the copyright owner. Note that some material has been sourced from data books, and so may have page numbers that are non-one based and noncontiguous.

PowerPC Multiprocessor Interrupt Controller (MPIC)

January 19, 1996

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PowerPC MP Interrupt Controller - MPIC

This document describes the MPIC-2A interrupt controller designed for use with PowerPC-based multiprocessor (and uniprocessor) systems. The MPIC-2A ASIC is compatible with the Open PIC Multiprocessor Interrupt Controller Register Interface Specification Revision 1.2 dated 4/95. Comments are welcome!

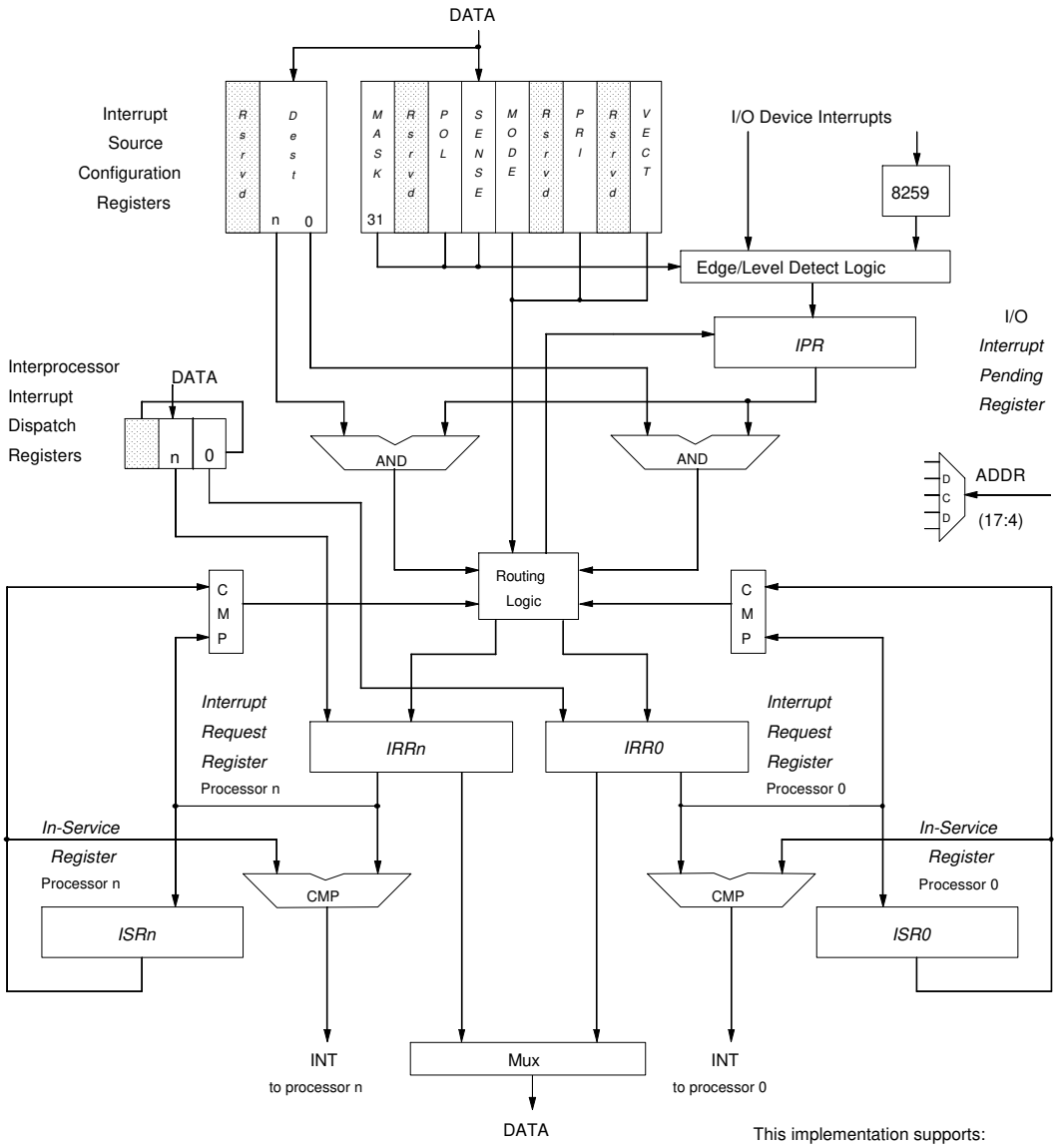
The few minor differences (improvements!) between the earlier MPIC-2 ASIC, which was built to version 1.0 of the Open PIC spec, and the newer MPIC-2A ASIC are also described in this document. Software written for MPIC-2 is upwardly compatible with MPIC-2A.

1. MPIC Functional Description

MPIC-2A supports
- 16 I/O device interrupts
- Up to 4 processors (0 through 3)
- 4 interprocessor interrupts
- 4 Global timers

An 8259A compatible interrupt controller can be connected to interrupt input 0.

PowerPC MP Interrupt Controller - MPIC



DWM 10/18/94

This implementation supports:

- 2 - 4 processors
- 2 - 4 interprocessor interrupts
- 12 - 16 I/O device interrupts
- + dual 8259 Cascade

1.1 Interrupt Source Configuration Registers

This section describes the Interrupt Source Configuration Registers and related logic. Each Interrupt Source Configuration Register (one per interrupt source) includes a Vector/Priority Register and a Destination Register. Each interrupt source also has a corresponding bit in the I/O Interrupt Pending Register.

1.1.1 Vector/Priority Register

Vector/Priority Registers -- Read/Write -- Offsets 0x10000, 20, 40, 60...

31	30	24	22	20	16	8	0
MSK	ACT	Res.	POL	S	Res	Res	Pri	Reserved for Vector Expansion	Vector

Vector: Interrupt Vector
Pri: Interrupt Priority. 0 is the lowest priority; 15 is the highest priority.
S: Sense:
0 = Edge Triggered, 1 = Level Triggered.
POL: Polarity:
0 = Active Low or Negative Edge.
1 = Active High or Positive Edge.
ACT: Activity bit, read-only -- When set indicates the Vector, Priority and Destination information for this interrupt source are in use and should not be changed.
MSK: Mask bit -- Setting this bit disables any further interrupts from this source. Reset sets this bit to one.

Only Positive Edge Triggered and Active Low Level Triggered interrupt sources are supported for I/O interrupt sources 1 through 15.

Unless otherwise specified, reset sets all bits in all program accessible registers to zero.

1.1.2 Destination Register

Destination Registers -- Read/Write -- Offsets 0x10010, 30, 50, 70...

31	0
Select Processors 31:0	

This register indicates the destination processor(s) for this interrupt source. If a single destination processor is selected (Directed delivery mode) then interrupts from this source are directed to that processor. If multiple destination processors are selected (Distributed delivery mode) then interrupts from this source are distributed among the selected destination processors using a fair, implementation specific algorithm.

MPIC-2A supports 4 processors: processors 0 through 3[1].

[1]The MPIC-2 ASIC supports 2 processors: processor 0 and 1.

1.1.3 I/O Interrupt Pending Register

The I/O Interrupt Pending Register contains 1 bit per I/O interrupt input.

For edge triggered interrupts, a transition on an interrupt input sets the corresponding bit in the I/O Interrupt Pending Register. Interrupt Acknowledge resets this bit. For level triggered inputs, the corresponding bit in the I/O Interrupt Pending Register is active as long as the interrupt input is active.

MPIC is intended to be used in conjunction with an 8259A compatible interrupt controller. Interrupts from ISA devices should normally be connected to the 8259. If an 8259A compatible interrupt controller is used, it must be connected to interrupt input 0 on the MPIC. Interrupt input 0 should be programmed as active high level triggered.

Interrupts from PCI and other non-ISA devices should be connected to the remaining interrupt inputs on MPIC. It is recommended that each PCI card slot or device be connected to a separate interrupt input on MPIC. Interrupts (INTA#, INTB#, INTC#, INTD#) from the **same** PCI card slot or device can be OR'd together. Interrupts from **different** PCI card slots or devices should **NOT** be OR'd together. PCI interrupts should be programmed as active low level triggered. Tie-ups are required on the PCI interrupt lines.

Interrupts from ISA devices can be connected to MPIC in some cases. Please see the section entitled *Programming Notes*.

The I/O Interrupt Pending Register is implementation-dependent and is not program accessible.

Edge/Level Detect Logic

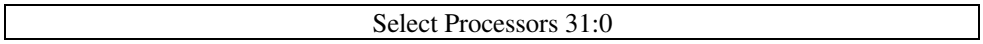
Each interrupt source can be programmed as either positive edge triggered or active low level triggered. Interrupt source 0 can also be programmed as active high level triggered. The Edge/Level Detect logic includes two levels of latches to compensate for potential metastability conditions with the interrupt inputs.

1.2 Per Processor Registers

This section describes the per processor registers and related logic.

1.2.1 Interprocessor Interrupt Dispatch Registers

Interprocessor Interrupt (IPI) 0 Dispatch Registers -- Write Only -- Offsets 0x20040, 21040, ...
Interprocessor Interrupt (IPI) 1 Dispatch Registers -- Write Only -- Offsets 0x20050, 21050, ...
Interprocessor Interrupt (IPI) 2 Dispatch Registers -- Write Only -- Offsets 0x20060, 21060, ...
Interprocessor Interrupt (IPI) 3 Dispatch Registers -- Write Only -- Offsets 0x20070, 21070, ...



There are 4 Interprocessor Interrupt (IPI) Dispatch Registers, 0 through 3. Writing to an IPI Dispatch Register causes an interprocessor interrupt request to be sent to one or more processors. A processor is interrupted if the bit in the IPI Dispatch Register corresponding to that processor is set during the write. Reading these registers returns zeros.

The IPI Dispatch registers are shared by all processors but are located, for convenience, in the per processor register page.

1.2.2 Current Task Priority Register

Current Task Priority Registers -- Read/Write -- Offsets 0x20080, 21080, ...

31 … 4	0
Reserved	Priority

There is one Task Priority Register per processor. Priority levels from 0 (lowest) to 15 (highest) are supported. Setting the Task Priority Register to 15 masks all interrupts to this processor because no interrupt source can have a priority higher than 15. (It is recommended, however, that PowerPC processors use the MSR_{EE} bit, rather than the Task Priority register, to disable external interrupts.) Reset sets the task priority registers to 0xF.

1.2.3 Interrupt Request Registers

There is one Interrupt Request Register per processor. The Interrupt Request Register contains the Priority, Vector and Interrupt Source identification for the highest priority pending interrupt for that processor.

Interrupt Acknowledge transfers the contents of this processor's Interrupt Request Register to this processor's In-Service Register.

As long as an interrupt is pending for, or in-service by, a processor, subsequent interrupts from the same interrupt source are routed to that processor till software issues End-of-Interrupt for that interrupt source.

The Interrupt Request Registers are implementation-dependent and are not program accessible.

1.2.3.1 Interrupt Routing

MPIC supports both 'Directed' and 'Distributed' delivery modes. In both modes, each processor's priority is calculated as the MAX of (Task Priority, IRR Priority, ISR Priority).

If a single destination processor is selected (Directed delivery mode), the interrupt is routed to **the** processor specified in the Destination field for this interrupt source **if** the interrupt's priority is higher than that processor's priority; otherwise the interrupt remains pending.

If multiple destination processors are selected (Distributed delivery mode), the interrupt is routed to **one** of the processors specified in the Destination field in the Interrupt Source Configuration Register for that interrupt source. MPIC-2 uses the following algorithm to route the interrupt:

- If an interrupt from the same interrupt source is already in service by a processor, the interrupt remains pending.
- If an interrupt from the same interrupt source is already pending in a processor's Interrupt Request Register, the interrupt is routed to that processor's Interrupt Request Register.
- Otherwise, processor priorities are compared. The interrupt is routed to the lowest priority processor specified in the Destination field for this interrupt source **if** the interrupt's priority is greater than that processor's priority; otherwise the interrupt remains pending. (A free-running 2-bit tie breaker counter is used to break ties among the processors.)

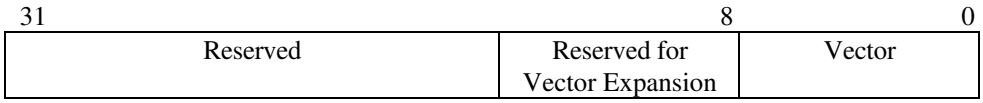
1.2.3.2 Interrupt Priority

MPIC supports programmable interrupt priority. Once a processor issues Interrupt Acknowledge, subsequent interrupts of equal or lower priority are blocked on that processor till that processor issues

End-of-Interrupt. Interrupt nesting (a higher priority interrupt preempts handling of a lower priority interrupt) is supported.

1.2.4 Interrupt Acknowledge Registers

Interrupt Acknowledge Register -- Read Only -- Offsets 0x200A0, 0x210A0, ...



On PowerPC-based systems, Interrupt Acknowledge is implemented as a read request to a memory-mapped Interrupt Acknowledge register. Please see the *Memory Map* section for the address used.

There is one Interrupt Acknowledge Register per processor. Interrupt Acknowledge:

- returns the interrupt vector corresponding to the highest priority pending interrupt in that processor's Interrupt Request Register (IRR).
- transfers the highest priority pending interrupt from that processor's IRR to that processor's In-Service Register.
- clears the bit in the Interrupt Pending Register corresponding to the highest priority pending interrupt in that processor's IRR. Note: this is effective only for edge triggered interrupts. Level triggered interrupts normally cause the bit in the IPR to be set to 1 every cycle till the device driver's interrupt service routine has cleared the interrupt at the source.

In some implementations, Interrupt Acknowledge also flushes data buffers between the device and system memory.

The 8259 interrupt controller, if used, has its own Interrupt Acknowledge.

Spurious Interrupt Vector Generation

A spurious interrupt (e.g. interrupt is deasserted or current task priority is raised before Interrupt Acknowledge) returns interrupt vector contained in the Spurious Vector Register.

1.2.5 In-Service Registers

There is one In-Service Priority Register per processor. Bits 1-15 correspond to interrupt priorities 1-15.

There is one Interrupt Source In-Service Register per processor. Each Interrupt Source In-Service Register contains one bit for each I/O interrupt source.

Interrupt Acknowledge copies the (highest priority) pending interrupt request from that processor's Interrupt Request Register to that processor's In-Service Registers. The In-Service Priority Register is used to block equal or lower priority interrupts from interrupting this processor till software issues an End-of-Interrupt request. The End-of-Interrupt request resets the highest priority interrupt in the In-Service Priority Register and the corresponding bit in the Interrupt Source In-Service Register.

The In-Service Registers are implementation-dependent and are not program accessible.

1.2.6 End-of-Interrupt Registers

End-of-Interrupt Registers -- Read/Write -- Offsets 0x200B0, 210B0, ...

31	0
EOI Code	

There is one End-of-Interrupt (EOI) Register per processor. Writing a zero to this register signals the end of processing for the highest priority interrupt currently in service by the associated processor. EOI Code values other than 0 are currently undefined and should not be used. Reading this register returns the last value written.

MPIC Implementation Note: When the EOI register is written, the highest priority interrupt in the In-Service Priority Register is reset along with the corresponding bit in the Interrupt Source In-Service register. MPIC-2 ignores the EOI Code on writes (zero is assumed). MPIC-2A REQUIRES the EOI Code be written as ZERO to signal the end of processing for the highest priority interrupt currently in service by the associated processor; EOI Code values other than zero are ignored. Both MPIC-2 and MPIC-2A return zero on reads.

1.3 Global Registers

1.3.1 Feature Reporting Registers

Feature Reporting Register 0 -- Read Only -- Offset 0x01000

31 27	16 13	8	0
Reserved	Num IRQ Sources	Res.	Num CPU	Version ID

Version ID: Version ID for this interrupt Controller. This value reports what level of the specification is supported by this implementation. The values are defined as follows:

Spec. Revision	Version ID
1.0	1
1.2	2

Num CPU: The number of the highest physical CPU supported. For instance, in a 4 processor controller, this value is 3.

Num IRQ: The number of the highest IRQ source supported. For instance, in a system with 16 I/O interrupt sources, this value is 15.

Feature Reporting Register 1 is reserved for future use.

1.3.2 Global Configuration Registers

Global Configuration Register 0 -- Read/Write -- Offset 0x01020

31	29	20	0
R	M	Reserved	Base (not used in PowerPC-based systems)

Base: Base Address Relocation field.This field is NOT used in PowerPC-based systems. Please see the description of the MPIC Base Address in the section entitled Memory Map, below.

M: Cascade Mode. Allows cascading of an external 8259 pair connected to the first interrupt source input pin (0):

0 -- 8259 Pass-Through Mode This mode passes interrupt source 0 directly through to the processor 0 INT pin. MPIC is essentially disabled. This is the default mode after reset.

1 -- 8259 Cascade Mode. In this mode, 8259 interrupts are delivered using the priority and distribution mechanism of MPIC. The Vector/Priority and Destination registers for interrupt source 0 are used to control the priority and delivery mode for all 8259 generated interrupt sources.

R: Reset Controller. Writing a one to this bit forces the controller logic to be reset. This bit is cleared automatically when the reset sequence is complete. While this bit is set, the values of all other registers are undefined.

1.3.3 Vendor Identification Register

Vendor Identification Register -- Read Only -- Offset 0x01080

31 24	16	8	0
Reserved	Stepping	Device ID	Vendor ID

Vendor ID: Specifies the manufacturer of this part. If zero, then this register is not supported and the Device ID and Stepping information are not valid. 0x14 for MPIC-2.
Device ID: Vendor specified identifier for this device. 0x46 for MPIC-2A[1].
Stepping: Stepping (silicon revision) for this device. Initially 0.

1.3.4 Processor Init Register

Processor Init Register -- Read/Write -- Offset 0x01090

31	0
Select Processors 31:0	

Writing to this register causes the INIT lines(s) to one or more processors to be activated. Writing a one to a bit causes the corresponding INIT line to be activated. Writing a zero to a bit causes the corresponding INIT line to be deactivated. (The INIT line(s)s are connected to the System Reset pin(s) on PowerPC processors. The System Reset input on a PowerPC processor is normally edge triggered.)

1.3.5 IPI Vector/Priority Registers

IPI 0 Vector/Priority Registers -- Read/Write -- Offset 0x010A0
IPI 1 Vector/Priority Registers -- Read/Write -- Offset 0x010B0
IPI 2 Vector/Priority Registers -- Read/Write -- Offset 0x010C0
IPI 3 Vector/Priority Registers -- Read/Write -- Offset 0x010D0

31	30	20	16	8	0
M S K	A C T	Reserved	Pri	Reserved for Vector Expansion	Vector

Vector: Interrupt Vector
Pri: Interrupt Priority. 0 is the lowest priority; 15 is the highest priority.
ACT: Activity bit, read-only.
MSK: Mask bit. Setting this bit disables any further interrupts from this source. Reset sets this bit to one.

There are 4 IPI Vector/Priority Registers, one for each IPI Dispatch Register.

[1]The MPIC-2 ASIC returns a Device ID of 0xFF.

1.3.6 Spurious Vector Register

Spurious Vector Register -- Read/Write -- Offset 0x010E0

31	8	0
Reserved	Reserved for Vector Expansion	Vector

Reset sets this register to 0x000000FF.

1.3.7 Global Timer Registers

MPIC-2 contains four global timers (0 through 3) which may be used for system timing or to generate periodic interrupts. The four timers share a Timer Frequency Reporting Register. Each timer also has four registers which are used for configuration and control:

- Current Count Register
- Base Count Register
- Vector/Priority Register
- Destination Register

Timer Frequency Reporting Register -- Read/Write -- Offset 0x010F0

31	0
Timer Frequency	

This register is used to report the frequency (in Hz) of the clock source for the global timers. For MPIC-2, the clock source for the global timers is the MPIC input clock frequency divided by 8.

Following reset, this register contains zero. System initialization code (aka engineering software or firmware) should initialize this register to one-eighth the MPIC clock frequency once the MPIC clock frequency (typically 33MHz) has been determined. A typical value for this register would be 0x003EF148 (4125000 decimal) indicating each timer is updated once every 240ns.

Global Timer 0 Current Count -- Read Only -- Offset 0x01100
Global Timer 1 Current Count -- Read Only -- Offset 0x01140
Global Timer 2 Current Count -- Read Only -- Offset 0x01180
Global Timer 3 Current Count -- Read Only -- Offset 0x011C0

31	0
T	Current Count

This register contains the 31-bit current count and the toggle (T) bit for this timer. The current count is loaded with the base count, and the toggle bit is cleared, whenever the Base Count Register is written AND the Count Inhibit bit in the Base Count Register transitions from 1 to a 0. The timer decrements while the Count Inhibit bit in the Base Count Register is zero. When the timer counts down to zero, an interrupt is generated, the toggle bit is inverted and the current count is reloaded from the base count.

Following reset, counting is disabled and the Current Count Register contains zero.

Global Timer 0 Base Count -- Read/Write -- Offset 0x01110
Global Timer 1 Base Count -- Read/Write -- Offset 0x01150
Global Timer 2 Base Count -- Read/Write -- Offset 0x01190
Global Timer 3 Base Count -- Read/Write -- Offset 0x011D0

31		0
CI	Base Count	

Base Count: This field contains the 31-bit base count for this timer. The current count is loaded with the base count, and the toggle bit in the Current Count Register is cleared, whenever the Base Count Register is written AND the Count Inhibit bit transitions from 1 to a 0. The timer decrements while the Count Inhibit bit is zero. When the timer counts down to zero, an interrupt is generated, the toggle bit in the Current Count Register is inverted and the current count is reloaded from the base count.

CI: Count Inhibit bit. Setting this bit to one inhibits counting for this timer. Setting this bit to zero allows counting to proceed. Reset sets this bit to one (counting inhibited).

Global Timer 0 Vector/Priority Register -- Read/Write -- Offset 0x01120
Global Timer 1 Vector/Priority Register -- Read/Write -- Offset 0x01160
Global Timer 2 Vector/Priority Register -- Read/Write -- Offset 0x011A0
Global Timer 3 Vector/Priority Register -- Read/Write -- Offset 0x011E0

31	30	20	16	8	0
MSK	ACT	Reserved	Pri	Reserved for Vector Expansion	Vector

Vector: Interrupt Vector
Pri: Interrupt Priority. 0 is the lowest priority; 15 is the highest priority.
ACT: Activity bit, read-only.
MSK: Mask bit. Setting this bit disables any further interrupts from this source. Reset sets this bit to one.

Global Timer 0 Destination Register -- Read/Write -- Offset 0x01130
Global Timer 1 Destination Register -- Read/Write -- Offset 0x01170
Global Timer 2 Destination Register -- Read/Write -- Offset 0x011B0
Global Timer 3 Destination Register -- Read/Write -- Offset 0x011F0

31	0
Select Processors 31:0	

This register indicates the destinations(s) for this timer's interrupts. For timer interrupts, only the Directed delivery mode is supported. This register may specify multiple destinations (multicast delivery).

1.4 Memory Map

MPIC Base Address

For systems using the MPIC-2A ASIC, the PCI Base Address Register within the PCI Configuration Space Header is used to locate the MPIC base address on any 256KB boundary within the PCI memory address space[1]. (The MPIC base address is typically located in the upper 32MB of the processor's real address space.)

All registers are 32-bits wide located on 128-bit boundaries.

Complete Interrupt Controller Register Map

Offset (hex)	31 0
0x3F000	*Reserved*
	...
0x23000	Processor 3 Per Processor Registers
0x22000	Processor 2 Per Processor Registers
0x21000	Processor 1 Per Processor Registers
0x20000	Processor 0 Per Processor Registers
	Reserved
0x10000	Interrupt Source Configuration Registers
	Reserved
0x01000	Global Registers
0x00000	*Reserved*

Interrupt Source Configuration Registers

The Interrupt Source Configuration Registers are located at the following offsets from the MPIC Base Address:

Offset (hex)	31 0
	Reserved
0x101F0	Interrupt Source 15 Destination Register
0x101E0	Interrupt Source 15 Vector/Priority Register
	...
0x10010	Interrupt Source 0 Destination Register
0x10000	Interrupt Source 0 Vector/Priority Register

[1]The MPIC base address is located in the PCI I/O address space for the MPIC-2 ASIC.

Global Registers

The Global Registers are located at the following offsets from the MPIC Base Address:

Offset (hex)	31 0
0x01200	*Reserved*
0x011F0	Timer 3 Destination Register
0x011E0	Timer 3 Vector/Priority Register
0x011D0	Timer 3 Base Count Register
0x011C0	Timer 3 Current Count Register
	...
0x01130	Timer 0 Destination Register
0x01120	Timer 0 Vector/Priority Register
0x01110	Timer 0 Base Count Register
0x01100	Timer 0 Current Count Register
0x010F0	Timer Frequency Reporting Register
0x010E0	Spurious Vector Register
0x010D0	IPI 3 Vector/Priority Register
0x010C0	IPI 2 Vector/Priority Register
0x010B0	IPI 1 Vector/Priority Register
0x010A0	IPI 0 Vector/Priority Register
0x01090	Processor Init Register
0x01080	Vendor Identification Register
	Reserved
0x01020	Global Configuration Register 0
	Reserved
0x01000	Feature Reporting Register 0

Per Processor Registers

The per processor registers are located on 4K boundaries within the processors' real address space. The per processor registers for processor 0 are located at offset 0x20000-20FFF from the MPIC Base Address. The per processor registers for processor 1 are located at offset 0x21000-21FFF from the MPIC Base Address. Within each of these 4K regions, the program accessible per processor registers are located at the following offsets:

Offset (hex)	31 0
	Reserved
0x0B0	End-of-Interrupt Register
0x0A0	Interrupt Acknowledge Register
	Reserved
0x080	Current Task Priority Register
0x070	IPI 3 Dispatch Register
0x060	IPI 2 Dispatch Register
0x050	IPI 1 Dispatch Register
0x040	IPI 0 Dispatch Register
	Reserved

To minimize bi-Endian design issues, the program accessible registers within the MPIC should be read and/or written 32 bits at a time. Exception: Only byte 3 of the Interrupt Acknowledge register is used. MPIC allows byte 3 of this register to be read using a single byte memory read request.

8259 Interrupt Vector

PowerPC-based systems typically access the 8259 Interrupt Controller's Interrupt Vector by issuing a 1-byte read to address 0xBFFFFFF0 within the processors' real address space. Planar logic converts this access to 8259 Interrupt Acknowledge cycles.

Accesses by PowerPC processors to registers within the MPIC or the 8259 should be tagged caching-inhibited.

1.5 PCI Configuration Space Header

0x00	Device ID 0x0046[1]	Vendor ID 0x1014
0x04	Status 0x0200	Command 0x0000
0x08	*Reserved*	
0x0C	*Reserved*	
0x10	Base Address Register 0x00000000[1]	
	Reserved	

Bit 1 of the PCI Command Register, when set to a 1, enables MPIC-2A to respond to accesses to the PCI Memory Address space.

1.6 Programming Notes

The following summarizes how an external interrupt is serviced:

- An external interrupt occurs.
- The processor state is saved in the machine status save/restore registers. A new value is loaded into the Machine State Register (MSR). The External Interrupt Enable bit in the new MSR (MSR_{EE}) is set to zero. Control is transferred to the O/S external interrupt handler.
- The external interrupt handler calculates the address of the Interrupt Acknowledge register for this processor (e.g. MPIC Base Address + 0x200A0 + (processor ID shifted left 12 bits)).
- The external interrupt handler issues an Interrupt Acknowledge request to read the interrupt vector (for that processor) from the MPIC.
  - If the interrupt vector indicates the interrupt source is the 8259, the interrupt handler issues a second Interrupt Acknowledge request to read the interrupt vector from the 8259. (PowerPC uses a different memory mapped address for the 8259's Interrupt Acknowledge.)
- The interrupt handler saves the processor state and other interrupt-specific information in system memory and quickly (AIX estimates 100 instructions or so) re-enables for external interrupts (the MSR_{EE} bit is set to 1). MPIC blocks interrupts, from interrupt sources with equal or lower priority, till End-of-Interrupt for that interrupt source. Interrupts from higher priority interrupt sources continue to be enabled.
  - If the interrupt source was the 8259, the interrupt handler issues an EOI request to the MPIC. This resets the In-Service bit for the 8259 within the MPIC and allows MPIC to recognize higher priority interrupt requests, if any, from the 8259. If none of the nested interrupt modes of the 8259 are enabled, the interrupt handler issues an EOI request to the 8259 at this time.
- The device driver interrupt service routine(s) associated with this interrupt vector are invoked. (There may be more than 1 device driver interrupt service routine associated with this interrupt vector if the interrupt is shared.)

[1]The MPIC-2 ASIC returns 0xFFFF for the Device ID and 0x00000001 for the Base Address register.

- If the interrupt source was NOT the 8259, the interrupt handler issues an EOI request for this interrupt vector to the MPIC. If the interrupt source was the 8259 and any of the nested interrupt modes of the 8259 are enabled, the interrupt handler issues an EOI request to the 8259.

Interrupt nesting is supported. See the section entitled *Interrupt Priority*.

Normally, interrupts from ISA devices are connected to the 8259 interrupt controller. ISA devices typically rely on the 8259 Interrupt Acknowledge to flush buffers between the ISA device and system memory. If interrupts from ISA devices are directly connected to the MPIC (bypassing the 8259), the device driver interrupt service routine **must** read status from the ISA device to ensure buffers between the device and system memory are flushed.

1.7 Electrical Specifications

Clock Frequency: 33MHz.

- Edge triggered interrupt inputs must remain stable for at least 100ns before and after a transition.

VCC/VDD: 5.0 Volt.
Cells: 22K (estimate).
Power: 300 mw (estimate).

1.8 Interface

The following table describes the interface used for MPIC. Address and data are in little-Endian format. Pins marked with a [2] are reserved (not connected).

Signal Name	Type	Description	Loading
INTIN[15::0]	In	Interrupt Inputs	
AD{31::0}	bidi, t/s	Address/Data	50pf
C/BE#[3::0]	bidi, t/s	Bus Command and Byte Enables	50pf
IDSEL	In	Initialization Device Select	
FRAME#	In	Cycle Frame	
IRDY#	In	Initiator Ready	
TRDY#	out, s/t/s	Target Ready	50pf
DEVSEL#	out, s/t/s	Device Select	50pf
STOP#	out, s/t/s	Stop	50pf
PERR#[2]	out, s/t/s	Parity Error	50pf
SERR#[2]	out, o/d	System Error	50pf
PAR	bidi, t/s	Data Parity	50pf
RST#	In	Reset	
CLK	In	Clock	
MEMACK_[2]	In	Memory Acknowledge	
FLSHREQ_[2]	out, PP	Flush Request	20pf
INT_[3::0]	out, PP	Processor 0 - 3 Interrupt Requests	20pf
INIT_[3::0]	out, PP	Processor 0 - 3 Initialization	20pf

Total: 73 signal I/O plus approximately 24 power I/O. t/s = bi-directional, three-state input/output. s/t/s = sustained three-state input/output. All t/s and s/t/s outputs are PCI compliant. o/d = Open Drain. PP = three-state Push-Pull output (8ma). Non-PCI inputs/outputs use TTL levels.

FLSHREQ_ and MEMACK_ are used to flush buffers in a PCI-to-PCI bridge during an Interrupt Acknowledge request.

1.9 5.0 Volt MPIC-2A ASIC Pinout

Pins marked with a [1] (X86-like interface) were used on MPIC-2 but are no longer used on MPIC-2A. Pins marked with a [2] are reserved (not connected). Please see the section entitled *MPIC-2A ASIC Application Notes*. VCC is 5 Volts. 160 pin, 0.65mm lead pitch PQFP.8/14/95. IBM P/N: MPIC-2A: 39H9930.

Pin#	Function
1	GND
2	INTIN(8)
3	
4	
5	
6	
7	
8	
9	
10	GND
11	A(17)[1]
12	A(16)[1]
13	A(13)[1]
14	A(12)[1]
15	
16	
17	
18	A(8)[1]
19	GND
20	VCC
21	A(7)[1]
22	A(6)[1]
23	A(5)[1]
24	A(4)[1]
25	TS_[1]
26	TT1[1]
27	
28	
29	GND
30	
31	
32	
33	
34	FLSHREQ_[2]
35	MEMACK_[2]
36	INTIN(7)
37	INTIN(6)
38	
39	GND
40	

Pin#	Function
41	VCC
42	TIE-DOWN
43	CLK
44	INTIN(5)
45	INTIN(4)
46	INTIN(3)
47	INTIN(2)
48	INTIN(1)
49	INTIN(0)
50	GND
51	GND
52	
53	
54	TIE-UP
55	
56	
57	TIE-UP
58	TIE-UP
59	
60	VCC
61	GND
62	
63	
64	RST#
65	
66	GND
67	
68	AD(31)
69	AD(30)
70	GND
71	AD(29)
72	AD(28)
73	AD(27)
74	AD(26)
75	AD(25)
76	AD(24)
77	C/BE#(3)
78	IDSEL
79	GND
80	

Pin#	Function
81	VCC
82	
83	AD(23)
84	AD(22)
85	AD(21)
86	AD(20)
87	AD(19)
88	AD(18)
89	AD(17)
90	AD(16)
91	GND
92	C/BE#(2)
93	
94	FRAME#
95	IRDY#
96	TRDY#
97	DEVSEL#
98	STOP#
99	GND
100	VCC
101	GND
102	
103	PERR#[2]
104	SERR#[2]
105	PAR
106	
107	C/BE#(1)
108	AD(15)
109	AD(14)
110	GND
111	AD(13)
112	AD(12)
113	AD(11)
114	AD(10)
115	AD(9)
116	AD(8)
117	
118	
119	
120	VCC

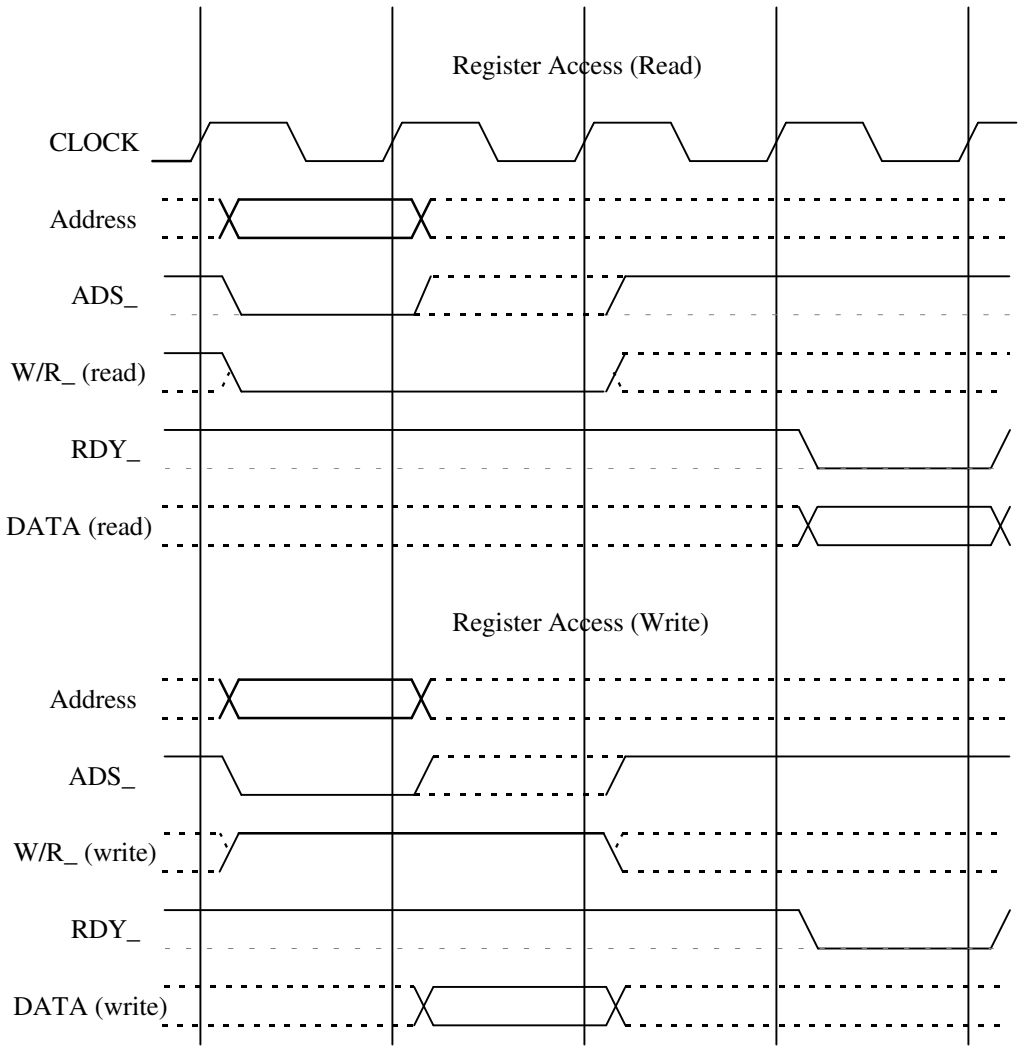
Pin#	Function
121	SCAN_OUT
122	GND
123	C/BE#(0)
124	AD(7)
125	AD(6)
126	AD(5)
127	AD(4)
128	AD(3)
129	AD(2)
130	GND
131	GND
132	AD(0)
133	AD(1)
134	
135	
136	
137	
138	
139	
140	GND
141	GND
142	VCC
143	INT_(3)
144	INT_(2)
145	INT_(1)
146	INT_(0)
147	INIT_(3)
148	INIT_(2)
149	INIT_(1)
150	GND
151	GND
152	INIT_(0)
153	INTIN(15)
154	INTIN(14)
155	INTIN(13)
156	INTIN(12)
157	INTIN(11)
158	INTIN(10)
159	INTIN(9)
160	VCC

1.10 MPIC-2A ASIC Application Notes

- The pin labeled ‘TIE-DOWN’ is used for test and should either be connected to ground (preferred) or left unconnected.
- The pins labeled ‘TIE-UP’ are used for test and should either be tied high (connected to VCC through a resistor) (preferred) or left unconnected.
- Unused interrupt inputs should also be tied high. (Interrupt inputs left floating will cause excessive power dissipation.)
- The MPIC-2A ASIC no longer supports the x86-like interface.
- The MPIC-2 ASIC did not implement STOP#.

1.11 Preliminary Timing Diagrams

This timing diagram is for the x86-like interface: TRDY_ is one cycle later for the PCI interface.



2. Architectural Notes

2.1 Task Priority Register

The hardware and software overhead required to update the task priority register synchronously with instruction execution may far outweigh the anticipated benefits of the task priority register. To minimize this overhead, the interrupt controller architecture should allow the task priority register to be updated asynchronously with respect to instruction execution. 'Lower' priority interrupts may continue to occur for an indeterminate number of cycles after the processor has updated the task priority register. If this is not acceptable, the interrupt controller architecture should recommend that, if the task priority register is not implemented within the processor, the task priority register should only be updated when the processor enters or exits an idle state.

Only when the task priority register is integrated within the processor, such that it can be accessed as quickly as the MSR_{EE} bit, for example, should the architecture require the task priority register be updated synchronously with instruction execution.

2.2 Differences between MPIC and the Open PIC Specification

MPIC does **not** implement 'private access' to the per processor registers (considered by some to be a RISC vs CISC issue). 'Private access' means that all processors can use the same real address (e.g. 0xFFC00000) to access their per processor registers. Lack of 'private access' means software must always use the processor ID to calculate the addresses of per processor registers (e.g. 0xFFC20000 + (processor ID shifted left 12 bits)). In addition, MPIC does **not** implement the following:

- The Who Am I Register
- The Base Address Relocation field in the Global Configuration Register. This field does not support PCI configuration nor does it provide sufficient granularity to allow PowerPC-based systems to relocate the Open PIC registers within the preferred upper 32MB of the processor's real address space. (The default base address specified in the Open PIC specification conflicts with ROM used in some PowerPC-based systems.)

MPIC implements the Polarity bit in the Vector/Priority register for the I/O interrupt sources. This bit is required to maintain software compatibility with parts built to version 1.0 of the Open PIC specification. This bit is reserved in version 1.2 of the Open PIC specification.

Except for the items noted above, MPIC is fully compatible with the Open PIC Interrupt Controller specification. We would, however, like to see the following fields/registers made optional (PowerPC processors already have similar function or the function is considered non-essential for PowerPC-based systems):

- Global Timers

END OF DOCUMENT

SABRE - S/A
Synchronous/Asynchronous SRAM Module with TAG
Application Specification
ES#50H7426

Engineering Change Number	Date
E21059	9/95

IPT Top Number	IBM Top number (Int'l)	IBM Top number (ETS)	IBM Microelectronics IS Premium	Density & Access
			IBM14P64724DPA-9	64K x 72 - 9ns
			IBM14P64724DPA-11	64K x 72 - 11ns
			IBM14P13724DPA-9	128K x 72 - 9ns
			IBM14P13724DPA-11	128K x 72 - 11ns
			IBM14P32726GAA-12	32K x 72 - 12ns
			IBM14P64726GAA-12	64K x 72 -12ns
			IBM14P13726BAA-12	128K x 72 - 12ns

TECH APPROVAL: Sid Shah

DATE PROCESSED:

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IBM
ENGINEERING
SPECIFICATION

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Features

- 256KB, 512K and 1MB secondary cache module family with TAG
- Organized as a 32K, 64K or 128K x 72 package on a 5.06” x 1.10”, 182-lead, Dual Read-out DIMM
- Available in both linear (PowerPC™) and interleaved (i486/Pentium™) burst mode and asynchronous SRAMs
- Fast access times: 9, and 11 with S-SRAM or 12ns with A-SRAM
- TAG access time: 10ns
- Low capacitive address, control, clock, and data bus loading
- Dual +3.3V and +5V, +/- 5% power supplies
- 5V-tolerant common data I/O
- Uses Burndy connector P/N ELF178KSC-3Z50 for Synchronous modules.
- P/N ELF182JSC-3Z50 for Asynchronous modules.

Description

The IBM family of 512KB, and 1MB synchronous SRAM modules use IBM’s burstable, high performance 0.5 micron, CMOS Static RAMs that are versatile and can achieve up to 8ns access using pipeline parts. The 512KB and 1MB modules integrate four and eight 64K x 18 burst SRAMs respectively. The burst mode operation of these modules can support either i486/Pentium or PowerPC-based systems. Asynchronous modules of 256KB, 512KB and 1MB are also available. The asynchronous 256KB/512KB module uses 32Kx 8 ASRAMs, while the 1MB uses 128K x 8 ASRAMs .

The module also contains a 16K x 15 cache Tag RAM (IDT71216-10), allowing fast comparison of the twelve stored common I/O Tag bits and current Tag input data. An active Tag MATCH output is generated when these two groups of data are equal for a given address.

In S-SRAM modules, at the rising edge of CLK (CLK0-4), all addresses, data inputs, burst control inputs (SRAM_CNT_EN, SRAM_ADS), and write enables (SRAM_WE) are latched. Equal clock lengths on the modules produce minimum clock skew. Asynchronous inputs include output enable and data outputs (controlled by SRAM_OE). Burst mode operation is accomplished initially with SRAM_ADS being LOW with a valid address during the rising edge of the clock. This latches the starting address of the burst with subsequent burst addresses being generated internally using the address advance pin, SRAM_CNT_EN. Individual write enable pins, SRAM_WE(0-7), allow individual bytes to be written in a given cycle.

All A-SRAM modules are fully static designs eliminating the need for external clocks or strobes. However, the Tag RAM requires a clock (CLK2) for its operation. The output enable (SRAM_OE) feature provides increased system flexibility and eliminate Bus contention problems.

The module is operated with dual +3.3V and +5V power supplies while inputs and outputs are 5V tolerant and LVTTL compatible.

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Connector Pin Assignment

GND	1	92	GND
PD0	2	93	PD1
PD2	3	94	PD3
DH30	4	95	DH31
DH28	5	96	DH29
DH26	6	97	DH27
DH24	7	98	DH25
VCC3.3	8	99	VCC3.3
DP3	9	100	SRAM_WE3
DH22	10	101	DH23
DH20	11	102	DH21
DH19	12	103	DH18
GND	13	104	GND
DH17	14	105	DH16
DP2	15	106	SRAM_WE2
DH15	16	107	DH14
DH12	17	108	DH13
VCC5	18	109	VCC5
DH11	19	110	DH10
DH9	20	111	DH8
DP1	21	112	SRAM_WE1
DH7	22	113	DH6
VCC3.3	23	114	VCC3.3
DH5	24	115	DH4
DH3	25	116	GND
DH2	26	117*	CLK0
DH0	27	118	GND
DP	28	119	DH1
GND	29	120	SRAM_WE0
CLK1	30*	121	DL31
GND	31	122	DL30
DL28	32	123	GND
DL26	33	124	DL29
DL24	34	125	DL27
DP7	35	126	DL25
VCC5	36	127	VCC5
DL22	37	128	SRAM_WE7
DL20	38	129	DL23
DL18	39	130	DL21
DL16	40	131	DL19
GND	41	132	GND
DP6	42	133	DL17
DL14	43	134	SRAM_WE6
DL12	44	135	DL15
DL11	45	136	DL13
GND	46	137	GND
DL9	47	138	DL10
DP5	48	139	DL8
DL7	49	140	SRAM_WE5
DL4	50	141	DL6
VCC3.3	51	142	VCC3.3
DL3	52	143	DL5
DL1	53	144	DL2
DL0	54	145	GND
GND	55	146*	CLK3
CLK2, (TAG)	56	147	GND
GND	57	148*	CLK4
DP4	58	149	GND
SRAM_OE0	59	150	SRAM_WE4
SRAM_OE1	60	151	SRAM_ALE
VCC3.3	61	152	VCC3.3
ADDR0_A	62	153	ADDR1_A
ADDR0_B	63	154	ADDR1_B
SRAM_ADS0	64*	155*	SRAM_CNT_EN0
SRAM_ADS1	65*	156*	SRAM_CNT_EN1
VCC5	66**	157**	VCC5
VCC5	67**	158**	VCC5
A28	68	159	A27
A26	69	160	A24
A25	70	161	A22
A23	71	162	A20
GND	72	163	GND
A21	73	164	A18
A19	74	165	A16
A17	75	166	A15
A13	76	167	A14
VCC3.3	77	168	VCC3.3
A12	78	169	A10
A11	79	170	A8
A9	80	171	A6
GND	81	172	GND
A7	82	173	A4
A5	83	174	A2
A3	84	175	A1
A0	85	176	RESERVED
VCC5	86	177	VCC5
TAG_CLR	87	178	TAG_VALID
TAG_MATCH	88	179	TAG_WE
TAG_OE	89	180	STANDBY
DIRTYIN	90	181	DIRTYOUT
GND	91	182	GND

NOTES:

* These pins are no connects for the asynchronous module version

** Synchronous modules do not have pins 66, 67, 157 and 158 (physical cut-out)

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Pin Definition and Description

Signal	I/O	Number of Pins	Description
A0-A28	I	29	Address inputs (MSB:0, LSB:28)
ADDR0	I	2	Least significant address bit when asynchronous SRAMs are used
ADDR1	I	2	Next to least significant address bit when asynchronous SRAMs are used
DH0-DH31	I/O	32	High data bus (MSB:0, LSB:31)
DL0-DL31	I/O	32	Low data bus (MSB:0, LSB:31)
DP0-DP7	I/O	8	Data parity bus (MSB:0, LSB:7)
PD0/IDS_CLK	I	1	Presence detect bits 0 / EEPROM serial clock
PD1/IDS_DATA	I/O	1	Presence detect bits 1 / EEPROM serial data
PD2-PD3	O	2	Presence detect bits 2 and 3
$\overline{\text{SRAM_ADS(0-1)}}$	I	2	SRAM address status control (ADSC) strobes
SRAM_ALE	I	1	SRAM address latch enable
$\overline{\text{SRAM_CNT_EN(0-1)}}$	I	2	SRAM burst advance control (ADV) enables
$\overline{\text{SRAM_OE(0-1)}}$	I	2	SRAM output enables
$\overline{\text{SRAM_WE(0-7)}}$	I	8	SRAM write enables (MSB:0, LSB:7)
$\overline{\text{TAG_CLR}}$	I	1	Tag RAM clear
TAG_MATCH	O	1	Tag RAM match indication
TAG_VALID	I	1	Tag RAM valid bit
$\overline{\text{TAG_WE}}$	I	1	Tag RAM write enable
$\overline{\text{TAG_OE}}$	I	1	Tag RAM output enable
DIRTYIN	I	1	Dirty input bit
DIRTYOUT	O	1	Dirty output bit
STANDBY	I	1	Standby pin
RESERVED		1	Reserved pins
CLK0-CLK4	I	5	Clock inputs: CLK(0,1,3,4) are for SRAMs, CLK2 is for TagRAM For 512KB or less use CLK(0-2) only For 1MB use all the clocks
GND	I	24	Ground.
VCC3.3	I	10	+3.3V power supply
VCC5	I	10	+5V power supply

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Ordering Information

Part Number	Organization	Speed	Leads	Type	Availability
IBM14P64724DPA-9	64K x 72	9 ns Access / 15 ns Cycle	182	PowerPC	Now
IBM14P64724DPA-11	64K x 72	11 ns Access / 15 ns Cycle	182	PowerPC	Now
IBM14P13724DPA-9	128K x 72	9 ns Access / 15 ns Cycle	182	PowerPC	Now
IBM14P13724DPA-11	128K x 72	11 ns Access / 15 ns Cycle	182	PowerPC	Now
IBM14P32726GAA-12	32K x 72	12 ns Access / 15 ns Cycle	182	Async	Now
IBM14P64726GAA-12	64K x 72	12 ns Access / 15 ns Cycle	182	Async	Now
IBM14P13726BAA-12	128K x 72	12 ns Access / 15 ns Cycle	182	Async	Now
IBM14P64722DPA-9	64K x 72	9 ns Access / 15 ns Cycle	182	Pentium	On Request
IBM14P64722DPA-11	64K x 72	11 ns Access / 15 ns Cycle	182	Pentium	On Request
IBM14P13722DPA-9	128K x 72	9 ns Access / 15 ns Cycle	182	Pentium	On Request
IBM14P13722DPA-11	128K x 72	11 ns Access / 15 ns Cycle	182	Pentium	On Request

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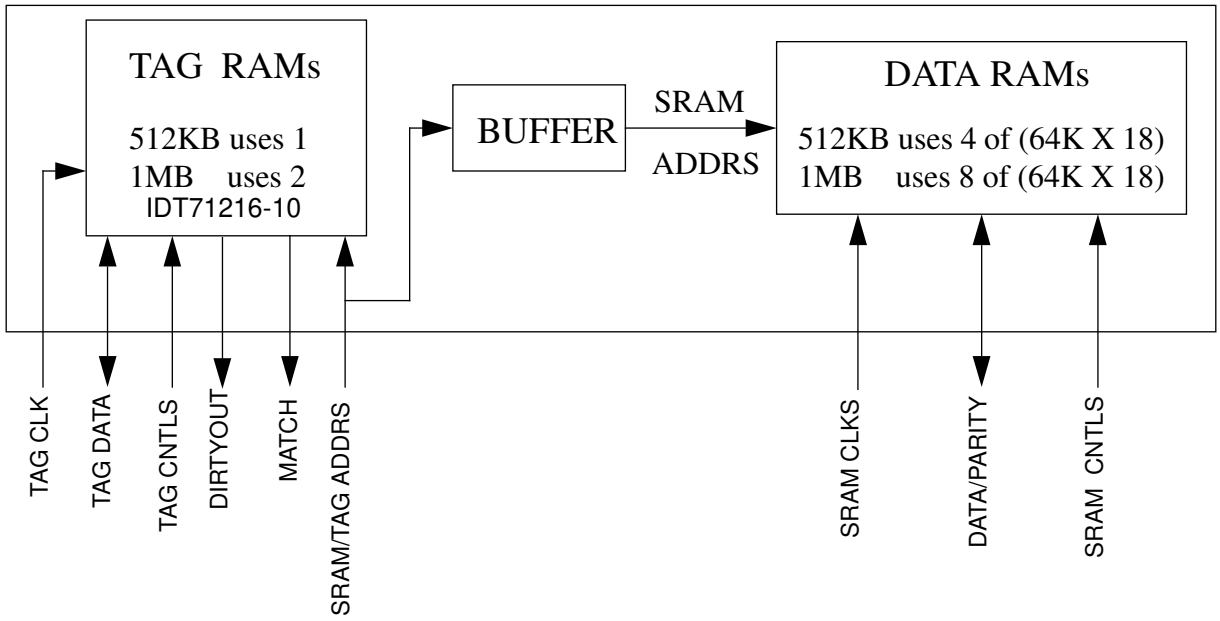
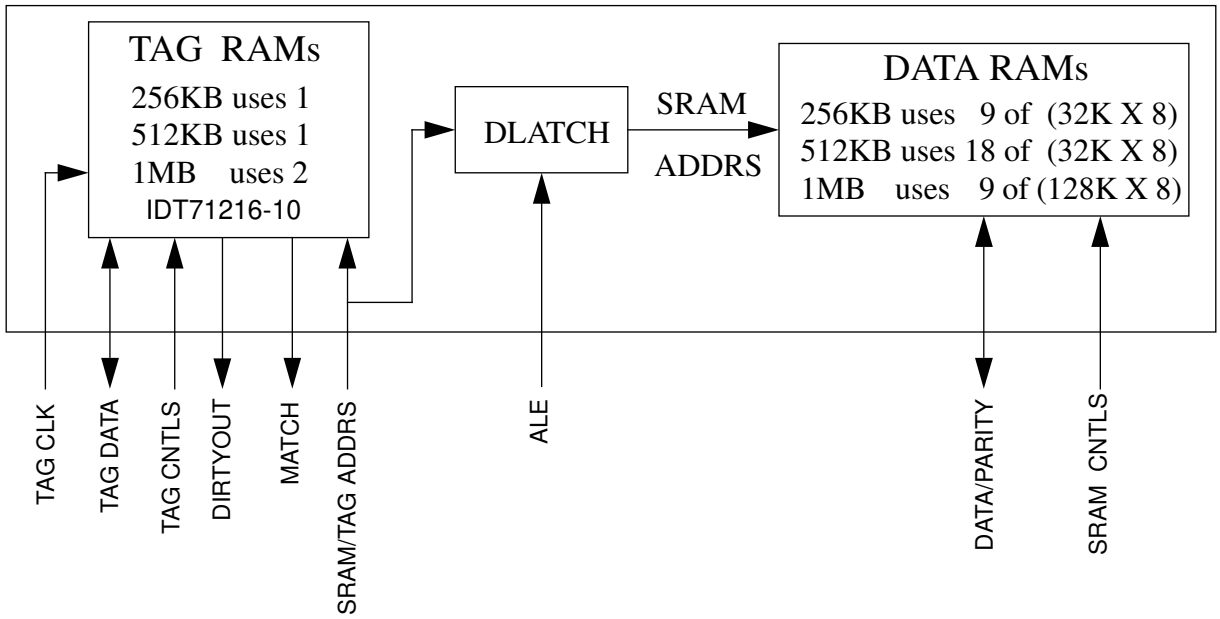
Block Diagram

Synchronous module (512KB & 1MB):



Asynchronous module (256KB, 512KB & 1MB):



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Burst Sequence Truth Table (Interleave Burst) for IBM14P64722DPA, IBM14P13722DPA ONLY

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(0,0)	(1,1)	(1,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(1,0)	(0,1)	(0,0)

Burst Sequence Truth Table (linear burst) for IBM14P64724DPA, IBM14P13724DPA ONLY

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(1,0)	(1,1)	(0,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(0,0)	(0,1)	(1,0)

Presence Detect Table

Part Number	Module Burst Type	Module Size	PD0	PD1	PD2	PD3
IBM14P64724DPA	Linear	512KB	Vcc3.3	GND	Vcc3.3	GND
IBM14P13724DPA	Linear	1MB	GND	Vcc3.3	Vcc3.3	GND
IBM14P32726GAA	Async	256KB	GND	GND	Vcc5	Vcc5
IBM14P64726GAA	Async	512KB	Vcc5	GND	Vcc5	Vcc5
IBM14P13726BAA	Async	1MB	GND	Vcc5	Vcc5	Vcc5
IBM14P64722DPA	Interleaved	512KB	Vcc3.3	GND	Vcc3.3	GND
IBM14P13722DPA	Interleaved	1MB	GND	Vcc3.3	Vcc3.3	GND

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (3.3V)	$V_{cc3.3}$	-0.5 to 4.6	V	1
Power Supply Voltage (5V)	V_{cc5}	-0.5 to 7.0	V	1
Input Voltage		-0.5 to 6.0	V	1,2
Output Voltage		-0.5 to V_{DD}+0.5	V	1,2
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See “Pin Definition and Description” table on page 5 for Input/Output voltage symbols and definitions.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{cc3.3}$	3.135	3.3	3.465	V	1
Supply Voltage	V_{cc5}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.2	—	5.5	V	1,2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1,3

1. All voltages referenced to GND. All $V_{cc3.3}$,V_{cc5} and GND pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)

Capacitance (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, f=1MHz) Maximum values

Parameter	Symbol	Test Condition	256KB	512KB	1MB	Units
Input Capacitance (Address)	C_{IN1}	V_{IN} = 0V	10	10	15	pF
Input Capacitance (Control, $\overline{CE}$, $\overline{OE}$)	C_{IN2}	V_{IN} = 0V	72	72	54	pF
Input Capacitance ($\overline{WE}$, CLK)	C_{IN3}	V_{IN} = 0V	8	8	16	pF
Data I/O Capacitance (DQ0-DQ71)	C_{OUT}	V_{OUT} = 0V	10	10	15	pF

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DC Electrical Characteristics (T_A= 0 to +70°C, $V_{cc3.3}$=3.3V ± 5%, V_{CC5} = 5V ± 5%)

For IBM14P64724DPA and IBM14P13724DPA only					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{cc15}		1220/1370	mA	1
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}		150/300	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}		8	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}		8	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC5} = 5V ± 5%)

For IBM14P64726GAA and IBM14P13726BAA only					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{cc12}		1680/1970	mA	1
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}		290/580	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}		15	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}		15	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

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AC Characteristics (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, Units in nsec)

For IBM14P64724DPA and IBM14P13724DPA only						
Parameter	Symbol	-9		-11		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	15.0	—	15.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	9.0	—	11.0	
Address Status Controller Setup Time	t_{ADSCS}	2.0	—	2.0	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.0	—	2.0	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.0	—	2.0	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.0	—	2.0	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.0	—	2.0	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.0	—	2.0	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.5	1,2
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	1,2
Output Enable to High Z	t_{OHZ}	2.0	5.5	2.0	6.5	1
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	1
Output Enable to Output Valid	t_{OQ}	—	5.0	—	6.0	

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} max is always less than T_{CLZ} min for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from HIZ to new RAM data.

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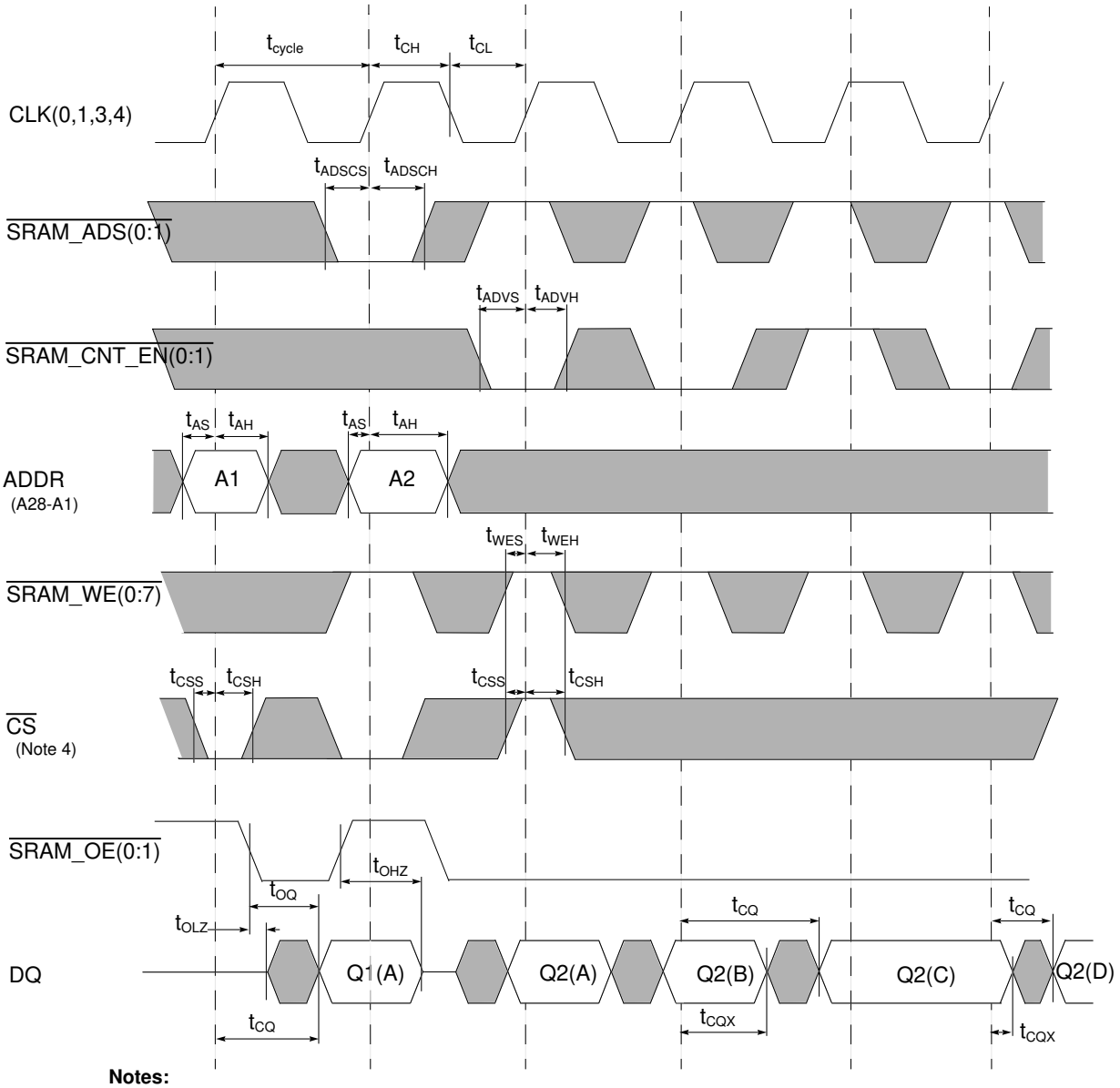
Synchronous SRAM Timing Diagram (Burst Read)

For IBM14P64724DPA and IBM14P13724DPA only



Notes:

1. Q1(A) and Q2(A) refer to output for Address A1 and A2 respectively.
2. Q2(B),Q2(C) and Q2(D) refer to output from subsequent internal burst counter addresses.
3. $\overline{ADSP}$ - Processor address status pin is tied high internal to the module.
4. $\overline{CS}$ - Address A12 serves as chip select for P/N 14P13724; standby pin serves as chip select for P/N 14P64724

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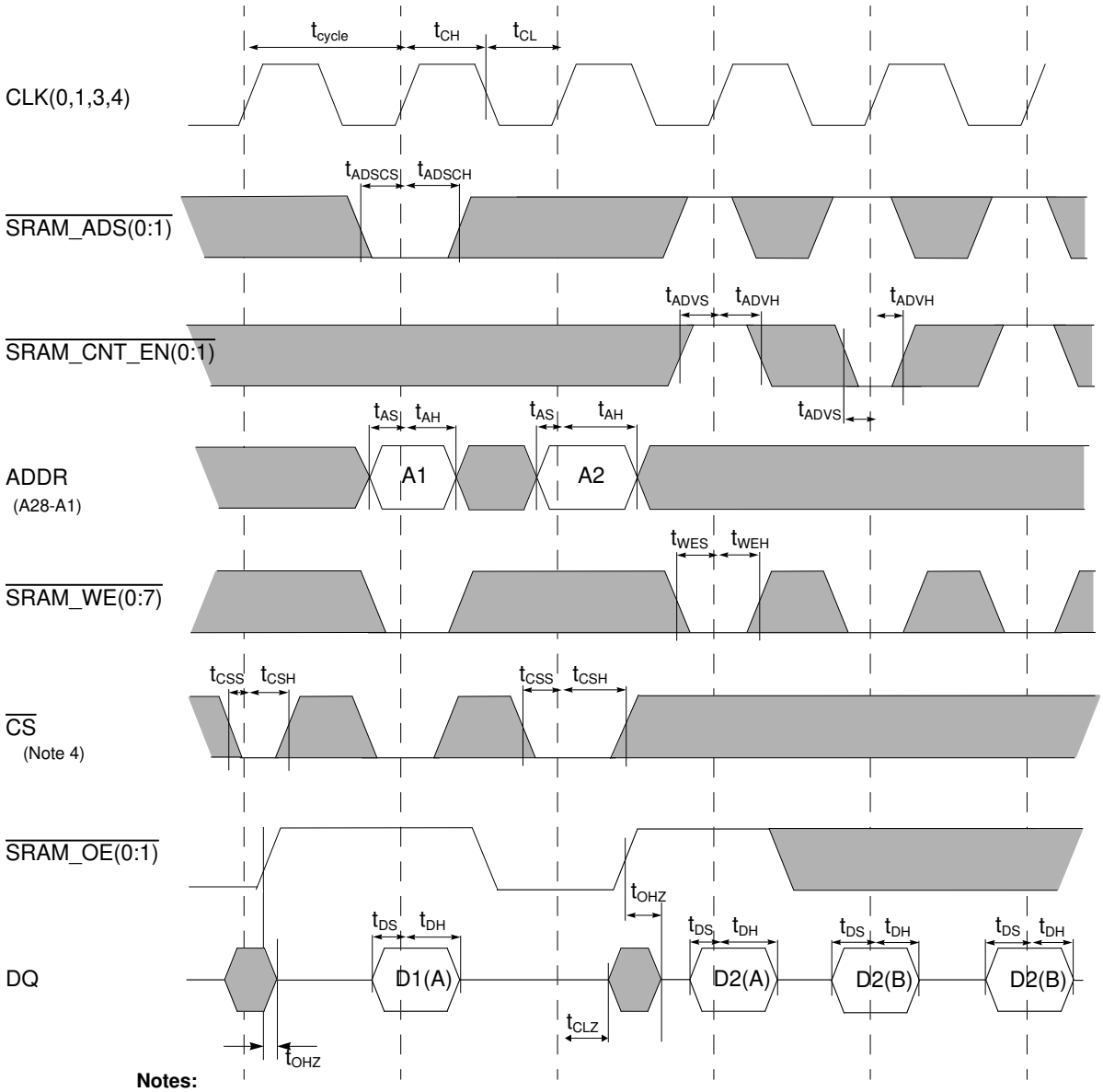
Synchronous SRAM Timing Diagram (Burst Write)

For IBM14P64724DPA and IBM14P13724DPA only



Notes:

1. D1(A) and D2(A) refer to data written to addresses A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. ADSP - Processor address status pin is tied high internal to the module
4. CS - Address A12 serves as chip select for P/N 14P13724; standby pin serves as chip select for P/N 14P64724

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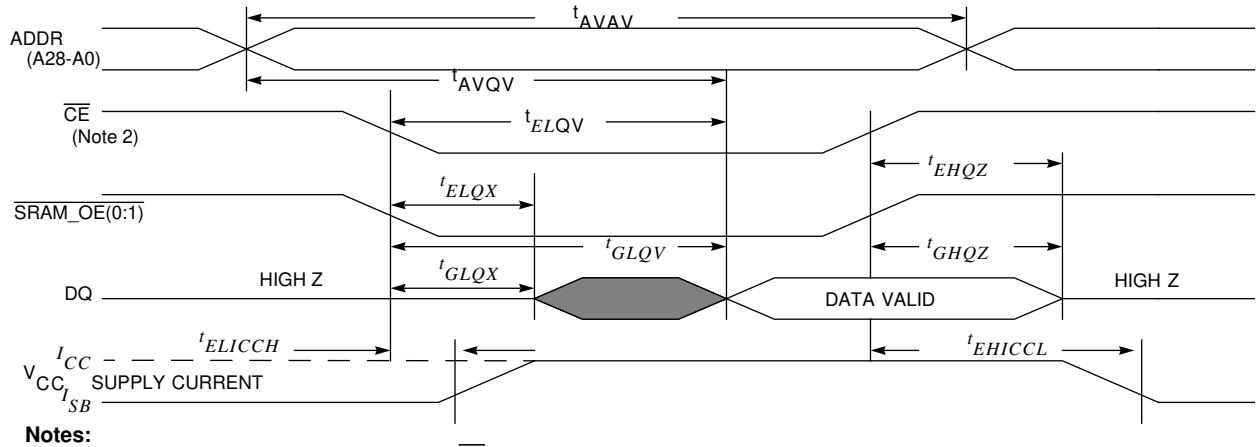
Asynchronous SRAM Timing Diagram (Read)



Notes:
1. Addresses valid prior to or coincident with $\overline{CE}$ going low.
2. $\overline{CE}$ - Address A13 serves as $\overline{CE}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726

Read Cycle

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{AVAV}	12		ns	2
Address Cycle Time	t_{AVQV}		12	ns	
Enable Access Time	t_{ELQV}		12	ns	3
Output Enable Access Time	t_{GLQV}		6	ns	
Output Hold from Address Change	t_{AXQX}	3		ns	4,5,6
Enable Low to Output Active	t_{ELQX}	4		ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	0	7	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0		ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	0	6	ns	4,5,6
Power Up Time	t_{ELICCH}	0		ns	
Power Down Time	t_{EHICCL}		12	ns	

1. $\overline{SRAM_WE(0:7)}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{CE}$ going low
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured +/- 500 mv from steady-state voltage.
6. This parameter is sampled and not 100% tested..

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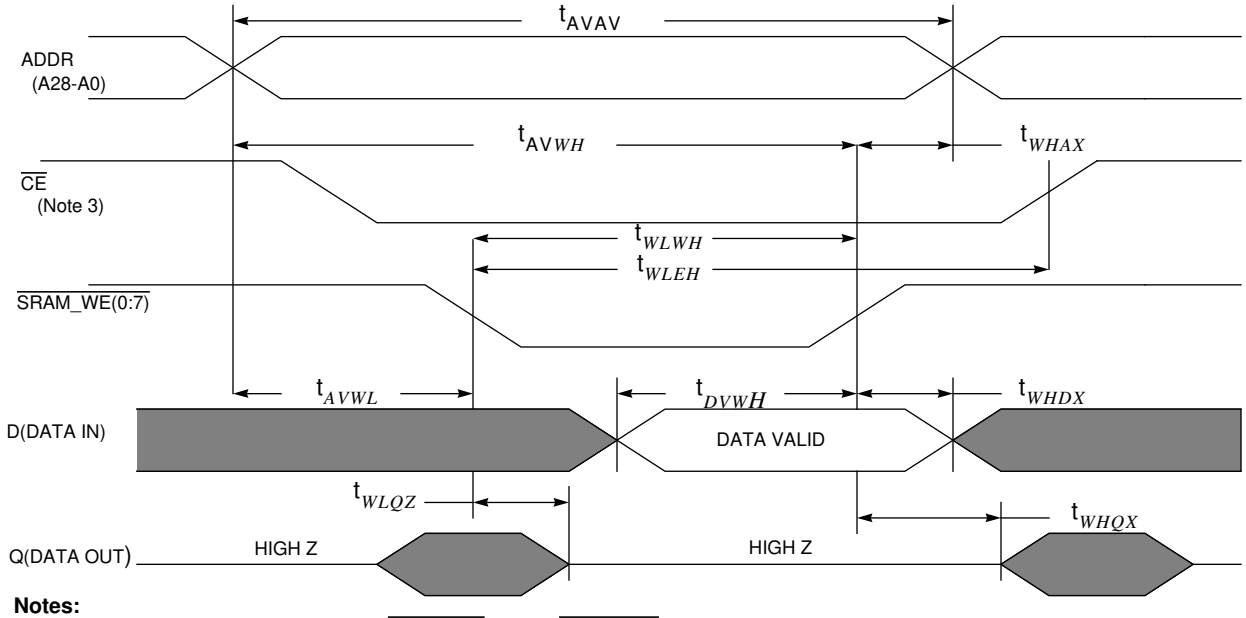
Asynchronous SRAM Timing Diagram (Write Cycle 1)



Notes:
1. A write occurs during the overlap of $\overline{\text{SRAM_OE}}$ low and $\overline{\text{SRAM_WE}}$ low..
2. If $\overline{\text{SRAM_OE}}$ goes low coincident with or after $\overline{\text{SRAM_WE}}$ goes low, the output will remain in a high impedance state.
3. $\overline{\text{CE}}$ - Address A13 serves as $\overline{\text{CE}}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726.

Write Cycle 1 ($\overline{\text{WE}}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	1
Address Setup Time	t_{AVWL}	0		ns	
Address Valid to End of Write	t_{AVWH}	10		ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	10		ns	
Write Pulse Width $\overline{G}$ High	t_{WLWH} t_{WLEH}	9		ns	2
Data Valid to End of Write	t_{DVWH}	6		ns	
Data Hold Time	t_{WHDX}	0		ns	
Write Low to Output High-Z	t_{WLQZ}	0	6	ns	3,4,5
Write High to Output Active	t_{WHQX}	2		ns	3,4,5
Write Recovery Time	t_{WHAX}	0		ns	

1. All timings are referenced from the last valid address to the first transitioning address.
2. If $\overline{\text{SRAM_OE}}$ is larger than or equal to V_{IH}, the output will remain in a high impedance state
3. At any given voltage and temperature , t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
4. Transistion is measured ±500 mv from steady state voltage.
5. This parameter is sampled and not 100% tested.

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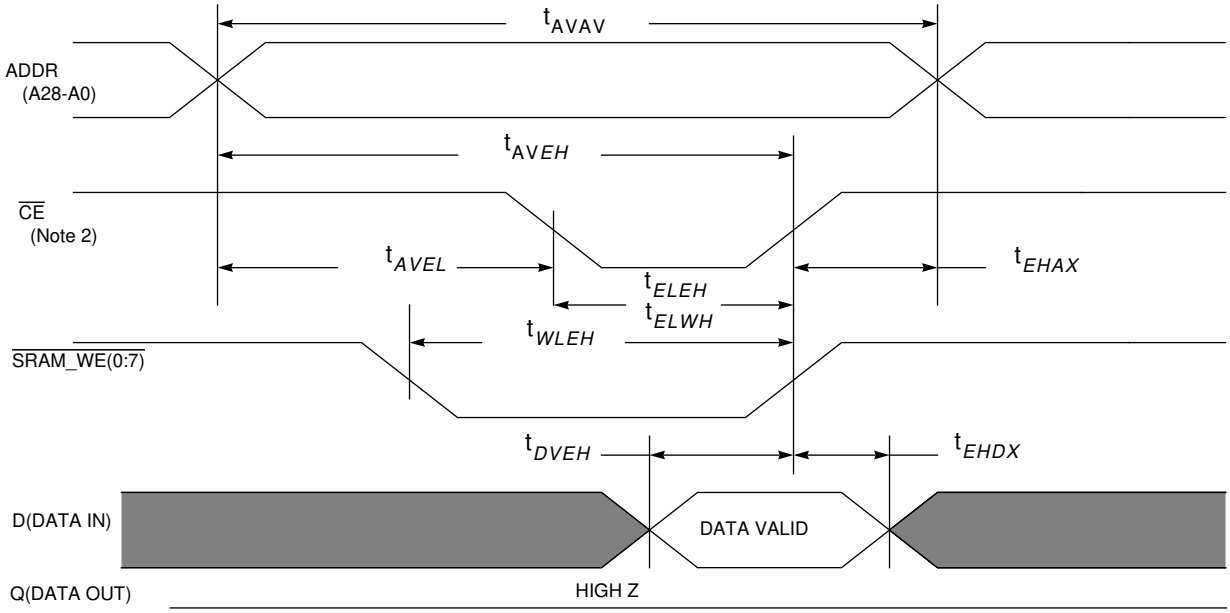
Asynchronous SRAM Timing Diagram (Write Cycle 2)



Notes:
1. A write occurs during the overlap of $\overline{\text{SRAM_OE}}$ low and $\overline{\text{SRAM_WE}}$ low.
2. $\overline{\text{CE}}$ - Address A13 serves as $\overline{\text{CE}}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726.

Write Cycle 2 ($\overline{\text{OE}}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	
Address Setup Time	t_{AVEL}	0		ns	
Address Valid to End of Write	t_{AVEH}	10		ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	9		ns	3,4
Data Valid to End of Write	t_{DVEH}	6		ns	
Data Hold Time	t_{EHDX}	0		ns	
Write Recovery Time	t_{EHAX}	0		ns	

1. A write occurs during the overlap of $\overline{\text{SRAM_OE}}$ low and $\overline{\text{SRAM_WE}}$ low
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{\text{SRAM_OE}}$ goes low coincident with or after $\overline{\text{SRAM_WE}}$ goes low, the output will remain in a high impedance state.
4. If $\overline{\text{SRAM_OE}}$ goes high coincident with or before $\overline{\text{SRAM_WE}}$ goes high, the output will remain in a high impedance state.

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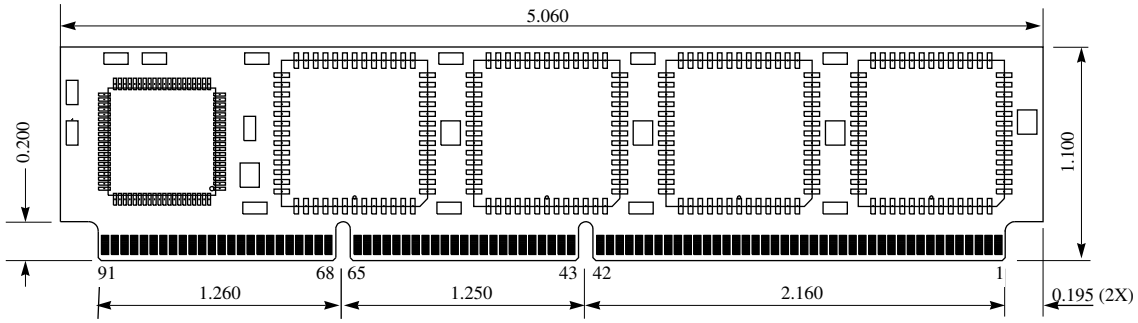
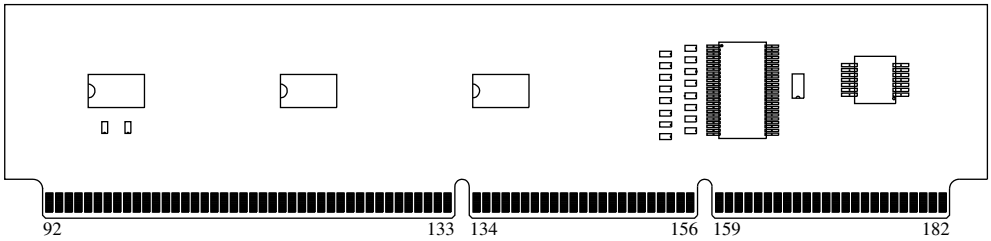
Layout Drawing 512KB (64K x 72), 182-pin Synchronous module

Front view:



Back view:



Uses Burndy connector: P/N ELF178KSC-3Z50

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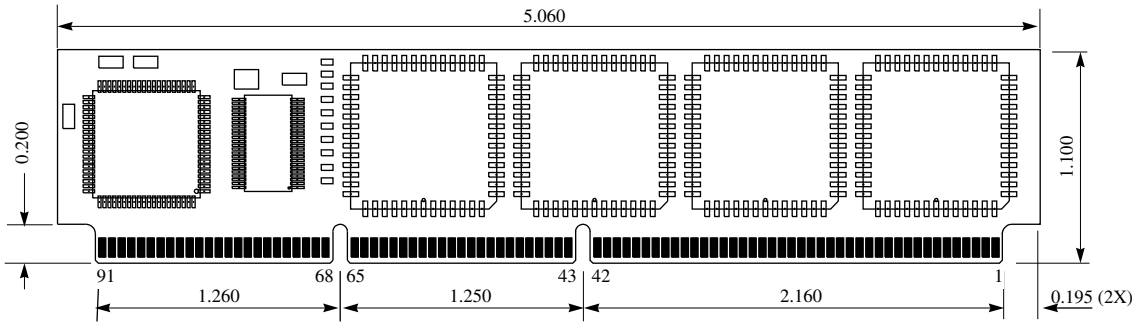
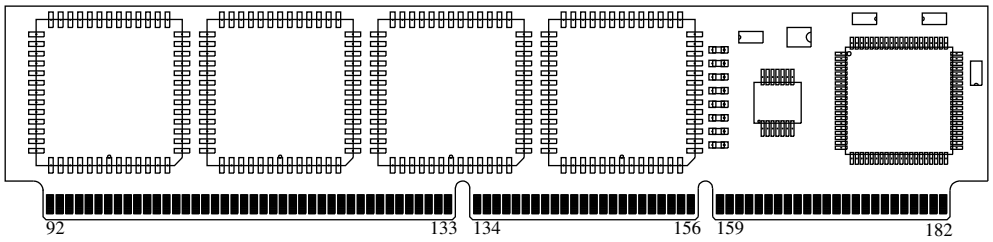
Layout Drawing 1MB (128K x 72), 182-pin Synchronous module

Front view:



Back view:



Uses Burndy connector: P/N ELF178KSC-3Z50

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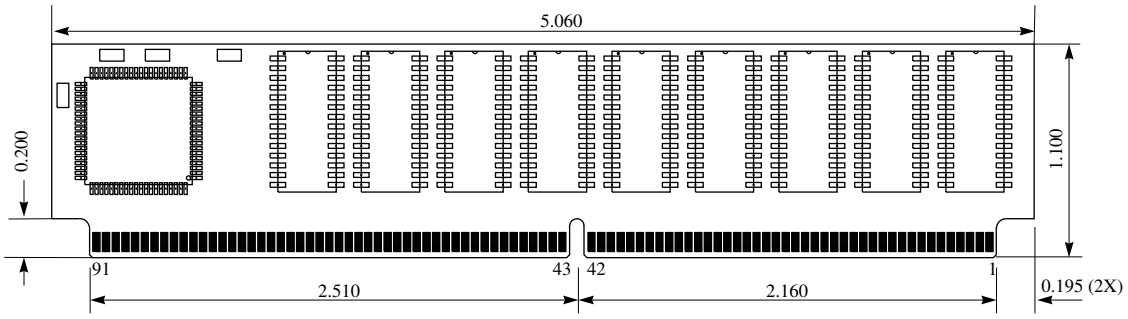
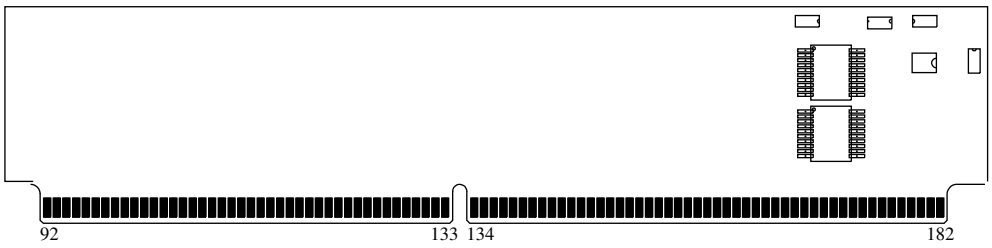
Layout Drawing 256KB (32K x 72), 182-pin Asynchronous module

Front view:



Back view:



Uses Burndy connector: P/N ELF182JSC-3Z50

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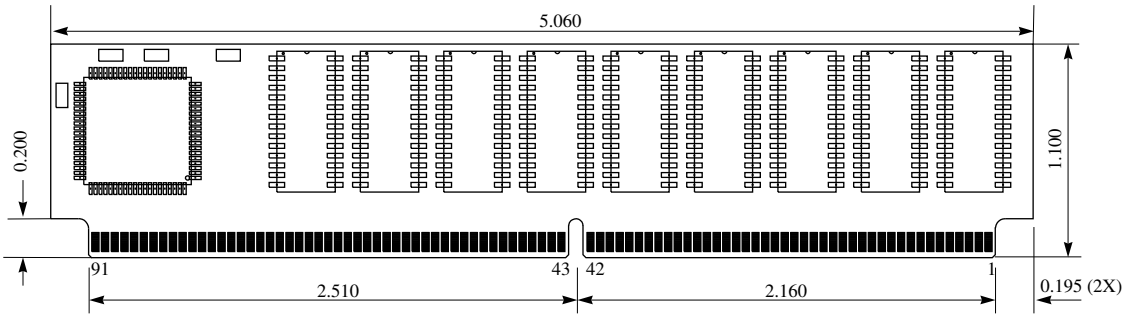
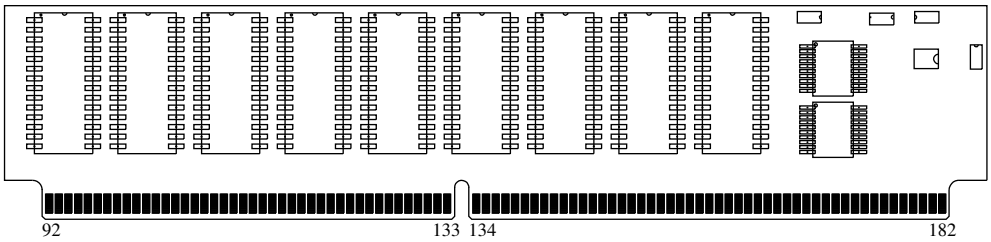
Layout Drawing 512KB (64K x 72), 182-pin Asynchronous module

Front view:



Back view:



Uses Burndy connector: P/N ELF182JSC-3Z50

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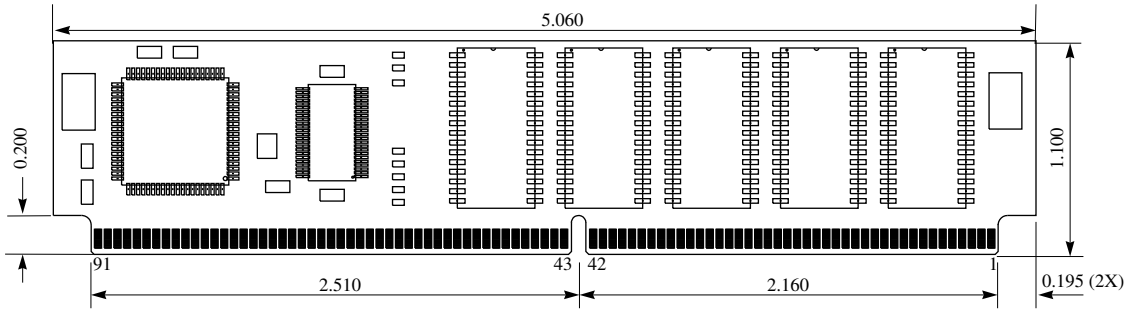
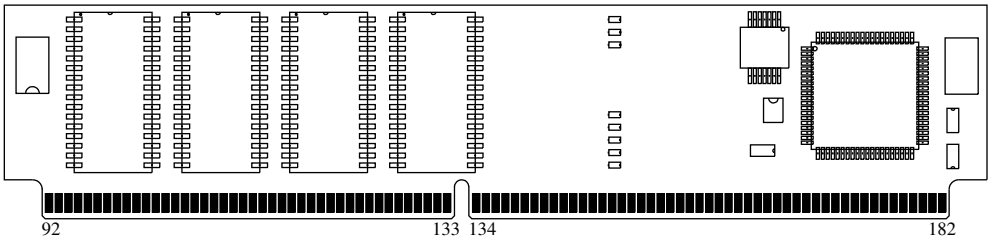
Layout Drawing 1MB (128K x 72), 182-pin Asynchronous module

Front view:



Back view:



Uses Burndy connector: P/N ELF182JSC-3Z50

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Revision Log

Rev	Contents of Modification
9/95	Preliminary Version

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MPR604HSU-02
(IBM Order Number)

MPC604EC/D
(Motorola Order Number)

11/95
REV 1

PowerPC™

Advance Information

PowerPC 604™ RISC Microprocessor Hardware Specifications

The PowerPC 604 microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the 604. For information about the functionality of the 604, refer to the *PowerPC 604 RISC Microprocessor Users Manual.*

This document contains the following topics:

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Section 1.2, “Electrical and Thermal Characteristics”	2
Section 1.3, “AC Electrical Characteristics”	3
Section 1.4, “PowerPC 604 Microprocessor Pin Assignments”	11
Section 1.5, “PowerPC 604 Microprocessor Pinout Listings”	14
Section 1.6, “PowerPC 604 Microprocessor Package Description”	19
Section 1.7, “System Design Information”	25
Section 1.8, “Thermal Management Information”	27
Section 1.9, “Ordering Information”	30

In this document, the term “604” is used as an abbreviation for the phrase “PowerPC 604 microprocessor.” The PowerPC 604 microprocessors are available from IBM as PPC604 and from Motorola as MPC604.

PRELIMINARY

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IBM®

MOTOROLA

1.1 General Parameters

Technology	0.5 µm CMOS, four-layer metal
Chip size	196 mm^2, 12.4 mm x 15.8 mm
Packages	Surface-mount 304-pin C4-CQFP
	Surface-mount 255-lead ceramic ball grid array (BGA)
Voltage	3.3 V ± 5%
Maximum power dissipation	24 W @ 133 MHz
	19 W @ 100 MHz

1.2 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 604. The following specifications are preliminary and subject to change without notice. For the most recent specifications, contact your local Motorola or IBM sales office.

1.2.1 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum rating and thermal characteristics for the 604.

Table 1. PowerPC 604 Microprocessor Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	V_{dd}	–0.3 to 3.6	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional operating conditions are given in DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** Input voltage must not be greater than the supply voltage by more than 2.5 V during power-on reset.

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Table 2. PowerPC 604 Microprocessor Thermal Characteristics

Characteristic	Symbol	Value	Rating
C4-CQFP package thermal resistance, junction-to-case	θ_{JC}	0.03	°C/W
BGA package thermal resistance, junction-to-case	θ_{JC}	0.03	°C/W

Notes:

1. For the BGA package, the θ_{JC} measurement is made from die junction to the back of the bare silicon die.
2. The junction temperature of the chip is a function of several parameters including θ_{JC}. Please refer to Section 1.8, “Thermal Management Information,” for additional details.

Table 3 provides the DC electrical characteristics for the 604.

Table 3. PowerPC 604 Microprocessor DC Electrical Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_j ≤ 105 °C, Input capacitance = 10 pF maximum

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	0	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	0	0.4	V
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 9 mA	V_{OL}	—	0.4	V

Table 4 provides the power dissipation numbers for the 604.

Table 4. PowerPC 604 Microprocessor Power Dissipation

	Processor Core Frequency			Unit	Notes
	100 MHz	120 MHz	133 MHz		
Full-On Mode					1
Typical	14.5	17.0	18.5	W	2
Maximum	19.0	22.5	24.0	W	3

Notes:
1. Power measured does not include power dissipated in output drivers.
2. Typical power is an average value measured at 3.3 V in a system executing typical applications and benchmark sequences. Typical power numbers should be used in planning for proper thermal management.
3. Maximum power is measured at 3.3 V using a worst case instruction mix. These values should be used for power supply design.

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1.3 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 604. These specifications are for parts that operate at processor core frequencies of 100, 120, and 133 MHz. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG0–PLL_CFG3 pins. All timings are specified respective to the SYSCLK.

1.3.1 Clock AC Specifications

Table 5 provides the clock AC timing specifications as defined in Figure 1.

Table 5. PowerPC 604 Microprocessor Clock AC Timing Specifications

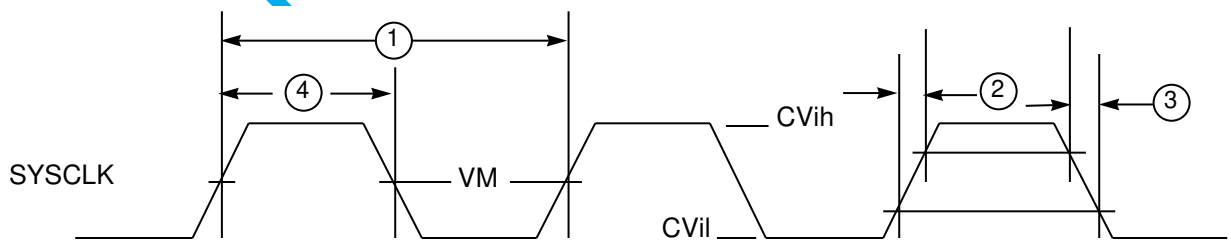
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
	Frequency of operation	50	100.0	60.0	120.0	66.67	133.3	MHz	1
	Frequency of VCO	180	360	180	360	180	360	MHz	2
	SYSCLK frequency	16.67	66.67	20.0	66.67	22.2	66.67	MHz	3
1	SYSCLK cycle time	15.0	60.0	15.0	50.0	15.0	45.0	ns	
2,3	SYSCLK rise and fall time	1.0	2.0	1.0	2.0	1.0	2.0	ns	4
4	SYSCLK duty cycle measured at 1.4 V	40	60	40	60	40	60	%	
5	SYSCLK jitter	—	±150	—	±150	—	±150	ps	5
6	Internal PLL relock time	—	100	—	100	—	100	µs	6, 7

Notes:
1. Times shown in specifications are only valid for the range of processor core frequencies specified.
2. **Caution**: The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
3. AC timing specifications are tested up to the maximum SYSCLK (bus) frequency shown in Table 5. However, it is theoretically possible to attain higher SYSCLK frequencies if allowed for by system design.
4. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
5. This number refers to cycle-to-cycle jitter.
6. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
7. Relock timing is guaranteed by design and is not tested.

PRELIMINARY

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.3.2 Input AC Specifications

Table 6 provides the input AC timing specifications for the 604 as defined in Figure 2.

Table 6. PowerPC 604 Microprocessor Input AC Timing Specifications

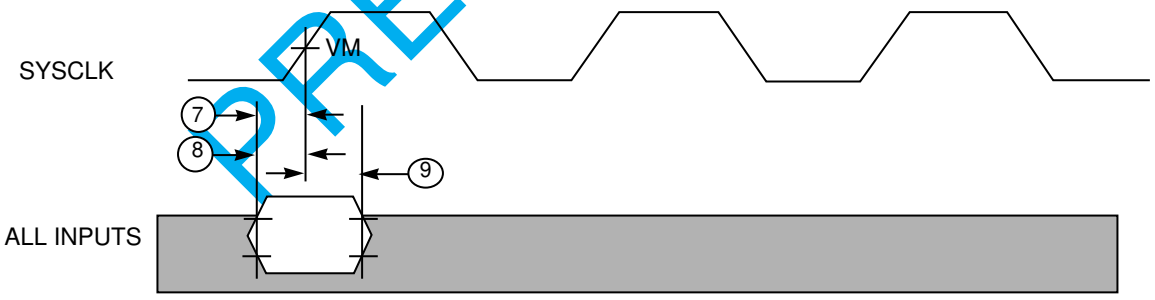
Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
7	$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$,$\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, and $\overline{\text{DBWO}}$ valid to SYSCLK (setup)	5.5	—	5.0	—	5.0		ns	
8	All other inputs valid to SYSCLK (setup)	5.5	—	4.0	—	4.0	—	ns	1
9	SYSCLK to all inputs invalid (hold)	0	—	0	—	0	—	ns	1
10	Mode select input valid to $\overline{\text{HRESET}}$ (input setup for $\overline{\text{DRTRY}}$)	8 * t_{sysclk}	—	8 * t_{sysclk}	—	8 * t_{sysclk}	—	ns	2,3,4,5
11	$\overline{\text{HRESET}}$ to mode select input invalid (input hold for $\overline{\text{DRTRY}}$)	0	—	0	—	0	—	ns	2,3,4,5

Notes:

1. All other input signals include the following signals—all inputs except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{AACK}}$, $\overline{\text{BG}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TA}}$, $\overline{\text{DBG}}$, $\overline{\text{DBB}}$, $\overline{\text{DBWO}}$, $\overline{\text{DBDIS}}$, $\overline{\text{TEA}}$, and JTAG inputs.
2. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
3. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
4. These values are guaranteed by design, and are not tested.
5. Note this is for configuration of the fast-L2 mode. The $\overline{\text{DRTRY}}$ signal must be held negated during fast-L2 mode.

Figure 2 provides the input timing diagram for the 604.



VM = Midpoint Voltage (1.4V)

Figure 2. PowerPC 604 Microprocessor Input Timing Diagram

PRELIMINARY

Figure 3 provides the timing diagram for the fast-L2 mode select input.

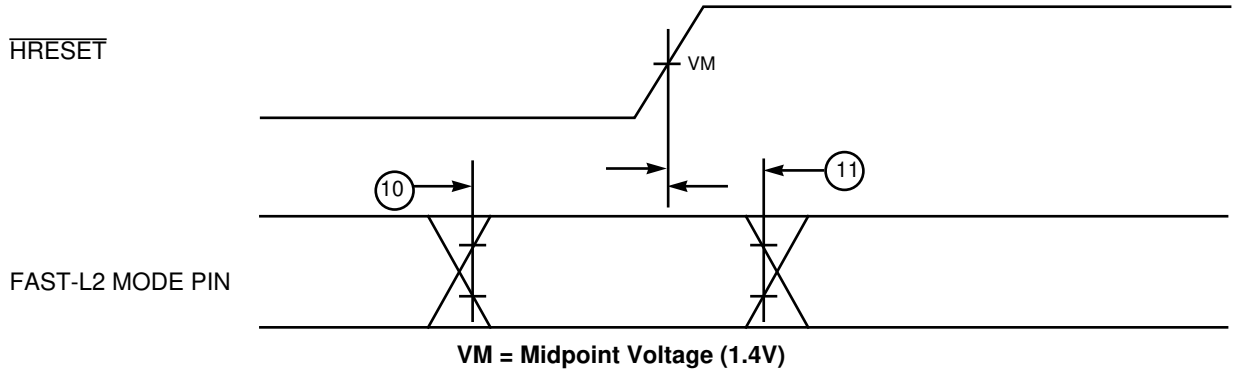


Figure 3. Fast-L2 Mode Select Input Timing Diagram

1.3.3 Output AC Specifications

Table 7 provides the output AC timing specifications for the 604 (shown in Figure 4).

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_j ≤ 105 °C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	0.75	—	0.75	—	0.75	—	ns	1
13a	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, and $\overline{DBB}$ output valid (for 5.5 V to 0.8 V)	—	8.5	—	7.5	—	7.0	ns	2
13b	SYSCLK to $\overline{TS}$, $\overline{XATS}$, $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, and $\overline{DBB}$ output valid (for 3.6 V to 0.8 V)	—	7.5	—	6.5	—	6.0	ns	
14a	SYSCLK to all other signals output valid (for 5.5 V to 0.8 V)	—	8.5	—	7.5	—	7.0	ns	2
14b	SYSCLK to all other signals output valid (for 3.6 V to 0.8 V)	—	7.5	—	6.5	—	6.0	ns	
15	SYSCLK to output invalid (output hold)	1.0	—	1.0	—	1.0	—	ns	
16	SYSCLK to output high impedance (all signals except $\overline{ARTRY}$, $\overline{SHD}$, $\overline{ABB}$, $\overline{DBB}$, $\overline{TS}$, and $\overline{XATS}$)	—	7.0	—	6.5	—	6.0	ns	
17	SYSCLK to output high impedance $\overline{TS}$, $\overline{XATS}$	—	7.0	—	6.5	—	6.0	ns	
18	SYSCLK to $\overline{ABB}$ and $\overline{DBB}$ high impedance after precharge	—	1.0* t_{sysclk}	—	1.0* t_{sysclk}	—	1.0* t_{sysclk}	ns	3
19	SYSCLK to $\overline{ARTRY}$ and $\overline{SHD}$ high impedance before precharge	—	7.0	—	6.5	—	6.0	ns	

PRELIMINARY

Table 7. PowerPC 604 Microprocessor Output AC Timing Specifications (Continued)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_j ≤ 105 °C

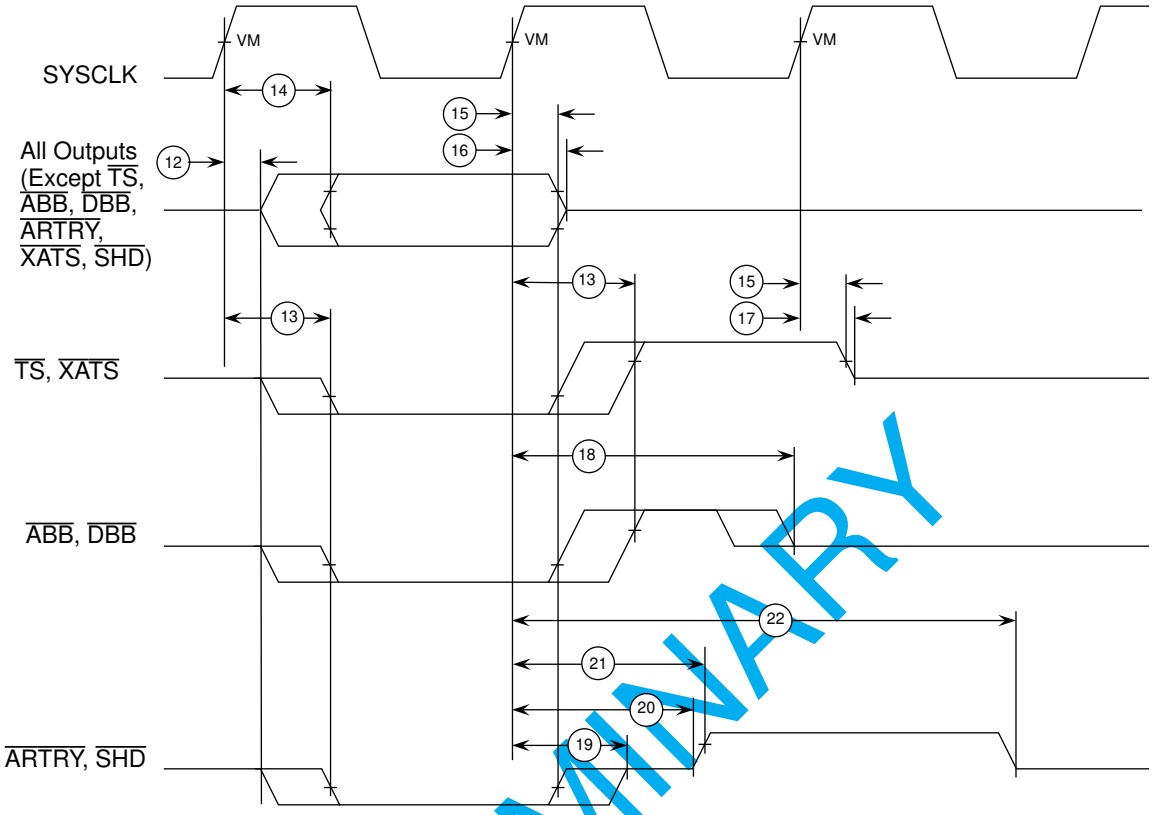
Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
20	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ precharge enable	—	0.5* t_{sysclk} + 0.75	—	0.5* t_{sysclk} + 0.75	—	0.5* t_{sysclk} + 0.75	ns	3
21	Maximum delay to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ precharge	—	1.5* t_{sysclk}	—	1.5* t_{sysclk}	—	1.5* t_{sysclk}	ns	3
22	SYSCLK to $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ high impedance after precharge	—	2.0* t_{sysclk}	—	2.0* t_{sysclk}	—	2.0* t_{sysclk}	ns	3
	Rise time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Rise time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Fall time ($\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4
	Fall time (all signals except $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{TS}}$, and $\overline{\text{XATS}}$)	1.0		1.0		1.0		ns	4

Notes:

1. These values are guaranteed by design, and are not tested.
2. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from 3.6 V to 0.8 V (5-V CMOS levels instead of 3.3-V CMOS levels).
3. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). When the unit is given as t_{sysclk} the numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
4. These specifications are nominal values.

PRELIMINARY

Figure 4 provides the output timing diagram for the 604.



Notes: VM = Midpoint voltage (1.4 V)
All output specifications are measured from 0.8 V or 2.0 V of the signal in question to the 1.4 V of the rising edge of the input SYSCLK.

Figure 4. PowerPC 604 Microprocessor Output Timing Diagram

PRELIMINARY

The output specifications of the 604 for both driving high and driving low depend on the capacitive loading on each output and the drive capability enabled for that output. Additionally, the timing specifications for outputs driving low also depend on the voltage swing required to drive to 0.8 V (either 5.5 V to 0.8 V or 3.6 V to 0.8 V). Table 7 provides the output AC timing specifications for a 50 pF load. In order to derive the actual timing specifications for a given set of conditions, it is recommended that IBIS simulation models be used. Contact the local Motorola or IBM sales office for information on the availability of these models.

1.3.4 JTAG AC Timing Specifications

Table 8 provides the JTAG AC timing specifications.

Table 8. JTAG AC Timing Specifications (Independent of SYSCLK)

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.5 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	2
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	0	—	ns	
7	Boundary-scan input data hold time	27	—	ns	
8	TCK to output data valid	4	35	ns	
9	TCK to output high impedance	3	24	ns	
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	1
13	TCK to TDO high impedance	3	15	ns	1

Notes:
1. Load capacitance = 50 pF.
2. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes.

Figure 5 provides the JTAG clock input timing diagram.

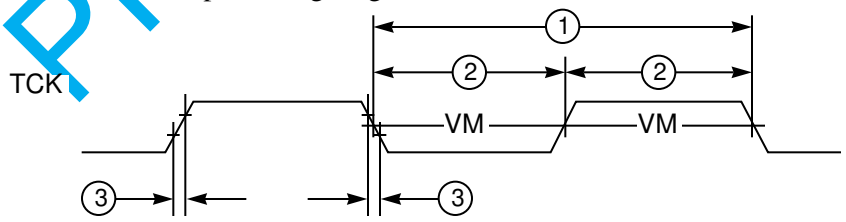


Figure 5. Clock Input Timing Diagram

PRELIMINARY

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

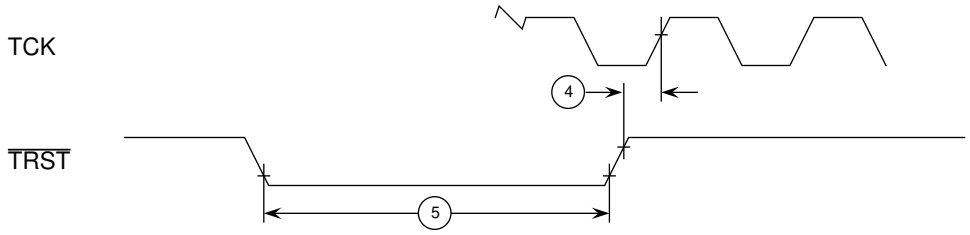


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

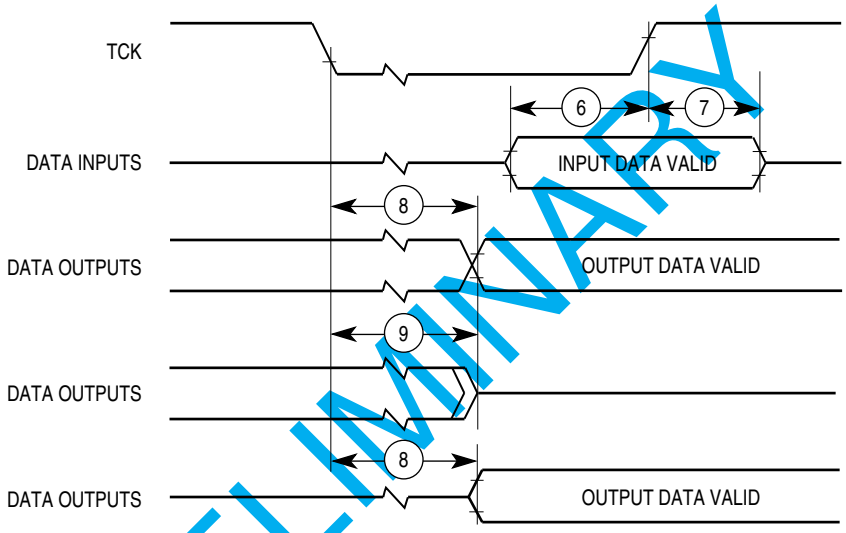


Figure 7. Boundary-Scan Timing Diagram

PRELIMINARY

Figure 8 provides the test access port timing diagram.

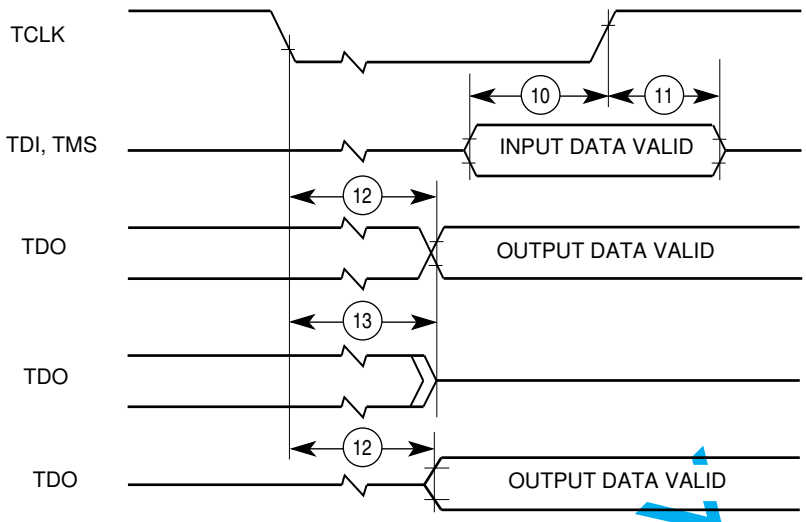


Figure 8. Test Access Port Timing Diagram

1.4 PowerPC 604 Microprocessor Pin Assignments

The following sections contain the pinout diagrams for the 604. Note that the 604 is currently offered in two packages. Motorola and IBM both offer a C4 Ceramic Quad Flat Pack (C4-CQFP), and a Ball Grid Array (BGA) package. Both IBM and Motorola C4-CQFP and BGA packages have identical pinouts.

PRELIMINARY

1.4.1 Pinout Diagram for the C4-CQFP Package

Figure 9 contains the pinout diagram of the C4-CQFP package for the 604.

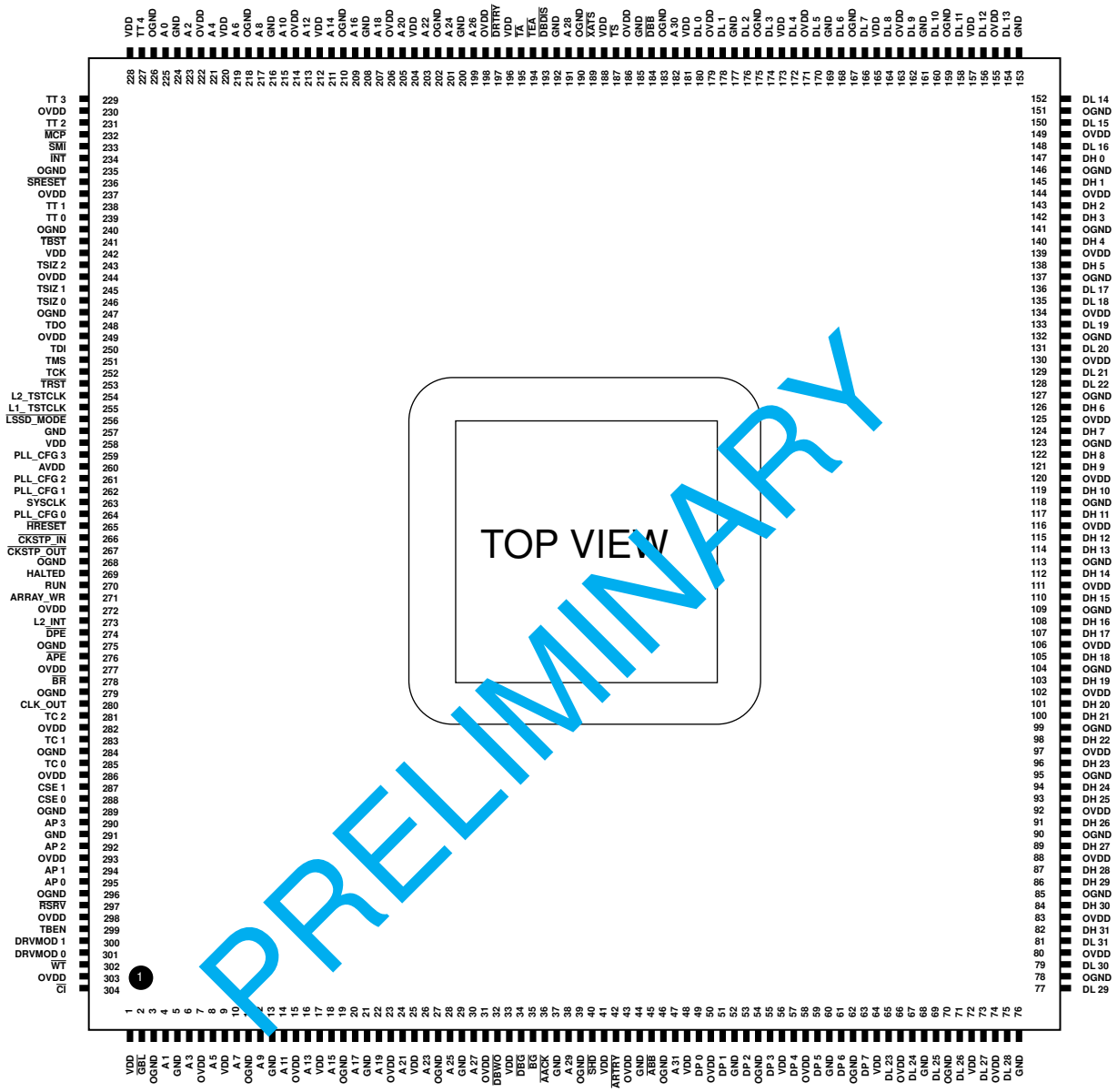
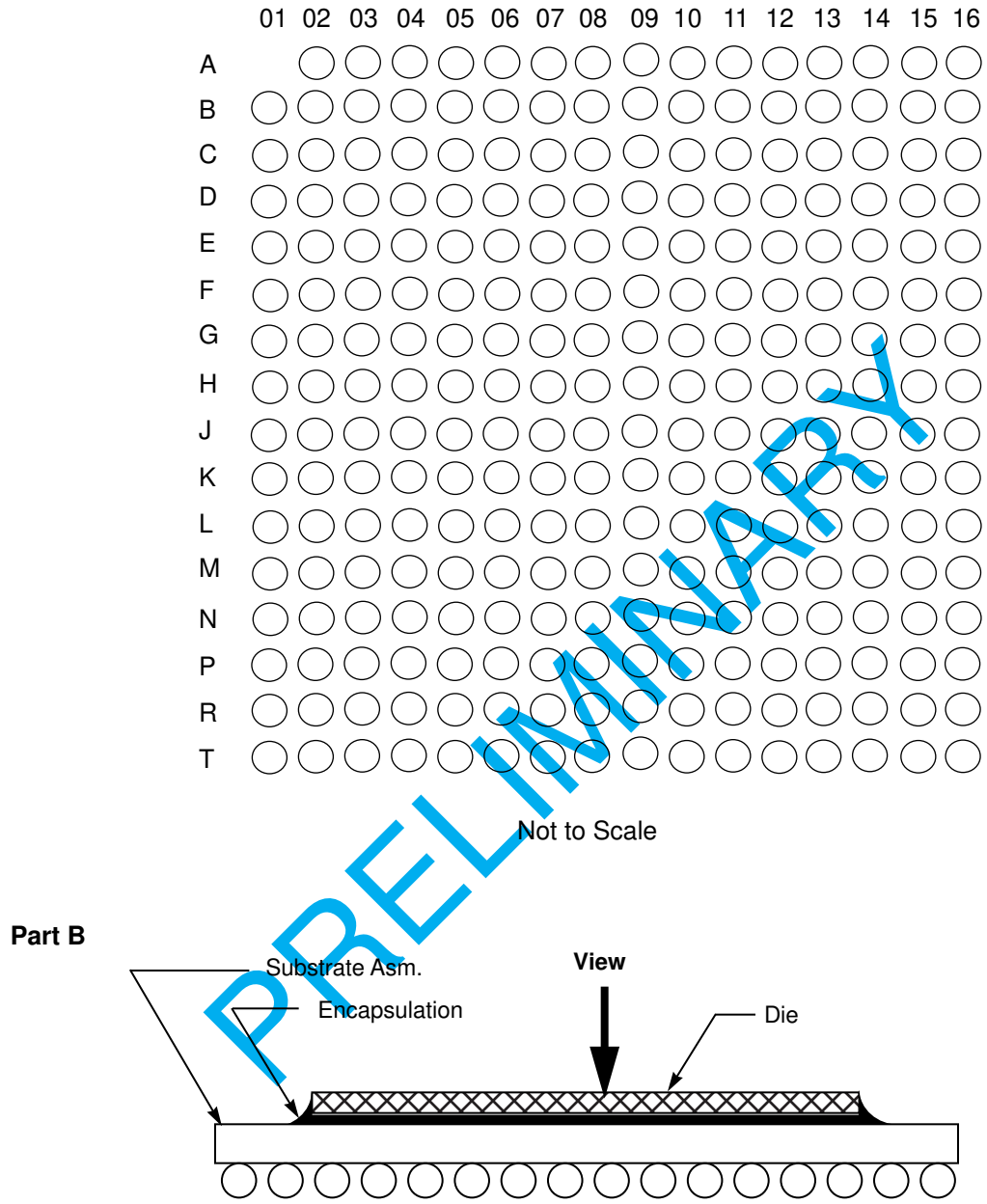


Figure 9. Pinout Diagram of the C4-CQFP Package

1.4.2 Pinout Diagram for the BGA Package

Figure 10 (in part A) shows the pinout of the BGA package as viewed from the top surface. Part B shows the side profile of the BGA package to indicate the direction of the top surface view.



PRELIMINARY

Figure 10. Pinout of the BGA Package as Viewed from the Top Surface

1.5 PowerPC 604 Microprocessor Pinout Listings

The following sections contain the pinout listings for the 604 C4-CQFP and BGA packages.

1.5.1 Pinout Listing for the C4-CQFP Package

Table 9 provides the pinout listing for the 604 C4-CQFP package.

Table 9. Pinout Listing for the C4-CQFP Package

Signal Name	Pin Number	Active	I/O
A0–A31	225, 4, 223, 6, 221, 8, 219, 10, 217, 12, 215, 14, 213, 16, 211, 18, 209, 20, 207, 22, 205, 24, 203, 26, 201, 28, 199, 30, 191, 38, 182, 47	High	I/O
$\overline{\text{AACK}}$	36	Low	Input
$\overline{\text{ABB}}$	45	Low	I/O
AP0–AP3	295, 294, 292, 290	High	I/O
$\overline{\text{APE}}$	276	Low	Output
ARRAY_WR[1]	271	Low	Input
$\overline{\text{ARTRY}}$	42	Low	I/O
AVDD	260	—	—
$\overline{\text{BG}}$	35	Low	Input
$\overline{\text{BR}}$	278	Low	Output
$\overline{\text{CI}}$	304	Low	Output
$\overline{\text{CKSTP_IN}}$	266	Low	Input
$\overline{\text{CKSTP_OUT}}$	267	Low	Output
CLK_OUT	280	—	Output
CSE0–CSE1	288, 287	High	Output
$\overline{\text{DBB}}$	184	Low	I/O
$\overline{\text{DBG}}$	34	Low	Input
$\overline{\text{DBDIS}}$	193	Low	Input
$\overline{\text{DBWO}}$	32	Low	Input
DH0–31	147, 145, 143, 142, 140, 138, 126, 124, 122, 121, 119, 117, 115, 114, 112, 110, 108, 107, 105, 103, 101, 100, 98, 96, 94, 93, 91, 89, 87, 86, 84, 82	High	I/O
DL0–DL31	180, 178, 176, 174, 172, 170, 168, 166, 164, 162, 160, 158, 156, 154, 152, 150, 148, 136, 135, 133, 131, 129, 128, 65, 67, 69, 71, 73, 75, 77, 79, 81	High	I/O
DP0–DP7	49, 51, 53, 55, 57, 59, 61, 63	High	I/O

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Table 9. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DPE}}$	274	Low	Output
$\overline{\text{DRTRY}}$	197	Low	Input
DRVMOD0–DRVMOD1 [2]	301, 300	High	Input
$\overline{\text{GBL}}$	2	Low	I/O
GND	5, 13, 21, 29, 37, 44, 52, 60, 68, 76, 153, 161, 169, 177, 185, 192, 200, 208, 216, 224, 257, 291	—	—
HALTED	269	High	Output
$\overline{\text{HRESET}}$	265	Low	Input
$\overline{\text{INT}}$	234	Low	Input
L1_TSTCLK [1]	255	Low	Input
L2_INT	273	High	Input
L2_TSTCLK [1]	254	Low	Input
$\overline{\text{LSSD_MODE}}$ [1]	256	Low	Input
$\overline{\text{MCP}}$	232	Low	Input
OGND	3, 11, 19, 27, 39, 46, 54, 62, 70, 78, 85, 90, 95, 99, 104, 109, 113, 118, 123, 127, 132, 137, 141, 146, 151, 159, 167, 175, 183, 190, 202, 210, 218, 226, 235, 240, 247, 268, 275, 279, 284, 289, 296	—	—
OVDD [3]	7, 15, 23, 31, 43, 50, 58, 66, 74, 80, 83, 88, 92, 97, 102, 106, 111, 116, 120, 125, 130, 134, 139, 144, 149, 155, 163, 171, 179, 186, 198, 206, 214, 222, 230, 237, 244, 249, 272, 277, 282, 286, 293, 298, 303	—	—
PLL_CFG0–PLL_CFG3	264, 262, 261, 259	High	Input
$\overline{\text{RSRV}}$	297	Low	Output
RUN	270	High	Input
$\overline{\text{SHD}}$	40	Low	I/O
$\overline{\text{SMI}}$	233	Low	Input
$\overline{\text{SRESET}}$	236	Low	Input
SYSCLK	263	—	Input
$\overline{\text{TA}}$	195	Low	Input
TBEN	299	High	Input
$\overline{\text{TBST}}$	241	Low	I/O
TC0–TC2	285, 283, 281	High	Output

PRELIMINARY

Table 9. Pinout Listing for the C4-CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
TCK	252	High	Input
TDI	250	High	Input
TDO	248	High	Output
$\overline{\text{TEA}}$	194	Low	Input
TMS	251	High	Input
$\overline{\text{TRST}}$	253	Low	Input
$\overline{\text{TS}}$	187	Low	I/O
TSIZ0–TSIZ2	246, 245, 243	High	I/O
TT0–TT4	239, 238, 231, 229, 227	High	I/O
$\overline{\text{WT}}$	302	Low	Output
VDD [3]	1, 9, 17, 25, 33, 41, 48, 56, 64, 72, 157, 165, 173, 181, 188, 196, 204, 212, 220, 228, 242, 258	—	—
$\overline{\text{XATS}}$	189	Low	I/O

Notes:
1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance with these specifications.
3. In the Motorola 604 C4-CQFP package, there is no electrical distinction between the OVDD and the VDD pins. These signals are internally shorted together. The OVDD and VDD signals have been listed separately to maintain compatibility with future parts.

PRELIMINARY

1.5.2 Pinout Listing for the BGA Package

Table 10 provides the pinout listing for the 604 BGA package.

Table 10. Pinout Listing for the BGA Package

Signal Name	Pin Number	Active	I/O
A0–A31	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP0–AP3	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
ARRAY_WR [1]	B07	Low	Input
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—

Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{BG}$	L01	Low	Input
$\overline{BR}$	B06	Low	Output
$\overline{CI}$	E01	Low	Output
$\overline{CKSTP_IN}$	D08	Low	Input
$\overline{CKSTP_OUT}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE0–CSE1	B01, B05	High	Output
$\overline{DBB}$	J14	Low	I/O
$\overline{DBG}$	N01	Low	Input
$\overline{DBDIS}$	H15	Low	Input
$\overline{DBWO}$	G04	Low	Input
DH0–31	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL0–DL31	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP0–DP7	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{DPE}$	A05	Low	Output
$\overline{DRTRY}$	G16	Low	Input
DRVMOD0–DRVMOD1 [2]	D05, C03	High	Input
$\overline{GBL}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
HALTED	B08	High	Output
$\overline{HRESET}$	A07	Low	Input
$\overline{INT}$	B15	Low	Input
L1_TSTCLK [1]	D11	Low	Input
L2_INT	D06	High	Input
L2_TSTCLK [1]	D12	Low	Input
$\overline{LSSD_MODE}$ [1]	B10	Low	Input
$\overline{MCP}$	C13	Low	Input
OVDD [3]	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—

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Table 10. Pinout Listing for the BGA Package (Continued)

Signal Name	Pin Number	Active	I/O
PLL_CFG0–PLL_CFG3	A08, B09, A09, D09	High	Input
$\overline{\text{RSRV}}$	D01	Low	Output
RUN	C08	High	Input
$\overline{\text{SHD}}$	H04	Low	I/O
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC0–TC2	A02, A03, C06	High	Output
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ0–TSIZ2	A13, D10, B12	High	I/O
TT0–TT4	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD [3]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—
$\overline{\text{XATS}}$	J16	Low	I/O

Notes:

1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. These are drive mode signals that must be pulled up to VDD to operate in accordance to these specifications.
3. In the 604 BGA package, there is no electrical distinction between the OVDD and the VDD pins. These signals are internally shorted together. The OVDD and VDD signals have been listed separately to maintain compatibility with future parts.

PRELIMINARY

1.6 PowerPC 604 Microprocessor Package Description

The following sections provide the package parameters and the mechanical dimensions for the 604.

1.6.1 C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the C4-CQFP package.

1.6.1.1 Motorola C4-CQFP Package Parameters

The package parameters for the Motorola C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
C4 encapsulation	Glass-filled Epoxy
Maximum module height	3.25 mm
Co-planarity specification	0.10 mm

1.6.1.2 IBM C4-CQFP Package Parameters

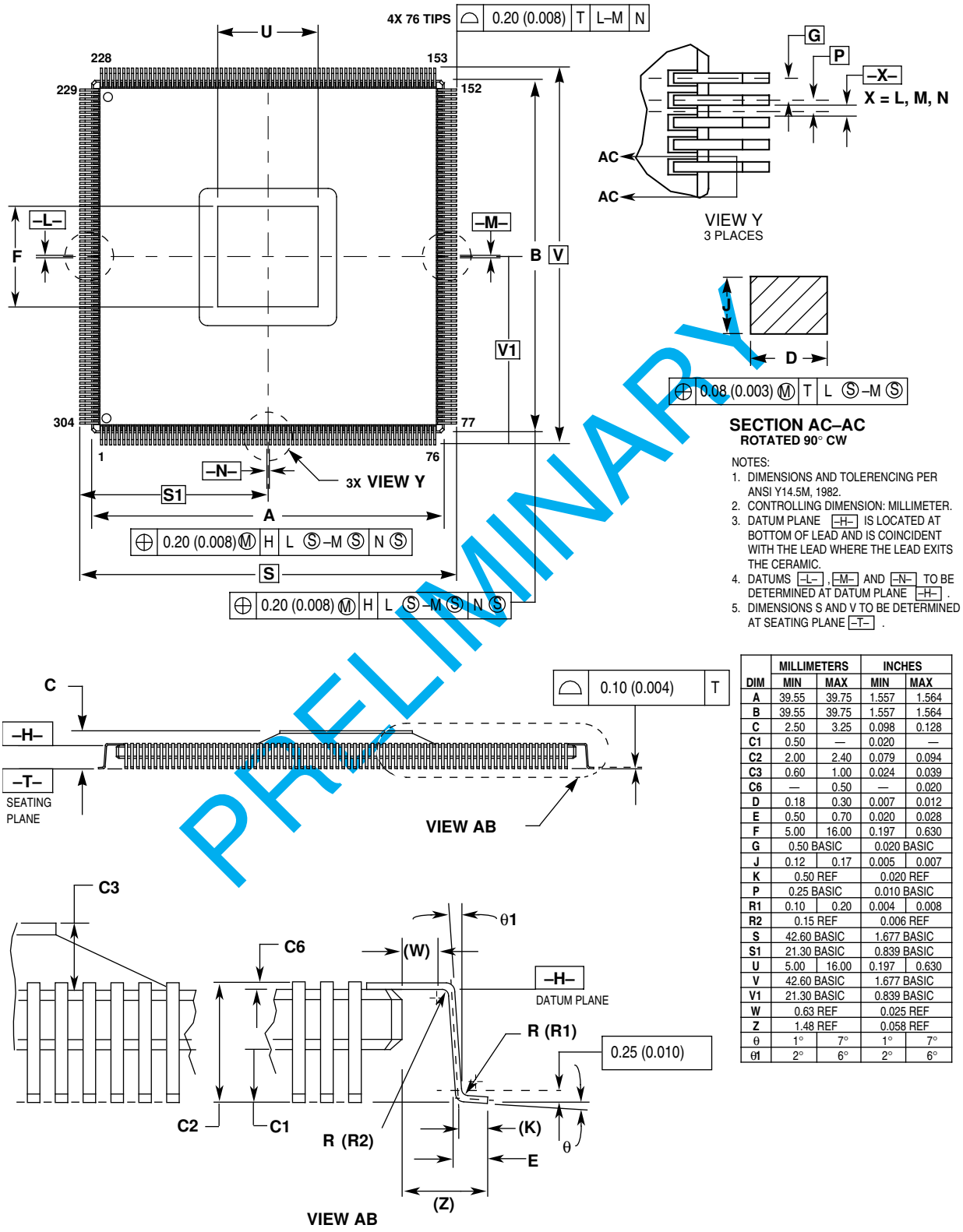
The package parameters for the IBM C4-CQFP are as provided in the following list. The package type is 40 mm, 304-pin ceramic quad flat pack.

Package outline	40 mm
Interconnects	304
Pitch	0.5 mm
Lead plating	Ni Au
Lead encapsulation	Glass-filled Epoxy
C4 encapsulation	Glass-filled Epoxy
Maximum module height	2.92 mm
Co-planarity specification	0.08 mm

PRELIMINARY

1.6.1.3 Mechanical Dimensions of the Motorola C4-CQFP Package

Figure 11 shows the mechanical dimensions of the Motorola C4-CQFP package.



NOTES:
1. DIMENSIONS AND TOLERENCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE CERAMIC.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.

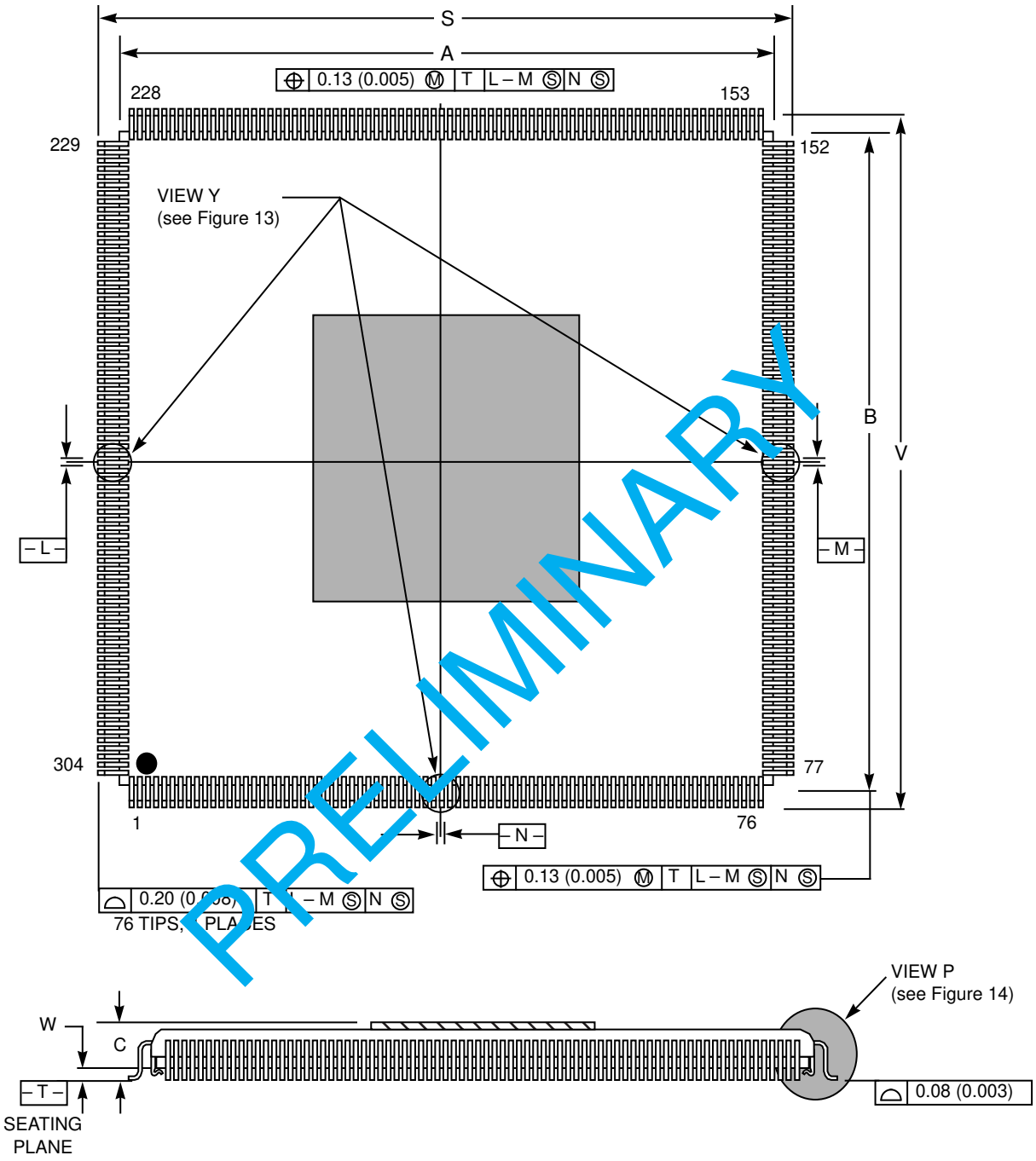
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	39.55	39.75	1.557	1.564
B	39.55	39.75	1.557	1.564
C	2.50	3.25	0.098	0.128
C1	0.50	—	0.020	—
C2	2.00	2.40	0.079	0.094
C3	0.60	1.00	0.024	0.039
C6	—	0.50	—	0.020
D	0.18	0.30	0.007	0.012
E	0.50	0.70	0.020	0.028
F	5.00	16.00	0.197	0.630
G	0.50 BASIC		0.020 BASIC	
J	0.12	0.17	0.005	0.007
K	0.50 REF		0.020 REF	
P	0.25 BASIC		0.010 BASIC	
R1	0.10	0.20	0.004	0.008
R2	0.15 REF		0.006 REF	
S	42.60 BASIC		1.677 BASIC	
S1	21.30 BASIC		0.839 BASIC	
U	5.00	16.00	0.197	0.630
V	42.60 BASIC		1.677 BASIC	
V1	21.30 BASIC		0.839 BASIC	
W	0.63 REF		0.025 REF	
Z	1.48 REF		0.058 REF	
θ	1°	7°	1°	7°
θ1	2°	6°	2°	6°

PRELIMINARY

Figure 11. Mechanical Dimensions of the Motorola C4-CQFP Package

1.6.1.4 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 12 shows the mechanical dimensions for the IBM C4-CQFP package.



PRELIMINARY

Figure 12. Mechanical Dimensions of the IBM C4-CQFP Package

Figure 13 and Figure 14 provide a more detailed representation of portions of IBM C4-CQFP package.

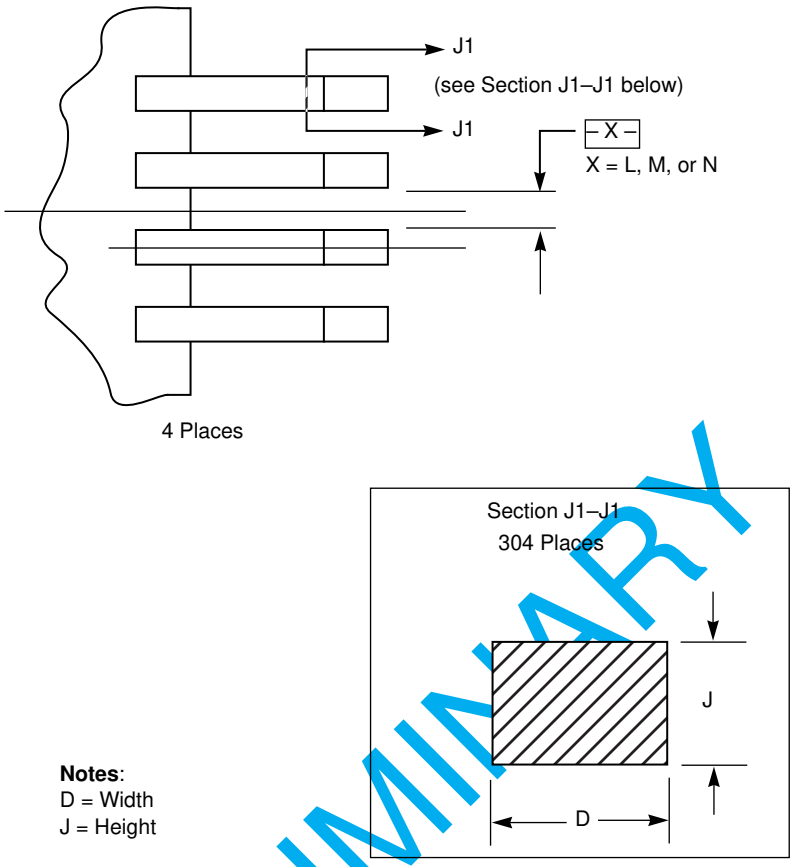


Figure 13. IBM C4-CQFP Mechanical Dimensions—View Y

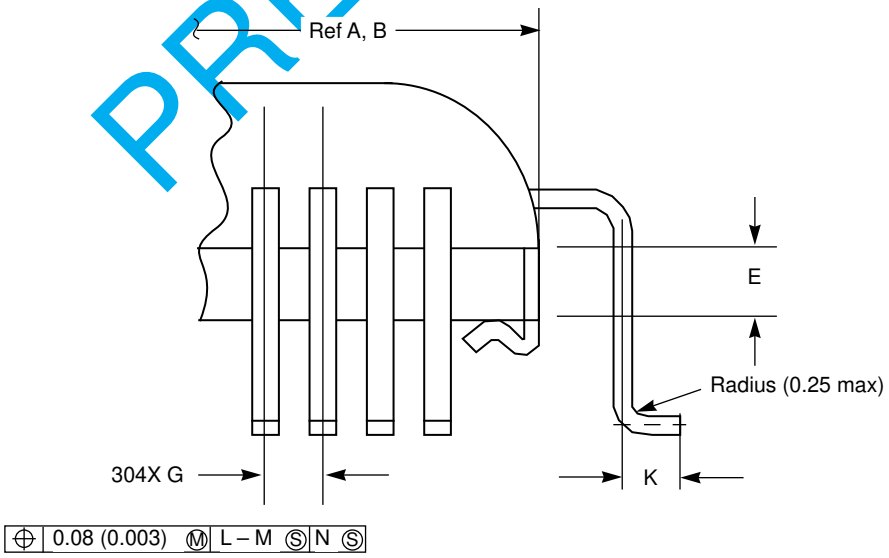


Figure 14. IBM C4-CQFP Mechanical Dimensions—View P

PRELIMINARY

Table 11 lists the mechanical dimensions values for the IBM C4-CQFP package.

Table 11. Mechanical Dimensions Values

Dim	Millimeters	
	Min	Max
A	39.93	40.08
B	39.93	40.08
C	2.32	2.92
D	0.23	0.28
E	0.635 REF	
G	0.5 BSC	
J	0.12	0.20
K	0.40	0.60
S	42.4	42.8
V	42.4	42.8
W	0.35	—

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982.
2. Controlling dimension—millimeter.
3. Datums – L –, –M –, and – N – to be determined at seating plane.
4. Dimensions S and V to be determined at seating plane – T–.
5. Dimensions A and B to outside of lead clip.

PRELIMINARY

1.6.2 BGA Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM and Motorola BGA packages.

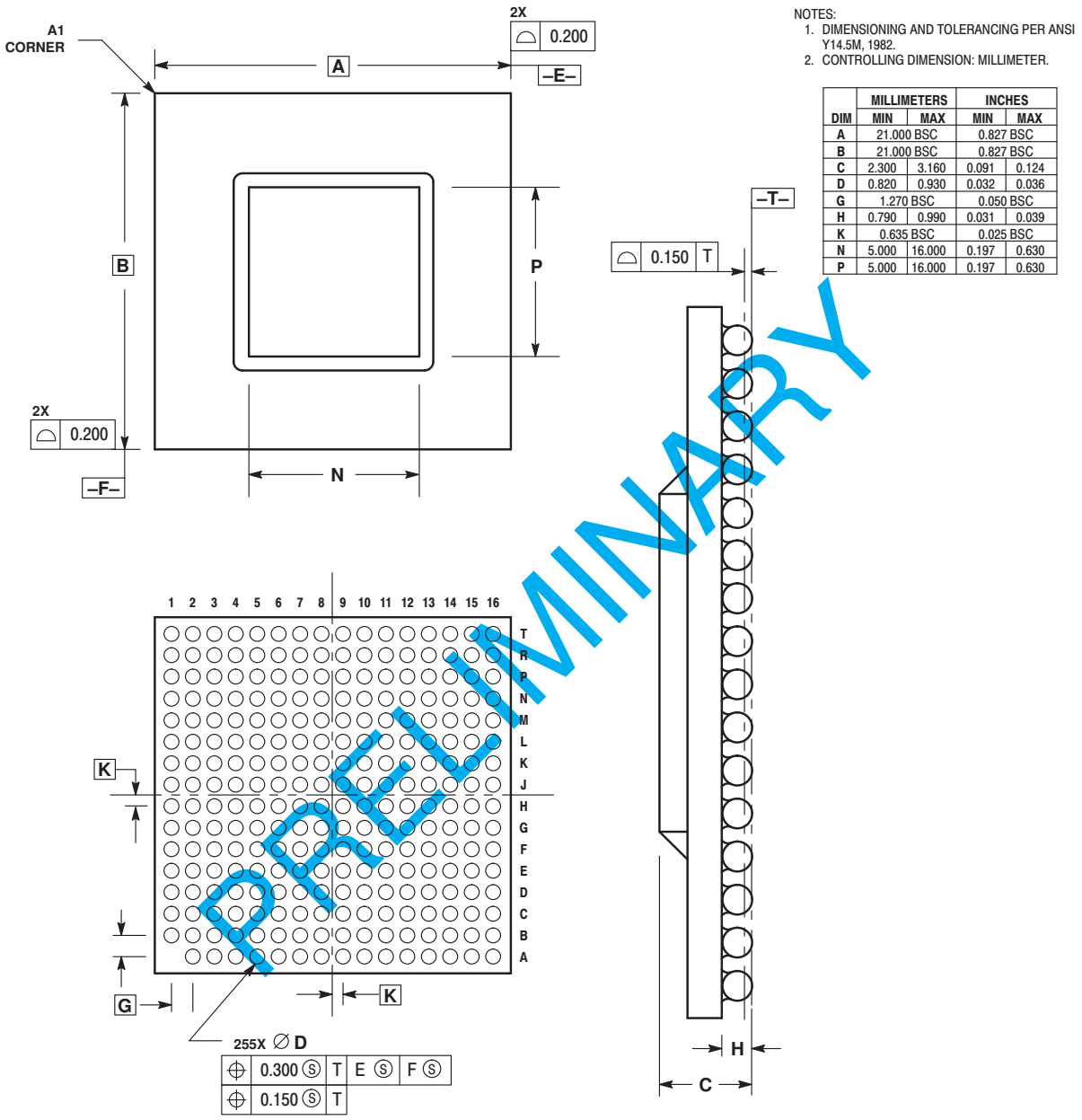
1.6.2.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 mm, 256-lead ceramic ball grid array (BGA).

Package outline	21 mm
Interconnects	255
Pitch	1.27 mm
Maximum module height	3.16 mm

1.6.2.2 Mechanical Dimensions of the BGA Package

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the IBM and Motorola BGA package.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.300	3.160	0.091	0.124
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

PRELIMINARY

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature of the BGA Package

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 604.

1.7.1 PLL Configuration

The SYSCLK input determines the external bus frequency at which the 604 will operate. The internal PLL can be configured to provide an internal (processor core) frequency that is a multiple of the external bus clock frequency. The PLL is configured by the PLL_CFG0–PLL_CFG3 signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU frequency of operation as shown in Table 12.

Table 12. PLL Configuration

PLL_CFG0 to PLL_CFG3	Bus, CPU and VCO Frequencies								
	CPU/ SYSCLK Ratio	Bus 16.6 MHz	Bus 20 MHz	Bus 25 MHz	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 60 MHz	Bus 66.6 MHz
0001	1:1	—	—	—	—	—	50 (200)	60 (240)	66.6 (266)
0100	2:1	—	—	—	—	—	100 (200)	120 (240)	133 (266)
0101	2:1	—	—	50 (200)	66.6 (266)	80 (320)	—	—	—
1000	3:1	—	—	—	100 (200)	120 (240)	150 (300)	—	—
1001	3:1	50 (200)	60 (240)	75 (300)					
1100	1.5:1				—	—	—	90 (180)	100 (200)
1101	1:5:1				50 (200)	60 (240)	75 (300)	90 (360)	
0011	PLL Bypass								

PRELIMINARY

Notes:

1. Some PLL configurations may select bus, CPU, or VCO frequencies which are not useful, not supported, or not tested for by the 604. VCO frequencies (shown in parenthesis in Table 12) should not fall below 180 MHz, and should not exceed 360 MHz.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, and the bus is set for 1:1 mode operation. The PLL-bypass mode is for test purposes only, and is not intended for functional use.
3. PLL_CFG0–PLL_CFG1 select the CPU-to-bus ratio (1:1,1.5:1, 2:1, 3:1), PLL_CFG2–PLL_CFG3 select the CPU-to-PLL multiplier (x2, x4).

1.7.2 PLL Power Supply Filtering

The AVDD power signal is provided on the 604 to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVDD input signal should be filtered using a circuit similar to the one shown in Figure 16. Note that the capacitors should be placed as close as possible to the AVDD input signal.

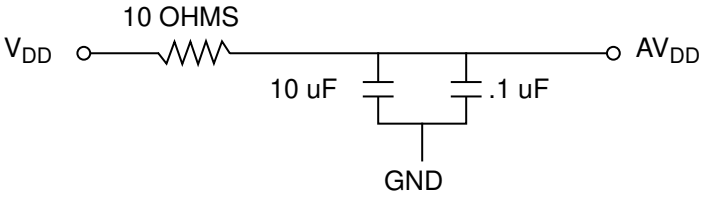


Figure 16. PLL Power Supply Filter Circuit

1.7.3 Decoupling Recommendations

The 604 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 604 system, and the 604 itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin of the 604.

These capacitors should range in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantalum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance in the traces. Power and ground connections must be made to all external Vdd and GND pins of the 604.

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) pins must remain unconnected.

PRELIMINARY

1.8 Thermal Management Information

This section provides thermal management information for the C4-CQFP and the BGA packages. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, airflow and the thermal interface material. Heat sinks are typically attached to a chip package by means of a spring clip to holes in the printed-circuit board; see Figure 17.

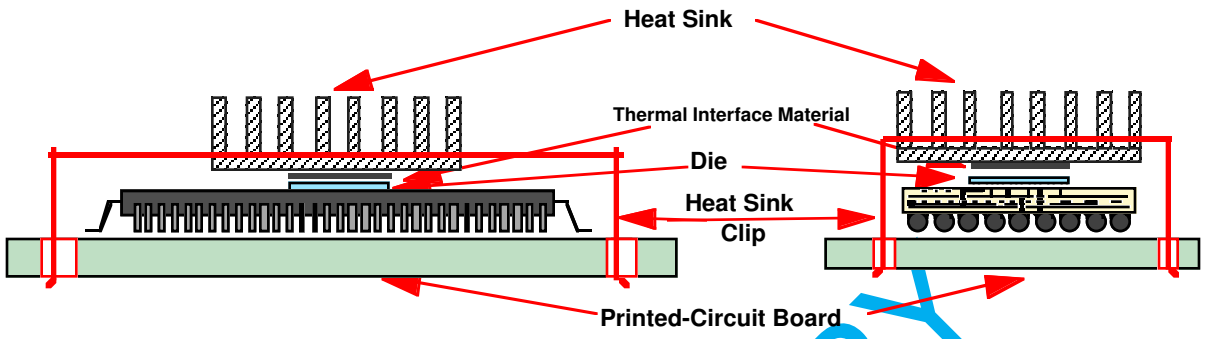


Figure 17. C4-CQFP and BGA Exploded Cross-Sectional View with Heat Sink

The board designer can choose between several types of heat sinks to place on the 604. There are several commercially-available heat sinks for the 604 provided by the following vendors:

Thermalloy
2021 W. Valley View Lane — 214-243-4321
P.O. Box 810839
Dallas, TX 75731

International Electronic Research Corporation (IERC)
135 W. Magnolia Blvd.
Burbank, CA 91502 — 818-842-7277

Aavid Engineering — 603-528-3400
One Kool Path
Laconic, NH 03247-0440

Wakefield Engineering — 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Ultimately, the final selection of an appropriate heat sink for the 604 depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

PRELIMINARY

1.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, the intrinsic conduction thermal resistance paths are as follows:

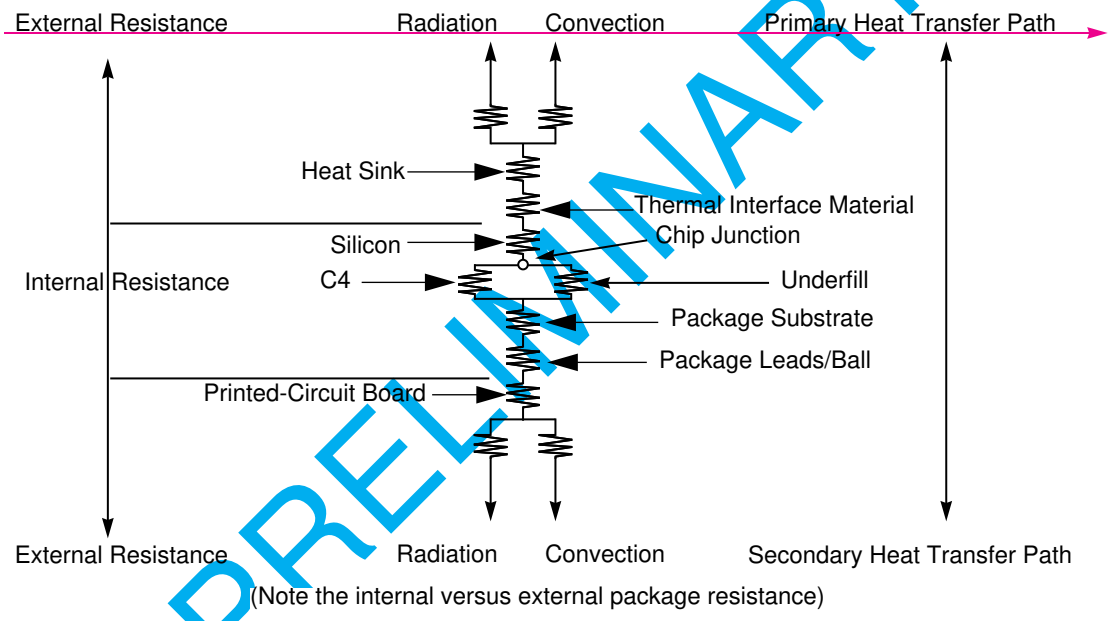
- The die junction-to-case thermal resistance
- The die junction-to-lead thermal resistance

These parameters are shown in Table 13.

Table 13. Package Thermal Resistance

Thermal Metric	C4-CQFP	BGA
Junction-to-case thermal resistance	0.03 °C/W	0.03 °C/W
Junction-to-lead (ball) thermal resistance	18.0 °C/W	2.2 °C/W

Figure 18 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



PRELIMINARY

Figure 18. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms. The following section provides a thermal management example for the 604 using one of the commercially available heat-sinks.

1.8.2 Thermal Management Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (R_{\theta jc} + R_a + R_{sa}) * Q$$

Where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the system cabinet
$R_{\theta jc}$ is the die-junction-to-case (top of die) thermal resistance of the device
R_a is the thermal resistance of the thermal interface material (thermal grease or thermal compound)
R_{sa} is the heat sink-to-ambient thermal resistance
Q is the power dissipated by the device

Typical die-junction temperatures (T_j) should be maintained less than 105 °C. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. A computer cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The thermal resistance of the interface material (R_a) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, and a power dissipation (Q) of 18 watts, the following expression for T_j is obtained:

Junction temperature: $T_j = 30\ °C + 5\ °C + (0.03\ °C/W + 1.0\ °C/W + R_{sa}) * 18\ W$

For a Thermalloy heat sink #2333B, the heatsink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 19.

PRELIMINARY

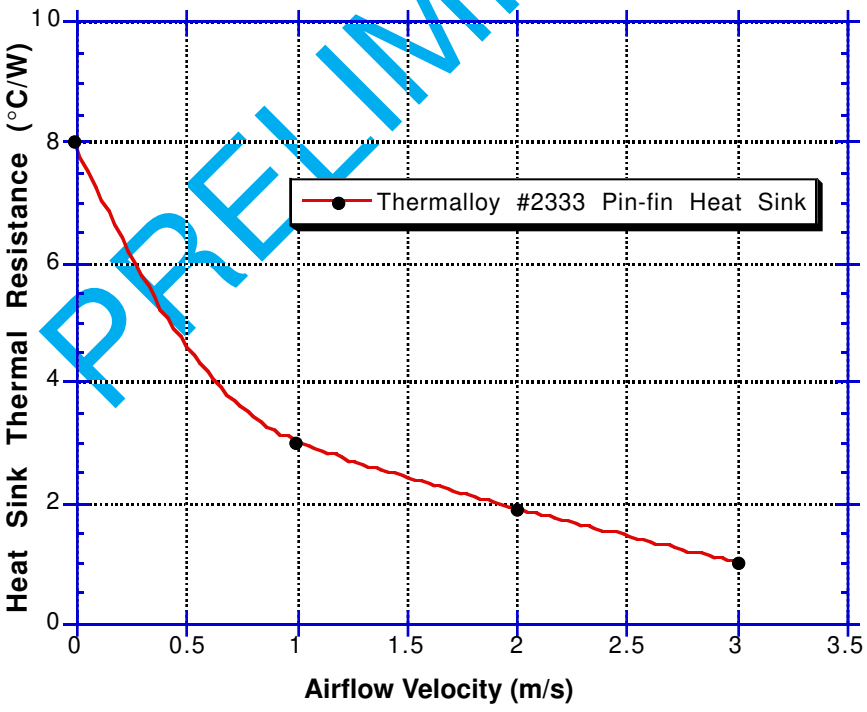


Figure 19. Thermalloy #2333B Pin-Fin Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Assuming an air velocity of 1 m/s, we have an effective R_{sa} of 3 °C/W, thus

$$T_j = 30°C + 5°C + (0.03\ °C/W + 1.0\ °C/W + 3\ °C/W) * 18\ W,$$

resulting in a junction temperature of approximately 107 °C which is more than the maximum operating temperature of the part. To ensure maximum reliability, it is desirable to operate the 604 well within its operating temperature range. Thus, to keep an 18-watts 604 within its proper operating range, an air velocity greater than 1 m/s should be used with the Thermalloy #2333B pin-fin heat sink.

Other heat sinks offered by Thermalloy, Aavid, Wakefield, and IERC offer different heat sink-to-ambient thermal resistances, and may or may not need air flow. It is necessary to perform an analysis as done above to select the desired heat sink.

Though the junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, next-level interconnect technology, system air temperature rise, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs. To expedite system-level thermal analysis, several “compact” thermal-package models are available within FLOTHERM®. These are available upon request.

1.9 Ordering Information

This section provides the part numbering nomenclature for the 604. Note that the individual part numbers correspond to a specific combination of 604 internal/bus frequencies, which must be observed to ensure proper operation of the device. For available frequency combinations, contact your local Motorola or IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier allows for the availability of future enhanced parts (that is, lower voltage, lower power, higher performance, etc.).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

PRELIMINARY

1.9.1 Motorola Part Number Key

Figure 20 provides the Motorola part numbering nomenclature for the 604.

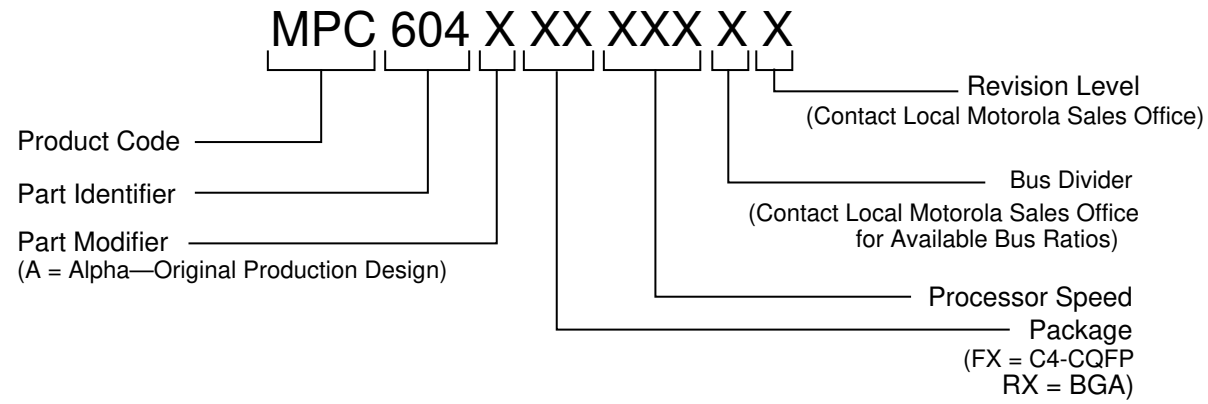


Figure 20. Motorola Part Number Key

1.9.2 IBM Part Number Key

Figure 21 provides the IBM part numbering nomenclature for the 604.

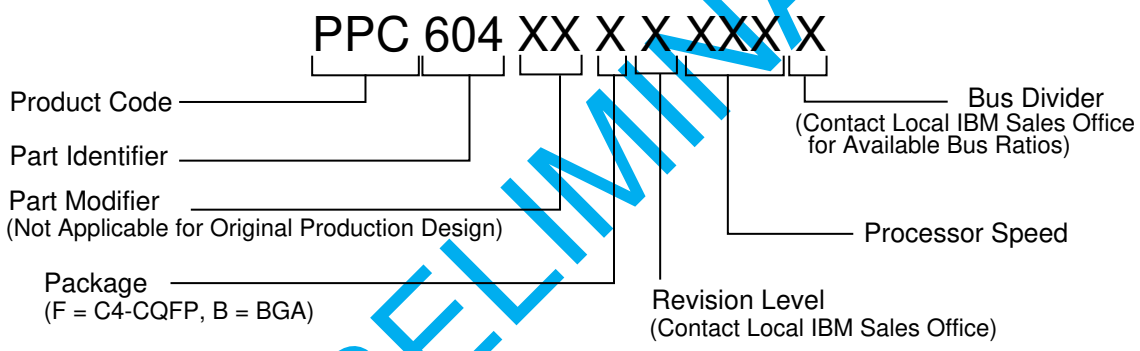


Figure 21. IBM Part Number Key

PRELIMINARY

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Ⓜ MOTOROLA

Preliminary **4M x 36 DRAM Module**

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

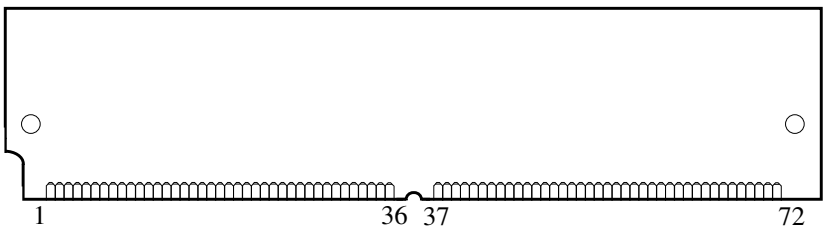
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 2048 refresh cycles distributed across 32ms
- 11/11 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D4360B is a 16MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 4Mx36 high speed memory array that is intended for use in 18, 36, and 72 bit parity applications. It is manufactured with 8 4Mx4 devices, each in a 300mil package, and 4 4Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25” long footprint. Related products include the 4Mx32 non-parity SIMM, IBM11D4320B, as well as other density and ECC-optimized SIMMs.

Card Outline



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Pin Description

$\overline{RAS}$0, $\overline{RAS}$2	Row Address Strobe
$\overline{CAS}$0 - $\overline{CAS}$3	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A10	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS}$0	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS}$2	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS}$3	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS}$1	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS}$0	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS}$2	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D4360BA-60	4M x 36	60ns	Sn/Pb	4.25” x 1” x .360”	
IBM11D4360BA-70	4M x 36	70ns	Sn/Pb	4.25” x 1” x .360”	
IBM11E4360BA-60	4M x 36	60ns	Au	4.25” x 1” x .360”	
IBM11E4360BA-70	4M x 36	70ns	Au	4.25” x 1” x .360”	

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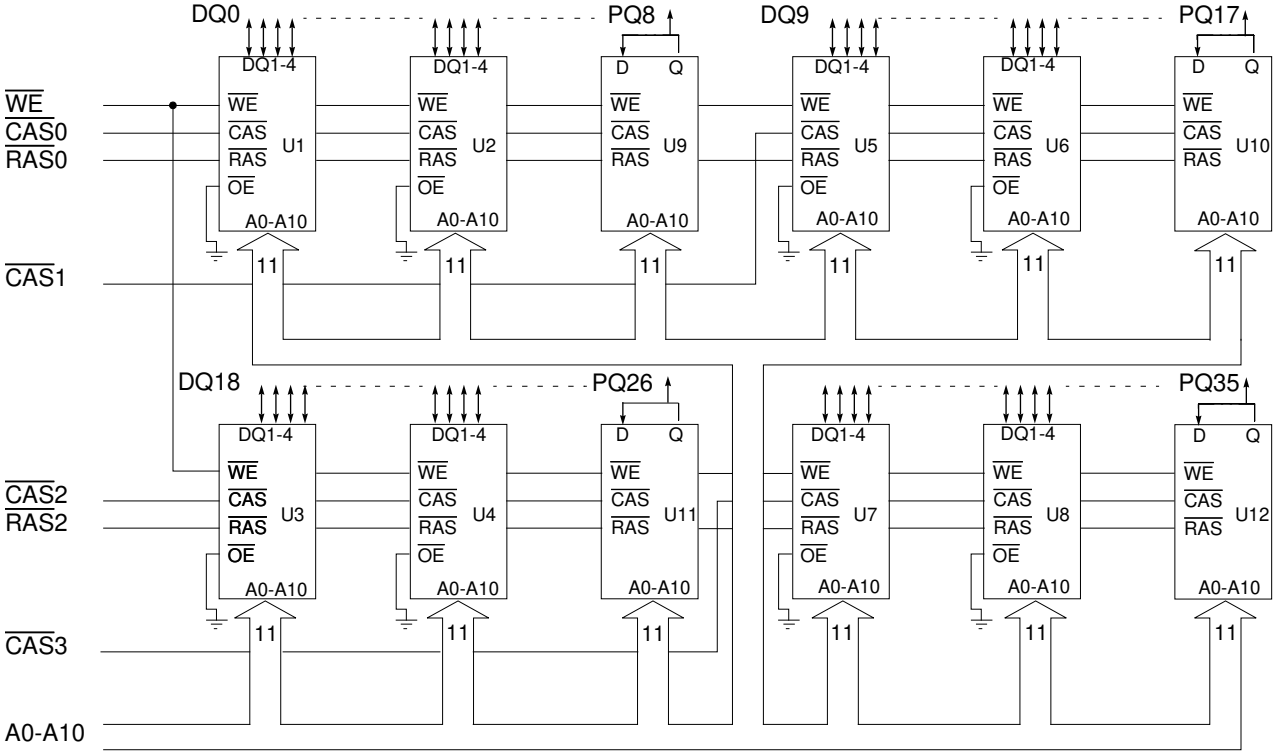
Block Diagram



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Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min(V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	7.9	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	Vcc + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A10)	78	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	31	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	18	pF	

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DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 2, 3
		-70	—	1280		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	1240	mA	1, 2, 3
		-70	—	1080		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1440	mA	1, 3
		-70	—	1280		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

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AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

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Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	45	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

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Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1, 2

1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	32	—	32	ms	1

1. 2048 refreshes are required every 32ms.

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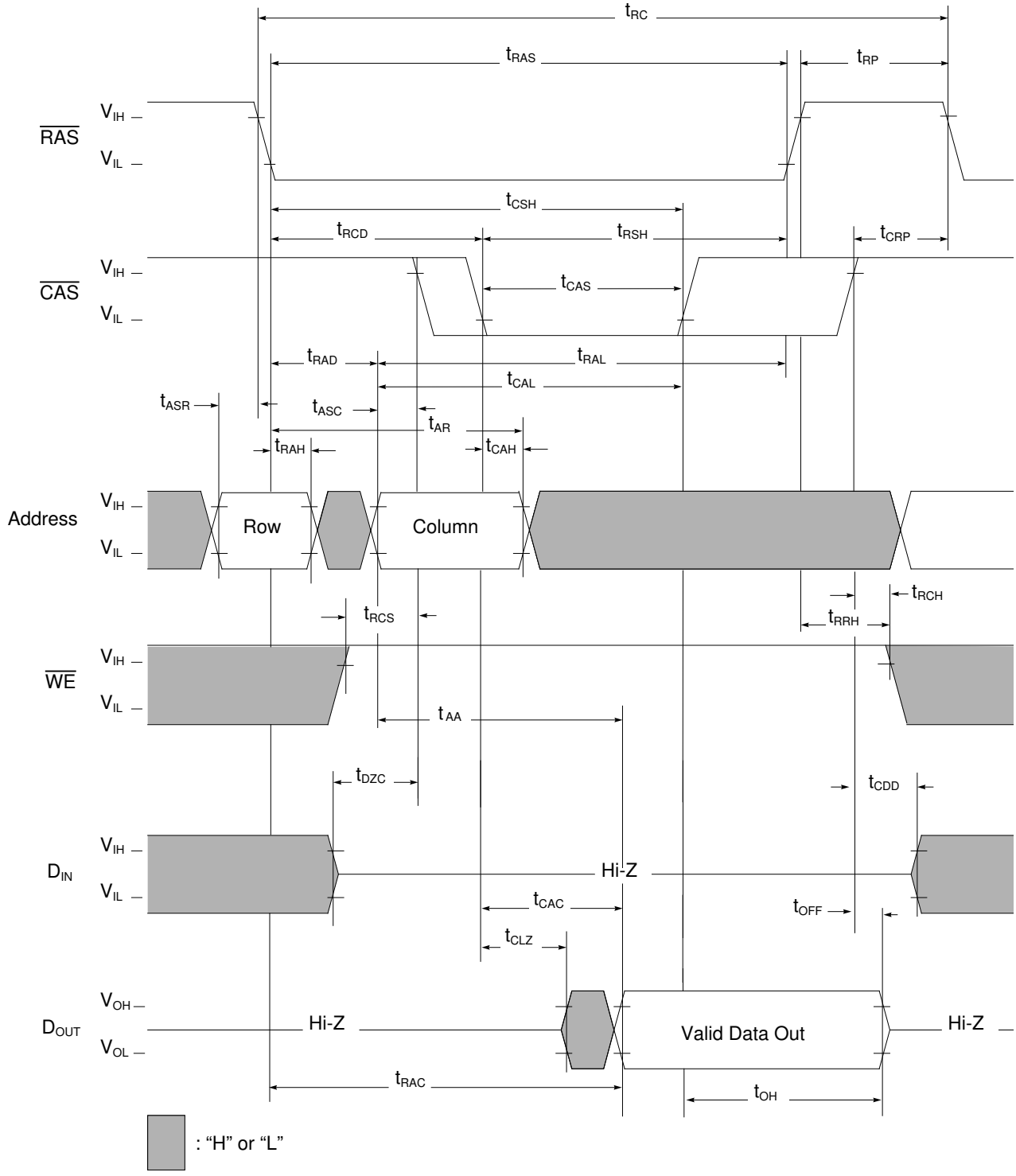
Read



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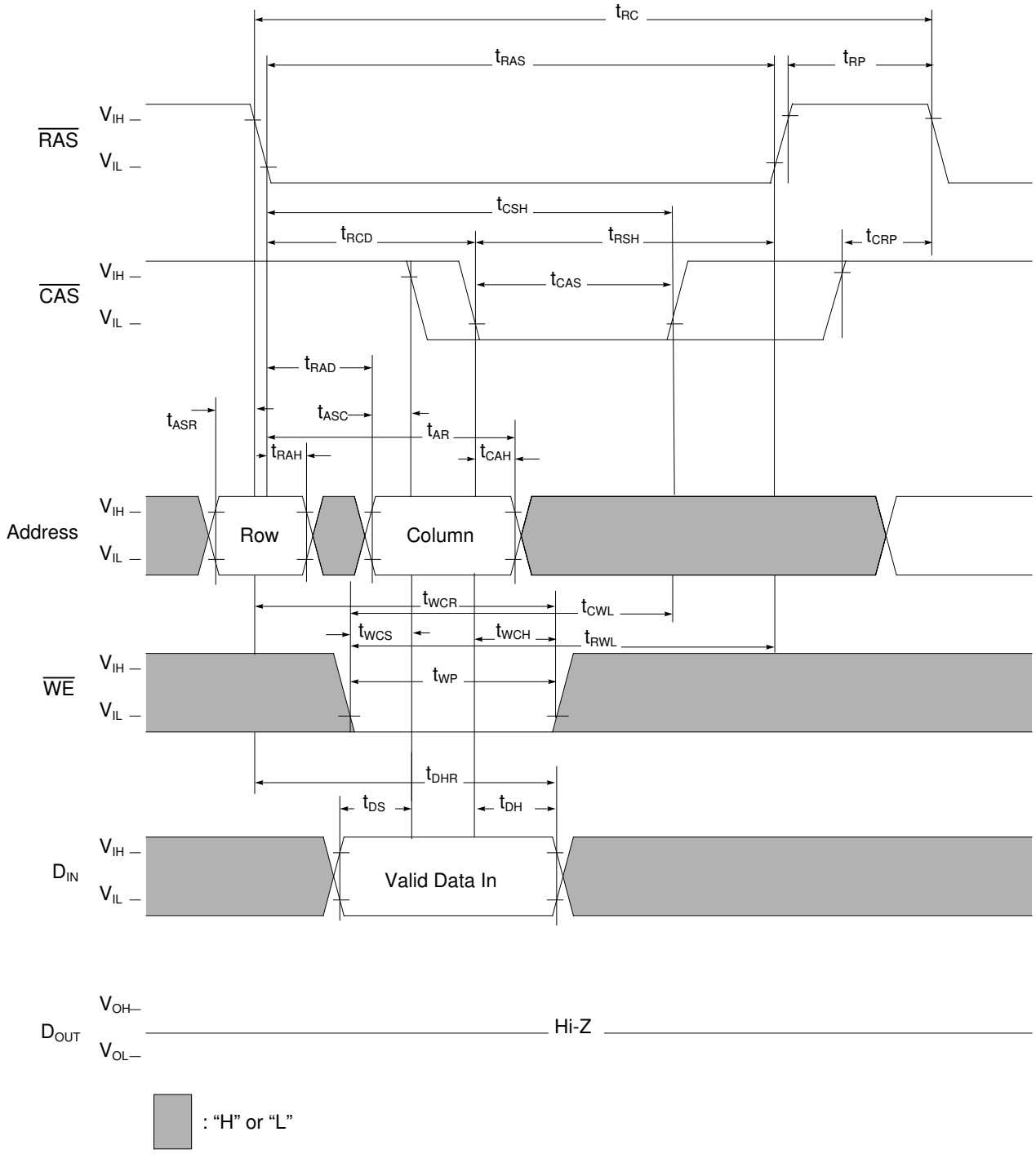
Write Cycle (Early Write)



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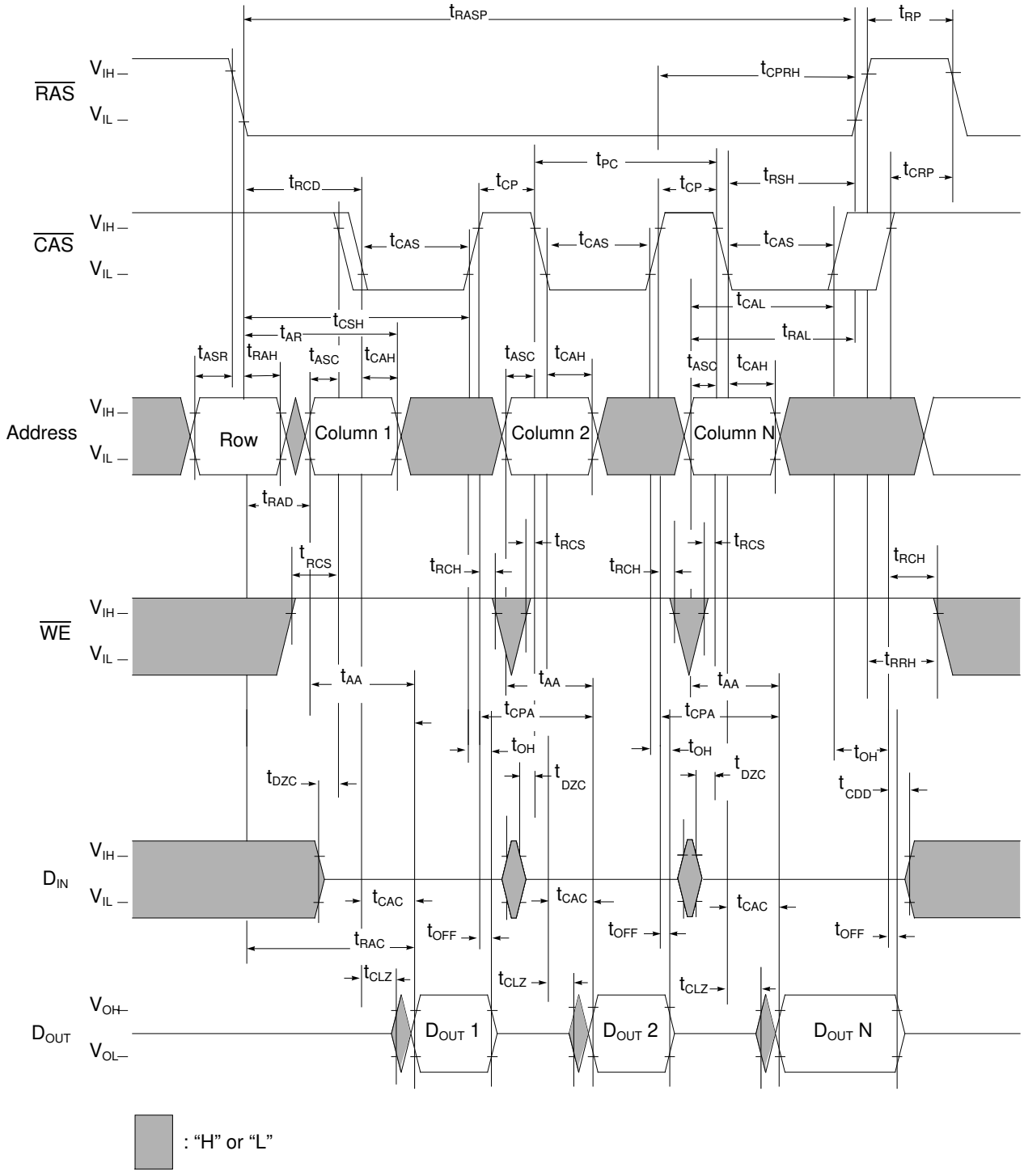
Fast Page Mode Read Cycle



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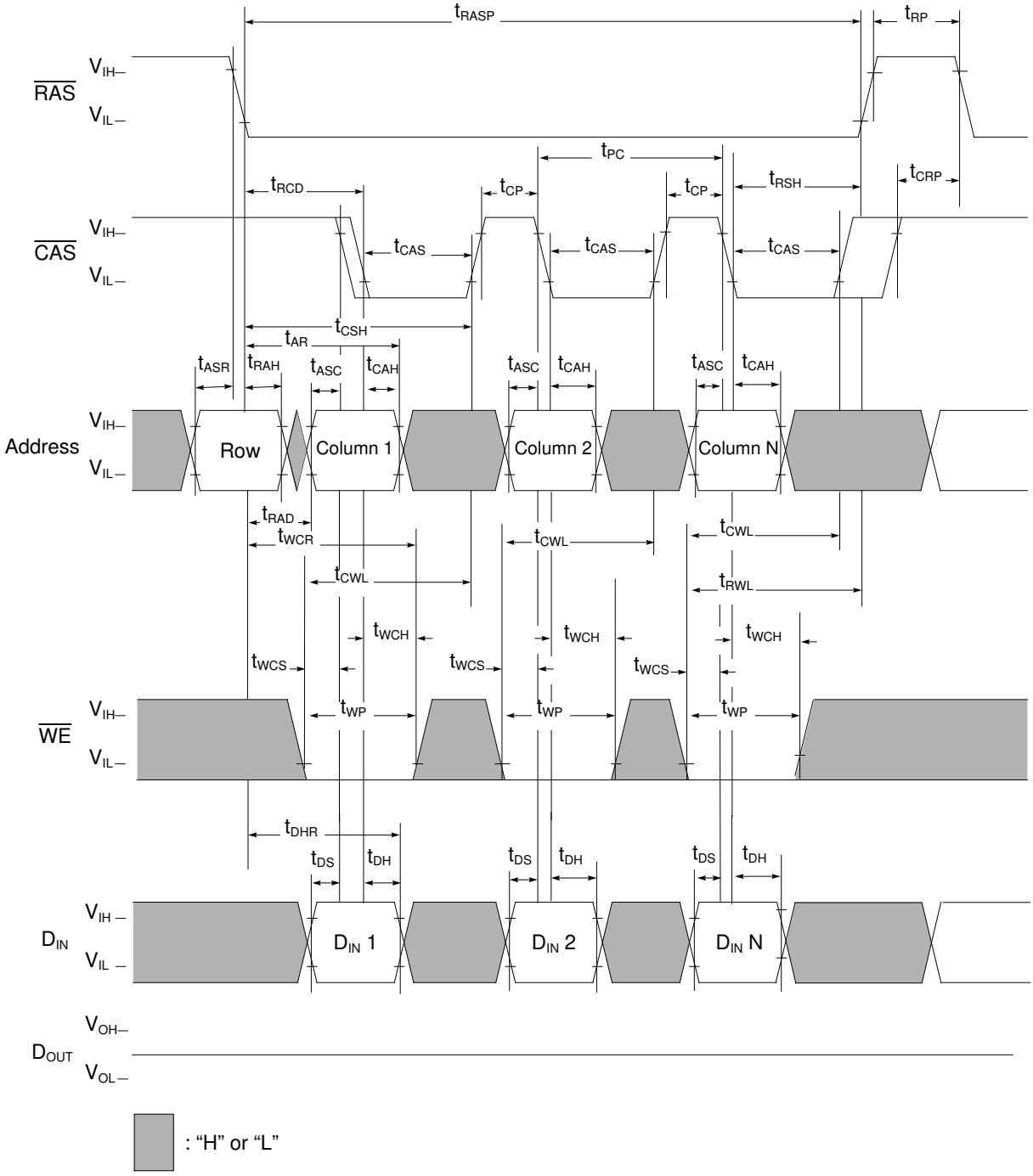
Fast Page Mode Write Cycle



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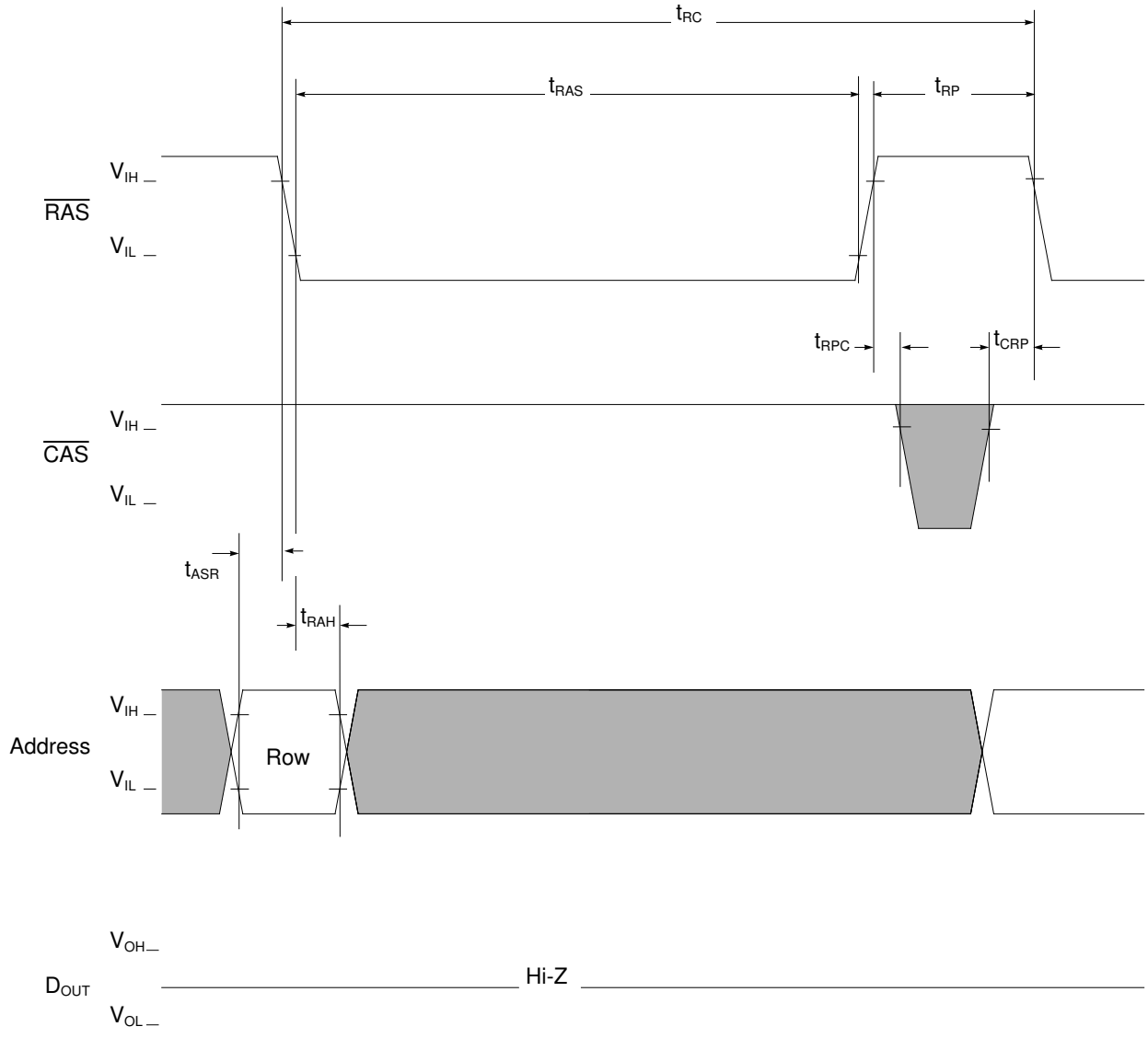
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

Note: $\overline{WE}$, D_{IN} are "H" or "L"

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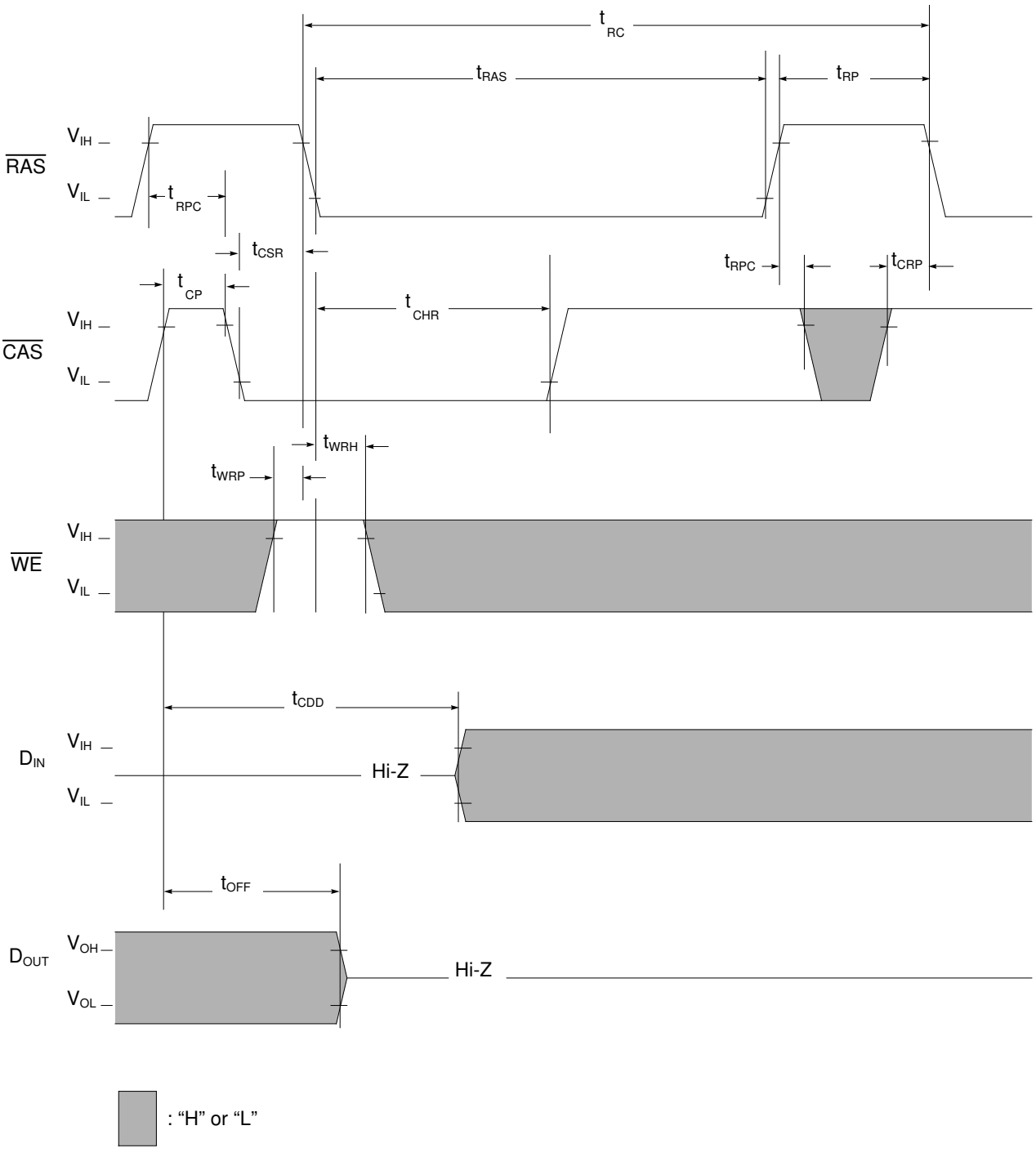
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



Note: Addresses are "H" or "L"

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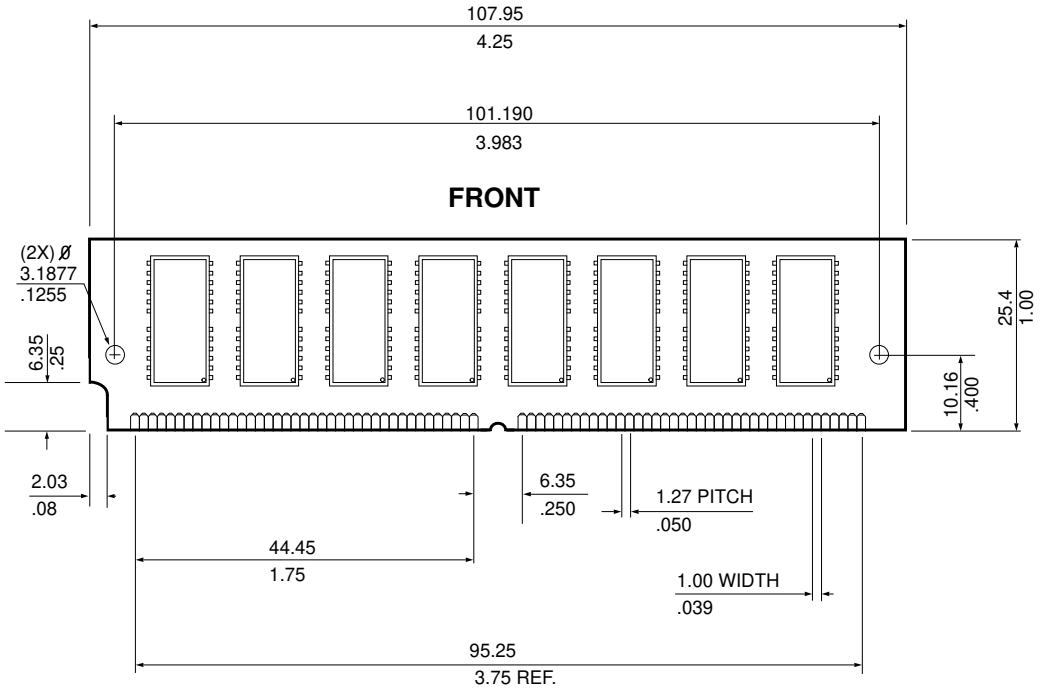
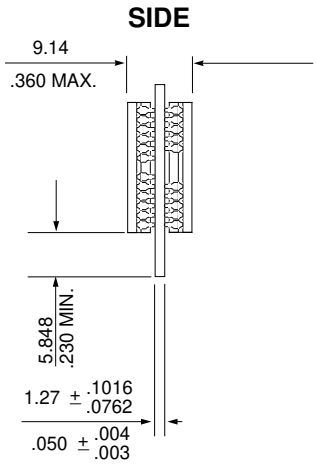
Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

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Revision Log

Rev	Contents of Modification
7/94	Initial release of 1Mx36 specification using 4Mx4 die revision “C”.

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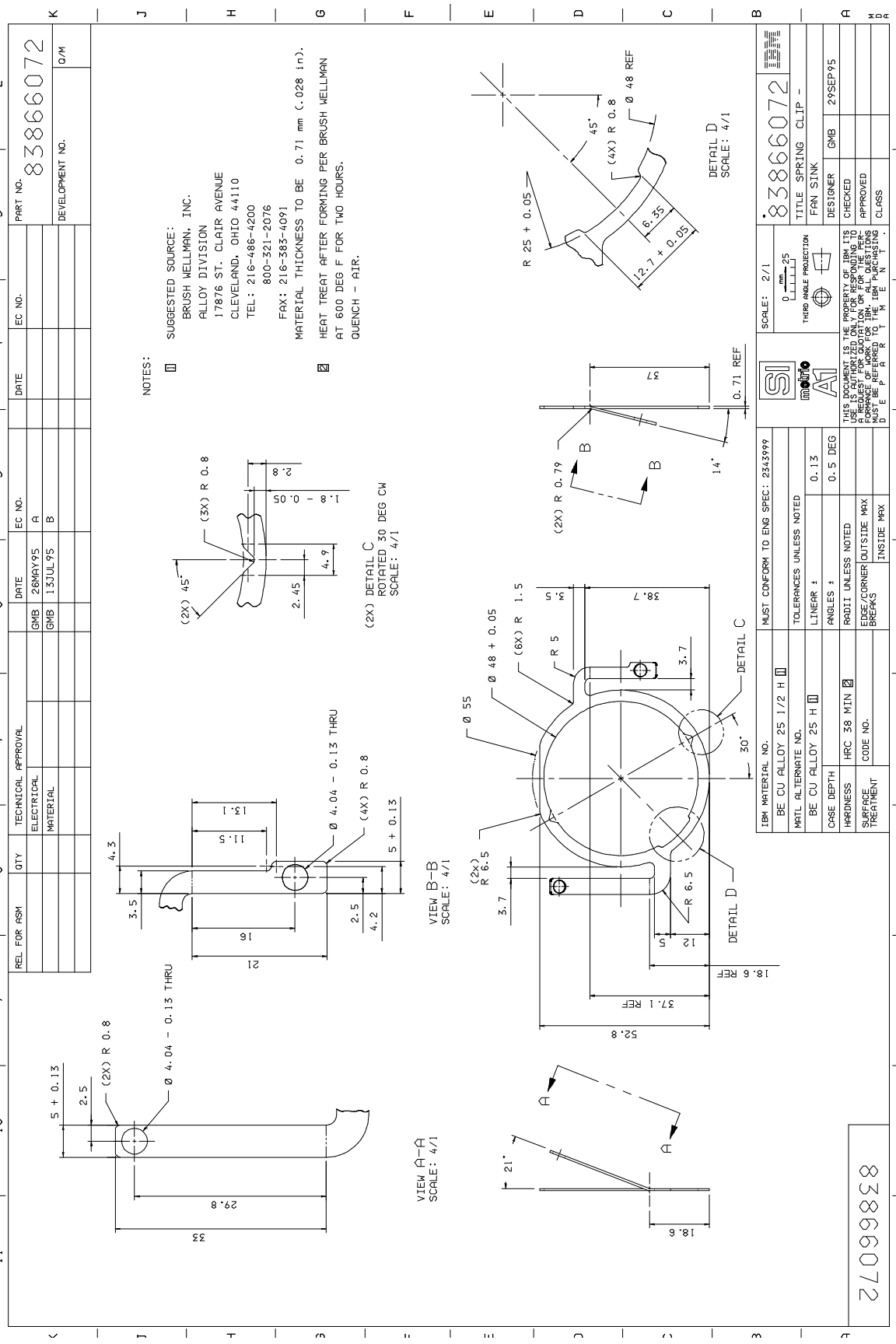
8386072
DEVELOPMENT NO.
Q/M
NOTES:
1. SUGGESTED SOURCE:
BRUSH WELLMAN, INC.
ALLOY DIVISION
17876 ST. CLAIR AVENUE
CLEVELAND, OHIO 44110
TEL: 216-486-4200
800-321-2076
FAX: 216-383-4091
MATERIAL THICKNESS TO BE 0.71 mm (.028 in).
2. HEAT TREAT AFTER FORMING PER BRUSH WELLMAN
AT 600 DEG F FOR TWO HOURS.
QUENCH - AIR.
(2X) DETAIL C
ROTATED 30 DEG CW
SCALE: 4/1
VIEW B-B
SCALE: 4/1
VIEW A-A
SCALE: 4/1
DETAIL D
SCALE: 4/1
DETAIL C
SCALE: 2/1
8386072
TITLE SPRING CLIP -
FAN SINK
DESIGNER GMB 29SEP95
CHECKED
APPROVED
CLASS
IBM MATERIAL NO.
BE CU ALLOY 25 1/2 H
MATL ALTERNATE NO.
BE CU ALLOY 25 H
CASE DEPTH
HARDNESS HRC 38 MIN
SURFACE TREATMENT
CODE NO.
MUST CONFORM TO ENG SPEC: 2343999
TOLERANCES UNLESS NOTED
LINEAR ±
ANGLES ±
RADII UNLESS NOTED
EDGE/CORNER BREAKS
OUTSIDE MAX
INSIDE MAX
0.13
0.5 DEG
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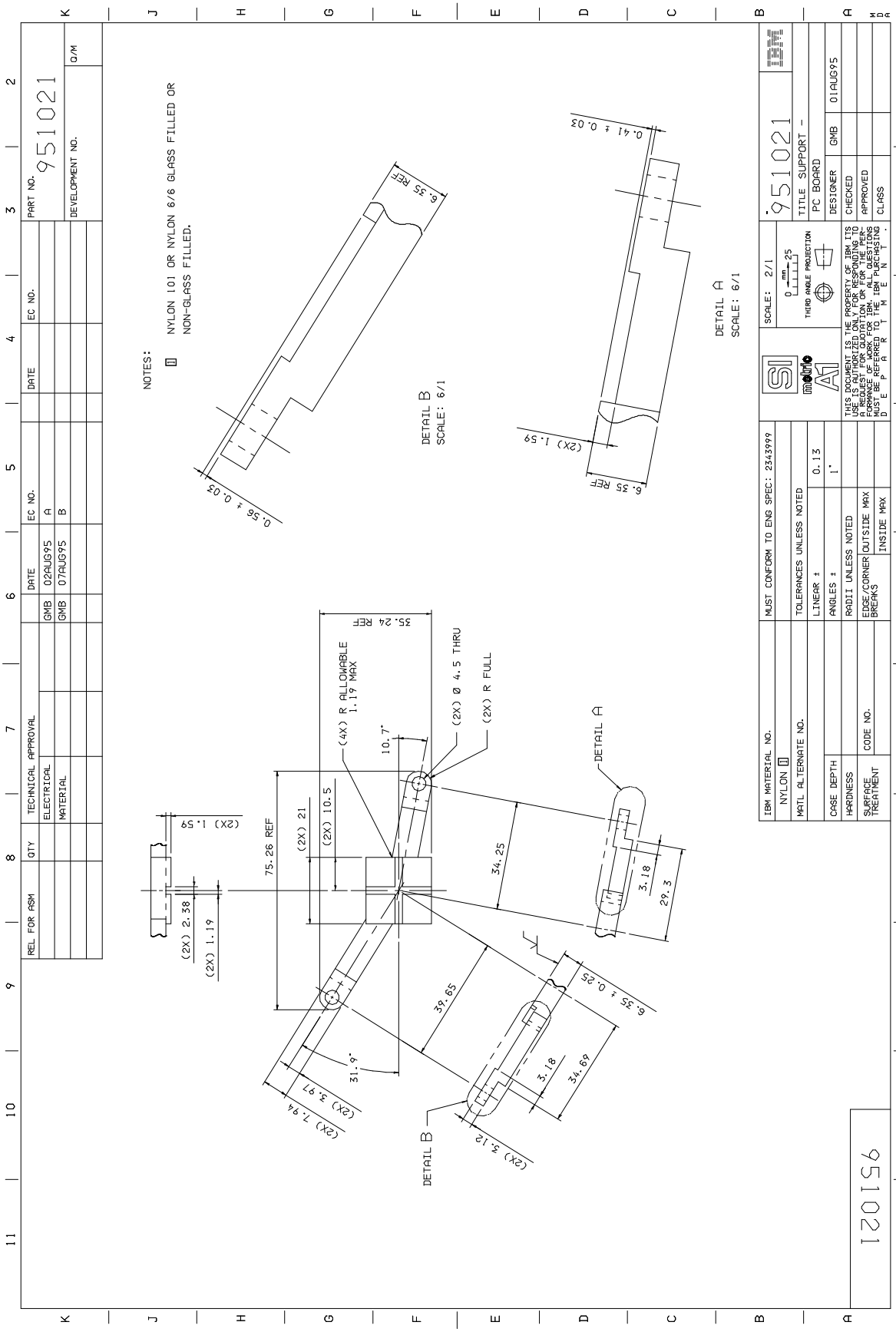
NOTES:
1. NYLON 101 OR NYLON 6/6 GLASS FILLED OR NON-GLASS FILLED.
DETAIL B
SCALE: 6/1
DETAIL A
SCALE: 6/1
DETAIL A
DETAIL B
75.26 REF
(2X) 21
(2X) 10.5
(4X) R ALLOWABLE 1.19 MAX
10.7°
(2X) Ø 4.5 THRU
(2X) R FULL
35.24 REF
34.25
39.65
31.9°
3.18
29.3
6.35 ± 0.25
34.69
(2X) 7.94
(2X) 3.97
(2X) 3.12
(2X) 2.38
(2X) 1.19
(2X) 1.59
0.56 ± 0.03
6.35 REF
0.41 ± 0.03
(2X) 1.59
6.35 REF
REL FOR ASM
QTY
TECHNICAL APPROVAL
ELECTRICAL
MATERIAL
DATE
EC NO.
GMB 02AUG95 A
GMB 07AUG95 B
PART NO. 951021
DEVELOPMENT NO.
Q/M
IBM MATERIAL NO.
NYLON 1
MATL ALTERNATE NO.
CASE DEPTH
HARDNESS
SURFACE TREATMENT
CODE NO.
MUST CONFORM TO ENG SPEC: 2343999
TOLERANCES UNLESS NOTED
LINEAR ± 0.13
ANGLES ± 1°
RADII UNLESS NOTED
EDGE/CORNER BREAKS
OUTSIDE MAX
INSIDE MAX
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0 mm 25
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