PowerPC

Preliminary, 8–14–96

Longtrail Reference Design Specification for Pass 2 (A CHRP-Compatible Reference Design) Version 0.1

Note: This document is a very rough preliminary version of the Longtrail reference design. Its purpose is to provide general guidance to engineers and programmers for the development of the Longtrail system.

This document changes frequently. It is the user's responsibility to obtain the latest version. The most currently released version is available on:

afs — cd to /afs/awd/work/PowerPC/reference_designs/longtrail
and copy the postscript file: ltspec 8_5.ps
or the most recently dated (e.g., 8_5) version.

ftp://ftp.austin.ibm.com
/pub/PPC_support/reference_designs/longtrail/spec

Howard Tanner
(512)838-5794
htanner@vnet.ibm.com
IBM Microelectronics

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IBM ®

Contacts

International Business Machines Corporation:
IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531
Tel: (800) PowerPC

World Wide Web Address:
http://www.chips.ibm.com
http://www.ibm.com

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Documentation
PowerPC 603e RISC Microprocessor Hardware Specification
PowerPC 603e RISC Microprocessor Technical Summary
PowerPC 603/604 RISC Microprocessor Hardware Specification
PowerPC 603/604 Reference Design Technical Specification
IBM PowerPC 603/604 Reference Board Design Files (on 8mm tape)
IBM PowerPC 604 Reference Board Mfg. Data Files (in Gerber format)
IBM14N1372 Data Sheet
IBM11D4360B Data Sheet
Motorola MPC970 Data Sheet
Altera 5130 Data Sheet
Integrated Device Technology IDT71216 Data Sheet

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About This Book

Difference between Pass 1 and Pass 2

This document describes pass 2 of the Longtrail reference design. Appendix A gives a complete summary of the the changes from pass 1. Highlights of those changes are as follows:

- Processor card replaced with a PGA
- VRM card added for voltage regulation
- Autoconfigure PAL replaced with jumpers or a configuration key card
- New silicon (pass 2)
- COAST, 160-pin L2 replaces 182 pin L2
- Some interrupts are reassigned
- A low cost clock chip is used
- Debug probe support changed to an industry-available component
- Audio changed to CS4236 standard and CS4232 optional
- Target for 2S2P (4 layer) board.

Design Team

Architecture
Gary Tsao and Howard Tanner

Applications Engineer
Robert Marshall

Board Design
Binh Hoang and Chong Nguyen

Engineering Manager
Steve Curtis

Project Business Manager
Scot Hallman

Peripherals and Special Circuits
Keith Braithwaite

Software Interface
Mike Stafford and John Dickol

1 Overview

Longtrail is a reference design provided by IBM to enable PowerPC OEM customers to easily build CHRP-compatible desktop uniprocessor PPC systems using the VLSI chipset. It may be cloned or modified. Major features of the design are:

- ATX form factor (9 in. x 12 in.) board with one full–length ISA slot, three full–length PCI slots, and one full–length shared PCI/ISA slot.
- Fully populated 17x17 PGA ZIF socket for 604, 603e, 603e-Valiant, 604e-Sirocco, or 604-Helmwind processors in a variety of frequencies.
- System bus operation up to 66MHz. The actual frequency depends of the frequency of the processor selected. Frequencies supported on the motherboard are 50, 55, 60 and 66 MHz.
- One 40-pin Voltage Regulation Module (VRM) with voltage output range from 2.1 to 3.5V (existing industry-available VRM).
- Option for auto or manual configuration using 20–pin key card or 13 on–board jumpers. Configuration parameters include: VRM voltage, CPU/PCI bus frequency, CPU PLL ratio, 603 or 604 processor family.
- PCI bus operation up to 33MHz. The PCI bus frequency is always 1/2 of the CPU bus frequency.
- Three 168-pin JEDEC standard DIMM sockets for standard 3.3v non-buffered DIMMs. Supports up to 192 M using 16 M DRAM technology. Supports up to 768M using 64M DRAM technology. EDO, burst EDO, and FPM are supported. Parity or non-parity are supported. Two single or double-bank JEDEC standard SDRAMs are supported.
- Socket for an industry standard L2 cache card. Uses an 160-pin connector containing 512K pipelined or synchronous burst L2 cache. Other cache cards may be designed to operate in this socket.
- Socket for MAC ROM card. 4 M flash or burst ROM. Uses 160 pin connector.
- CHRP compliant audio subsystem on motherboard comprised of a Crystal Semiconductor CS4236 chip and 3.5mm stereo jacks for line-in, line-out, microphone, earphone, and game port connector. Wave table and a 3D sound connectors are included. Connectors are provided to support CS4232 chip plus external FM synthesis if necessary.
- Support for:
  - 512K boot code connected behind the ISA bridge

  - 8 K or 32 K NVRAM connected behind the ISA bridge
  - RTC with password protect
  - Standard IBM compatible I/O — 2 serial, 1 parallel (IEEE 1284 extended capabilities) port
  - PS2 Keyboard/mouse
  - Floppy disk, 1/2/4M with media sense — autoeject or PC
  - Apple I/O — ADB keyboard/mouse, 2 SCC serial ports, 1 MESH SCSI
  - IDE — Two channels with up to two devices per channel
    - Bus master capability on DMA drives
    - PIO modes 0–4 and multiword DMA modes 1–3
  - Hardfile light driver
  - Power good light driver
  - Password override switch or jumper
  - Manual reset button
  - Boot flash update with lockout
  - MAC ROM flash update with lockout
  - Speaker connector and tone generation via ”timer 2”
- Energy Star power management
  - Hibernate mode only (energy star)
  - Suspend mode with limited power reduction (may not achieve energy star)
- Designed for operation with
  - Either standard or power–managed power supplies
  - Either standard or auto eject floppies
- Supports software controlled power-down. OEMs may choose to connect a normally-open push button at one or both of the following 2-pin headers:
  - Immediate on/off (independent of software state)
  - Immediate on/no off function – (Apple power switch function)
    (May be software-configured for software-controlled power-off request).

2 Reference Design Offering

The following items comprise the reference design offering and may be ordered separately:

1. A documentation package comprising specifications for the motherboard and all plugable items, schematics for the motherboard and all plugable items, bill–of–materials for the motherboard and all plugable items. The package will include copies of the following:

   CHRP Specification

   Macintosh Technology in CHRP

   Up to date references for all major documents.

   The documentation package will also include a book or section outlining how to use the firmware development kit. It will also include flow charts, checkpoint reference listings and other aids to understanding, debugging, and modifying the firmware. This package will be authored by the firmware supplier.

2. Motherboard equipped with:

   1 – 32M, 10 ns SDRAM DIMM

   1 – Cache card with 512 K pipelined burst SRAM

   1 – 3.3v 4M Flash MAC OS ROM card (Later ships may have burst ROM rather than flash)

   1 – VRM card

   1 – Boot ROM with open firmware boot code and RTAS compatible with NT, MAC OS 7.5 and MAC OS 8.0

   1 – 512K pipeline burst L2 card

   1 – Documentation package.

3. The processors listed in Table 1 are supported in the design:

Table 1. Supported Processors

Processor	100 MHz	120 MHz	133 MHz	150 MHz	166 MHz	180 MHz	200 MHz	233 MHz	266 MHz
603e	X	X	X						
603e-Valiant				X	X	X	X		
604			X	X	X				
604e-Sirocco				X	X	X			
604e-Helmwind							X	X	X

4. A complete system is outlined in Table 2. This offering includes the documentation package.

Table 2. Quickstart Peripheral List

Description	Manufacturer
Processor	Helmwind 604e or Valiant 603e
L2 Cache	512KB Pipelined Burst
Memory DIMMs	3.3V, 10ns SDRAM
Memory Total	32MB or more
Video adapter card	ATI XClaim (PCI)
Hard Disk Drive	Quantum Fireball2 1.2GB (IBM P/N 41H6956
Floppy Disk Drive	Sony MPF520–7 or Mitsubishi MF 355F–3792–ME
CD ROM Drive	TEAC–6X (IBM P/N 06H9430)
Audio	Controller: Crystal 4236 Wave Table Cardlet: Yamaha Waveforce DB50XG 3DO Cardlet: Philips Incredible Sound ISH 9022 588 00001
Chassis	Palo Alto Design Group ATMT–ATX Mini Tower
CPU Fan (if necessary)	Panaflow FBA08T12M
Power Supply	Seasonic SS–200GPX, 200W, w/internal fan
Keyboard	Interex Products Mac–105A (ADB) or IBM PS/2 Compatible
Mouse	Interex Products Mac–100A (ADB) or IBM PS/2 Compatible
Modem	U.S. Robotics Sportster Voice for Macintosh Computers Model #1141 (28.8 / 33.6) (external) or U.S. Robotics Sportster (IBM) Computers (28.8 / 33.6) (internal)

5. RISCWATCH support package

   A package of documentation will be prepared for each processor offered indicating sources of RISCWATCH product and code for each processor. The form and delivery mode of this package is not yet clear. The intention is to make it easy for the customer to find and obtain the tools necessary for debug.

6. Design tapes

Cadence and/or Gerber design tapes are available on a special request basis.

2.1 Operating Systems

Longtrail will be ported to operate with MAC OS 7.5, CHRP release and NT 4.0. AIX and any other "shrink wrapped" OS that follows the CHRP guidelines should operate, but no testing is planned to validate other OSs. Table 3 shows operating system availability dates.

Table 3. Operating System Projected Availability Date

OS	alpha	beta	ship
NT 5.0	4-96	7-96	11-96
MacOS 7.5 CHRP	8-96	12-96	3-97
MacOS 8.0	?	?	?

2.2 Open Firmware Boot Code (OF)

The supplied OF boot code includes support for the following cards (see Table 4).

Table 4. Supported Options

Video Cards	ATI Exclaim S3 Trio
SCSI Cards	Adaptec AHA2940
Ethernet Cards	3COM EtherLink III DEC 21140
Token Ring Cards	IBM xxxx

2.2.1 Support for Network Boot

The boot code will support network boot from ethernet and token ring.

2.2.2 Support for Performance Tuning

An additional feature supported in the boot code is the capability of breaking into a memory controller/system tuning mode during boot. This capability allows designers to alter all IDE, memory controller, and bridge chip parameters that affect performance. Menu screen(s) are presented.

Specific items that may be tuned via the GUI interface include the following:

- All memory timing parameters
- L2 cache behavior such as write back policy
- ROM timings
- GGII characteristics that affect performance.
- ISA bridge buffer control and other factors that affect performance
- IDE parameters that affect performance.

2.2.3 DIMM Support

The OF will support DIMMs that ship with or without EEPROM. In the case of no EEPROM, the OF will use cut–and–try probe methods to determine the amount and type of memory present. This is similar to methods used in X86 BIOS. If EEPROM–equipped DIMMs are found, the OF will determine the characteristics of the memory (including the number of DRAM modules) from the EEPROM, and it will use a computational algorithm to set the memory controller optimally for the speed and type of memory present. If both EEPROM and non EEPROM DIMMs are present, the OP will not be able to take advantage of the computational algorithm.

2.3 Device Drivers

The OSs will support at least the following add–in cards (see Table 5).

Table 5. Add–In Support by OS

Card	MacOS 7.5	NT
ATI Xclaim Graphics	yes	yes
S3 Trio Graphics	yes	yes
Adaptec AHA2940 SCSI	yes	yes
3COM EtherLink III	yes	yes
DEC 21140 Ethernet	yes	yes
IBM xxxx PCI Token Ring	yes	yes
xxxx ISA Modem	no	yes
xxxx ISA Modem	no	yes
xxxx ISA Modem	no	yes

2.4 Debug Support

IBM will not directly offer any probe tools. Vendors provide those found in

Table 6. Vendor Provided Tools

Item	Vendor	Product
PGA probe aid	HP	HP 2465A PowerPC 604 PGA Preprocessor Interface
	TBD	TBD
Memory probe card	TBD	TBD
	TBD	TBD
PCI probe and aids	TBD	TBD
	TBD	TBD

3 Motherboard Specification

3.1 Purpose

This specification is primarily written to define the software interface in enough detail so that the Open Firmware (OF) boot code and the Real Time Abstraction Services (RTAS) may be written. The primary sources of information are the manufacturers data books and various other documents listed below. This document does not attempt to give the total software interface. It does outline the way the various chips are, or must be, configured and provides information not found in the data books. All information, such as registers unique to this motherboard, is provided; however, code writers are required to consult the references for most information and consult this specification for exceptions, special cases, power-on configuration strappings, etc.

Later versions of this specification will be expanded to include all hardware interface pin descriptions, timings etc.

3.2 Reference Documentation

Boot code writers will need all of the following documents:

Golden Gate II Functional Specification 0.8.4 or later. This document is available under non–disclosure from VLSI. Contact Kevin Mankin at (408) 434–7532.

Tollgate Functional Specification. Available from the same source as above.

Symphony Labs SL82C565 Data Book. publication number 2562 Version A.6 or later. Available from Symphony Labs (408) 986–1701.

National PC 87C308VUL Data Book. September 1995 version or later. Available from National Semiconductor Corporation.

PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture (aka CHRP version 1.0 or later) ISBN 1–5560–3948. Available from Morgan Kauffman Publishers. 1–800–745–7323.

Macintosh Technology in the Common Hardware Reference Platform. ISBN 1–55860–393–X. Available from Morgan Kauffman Publishers 1–800–745–7323.

PowerPC Microprocessor Common Hardware Reference Platform: I/O Device Reference — Version 1.0 or later, author Lee Wilson, IBM Austin. This book defines the programming interface for all standard CHRP hardware.

IC Works W49C65–01 Clock chip data book. Available from IC Works (408) 992–0202.

Hydra ERS—Hydra chip specification from Apple Computer (if available).

NM24C02L Serial EEPROM data sheets available from National Semiconductor Corporation.

Open PIC Multiprocessor Interrupt Controller Register Interface Specification, Revision 1.2 from Don McCauley, IBM Corporation.

Intel 82378ZB SIO Chip Data Book. This chip is not used, but the data book provides a useful reference when other data books are not clear

Crystal Semiconductor Data books for CS4232 and CS4236 Audio chips.

8 Byte Unbuffered DIMM Product Overview from the IBM Microelectronics memory products group in Burlington Vermont or via the WWW.

168 Pin Unbuffered SDRAM DIMM Overview from the IBM Microelectronics memory products group in Burlington Vermont or via the WWW.

ISA PNP Standard IEEE publication	xxxx.
OF Specification	xxxx.
PowerPC binding to the OF specification	xxxx.
CHRP binding to the OF specification	xxxx.
PCI binding to the OF specification	xxxx.
ISA binding to the OF specification	xxxx.
PNP binding to the OF specification	xxxx.

NOTE: Open Firmware information, relating to IEEE Std 1275–1994 can be reviewed via the World Wide Web:

http://playground.sun.com/1275/
or
http://chrp.apple.com/1275/

3.3 Chipset Overview

Figure 1 is a block diagram of the Longtrail motherboard showing how the major components are interconnected.

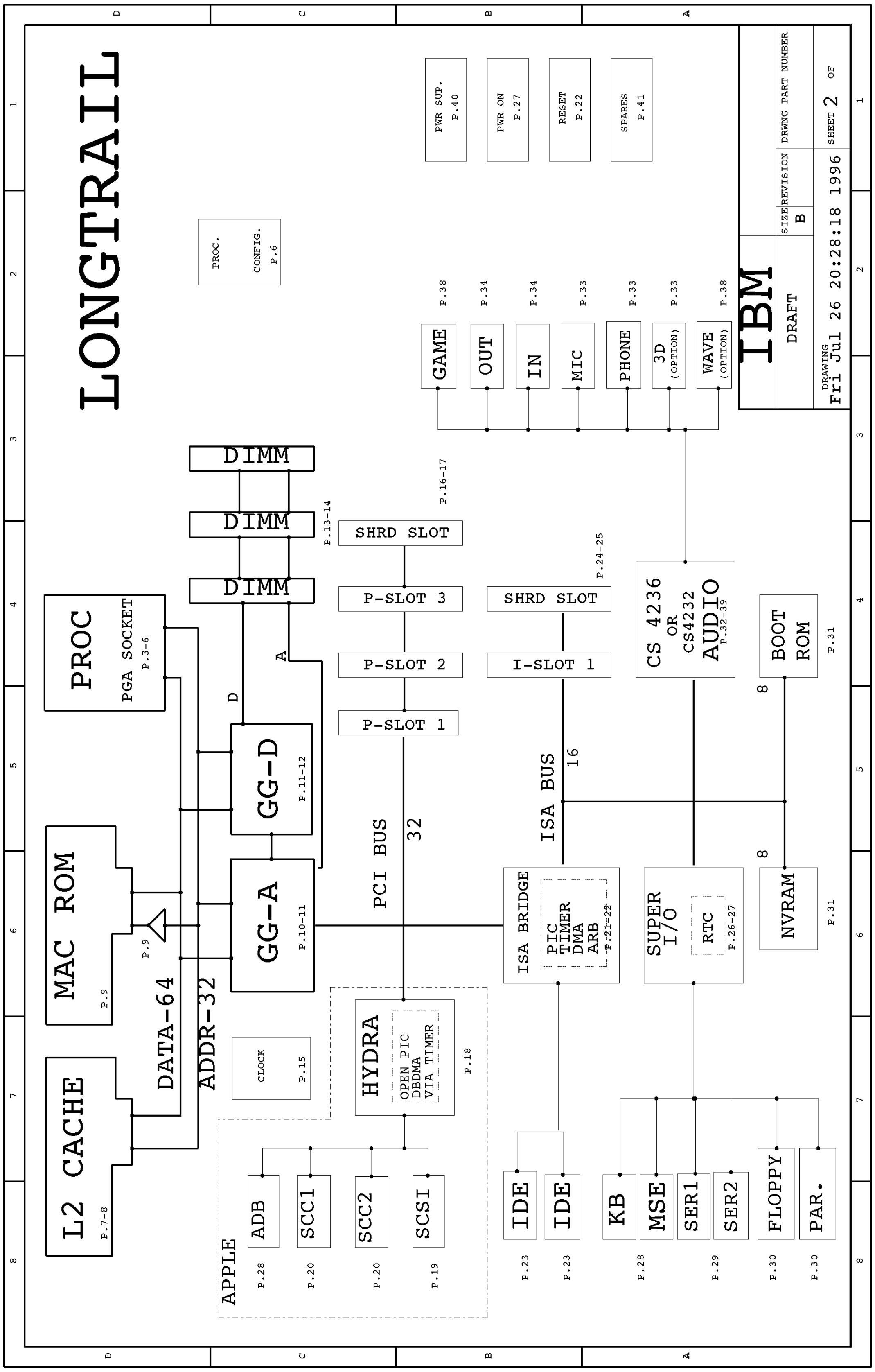

Figure 1. Motherboard Block Diagram

The chipset on the motherboard comprises the following:

- VLSI Golden Gate II

  This two–chip set provides the memory control and PCI bus bridge function. It is CHRP compatible and also provides a PReP map mode.

- ISA Bridge

  This chip may either be the Symphony Labs 82C565 or the VLSI Tollgate (TG). These parts are nearly pin compatible.

  The motherboard has optional resistor sites and wiring so that either chip may be used with appropriate changes in the way that the board is populated. The configuration programming models are different. Boot code supports both and tests to determine which chip is present.

- SuperIO

  The National Semiconductor PC308VUL is utilized. It provides the RTC, FDC, two serial ports, one 1284 parallel port, keyboard controller, and mouse controller. It also has power management functions which are used in the Longtrail power management logic. Currently there is no plan to utilize the infrared (IRDA) capability. Longtrail will not block the ability to add IRDA capability.

  The following version of the National part is available:

  - PC87308VUL–IBN contains KB/MSE code licensed by Phoenix.

- Hydra (Available from VLSI or TI)

  The Hydra chip designed by Apple provides control for all of the Apple I/O (2 SCC ports, ADB port, and SCSII port). It also includes the Open PIC controller. It connects to the PCI bus. The cache indicator two–wire interface is used as an I2C controller.

- CS4236 Audio — Crystal Semiconductor

An audio subsystem is included. Sites for a FM synthesizer are included on the board if a regression to the 4232 controller is necessary. Connectors for wave table and 3-D sound upgrade cardlets are also provided.

3.4 General Firmware Programming Considerations

3.4.1 Abstractions in CHRP

Two levels of abstraction are inherent in the CHRP specification. The first is open firmware. This is the boot code. It builds an open firmware description of the topology and capabilities of the host board in main memory. Theoretically any OS can read and interpret the OF description. The OS programming interface for all I/O supplied on the motherboard is fixed and defined in CHRP.

The second abstraction is RTAS. This is code that resides in boot ROM and can be executed during run time. It abstracts certain elements such as NVRAM, power management, and such, which are platform specific. The OS need only make RTAS calls to execute some functions in a platform independent way. This is a low–level BIOS–type function.

3.4.2 MAC OS 7.5, CHRP release

In general, MAC OS 7.5, CHRP release, expects the OF to configure and tune the platform for fastest operational modes before handing over control. There are a number of elements which must be configured according to the capabilities of the particular hardware device that is connected. For example the IDE must be configured differently if the drive supports DMA than if it does not, even though the chip may support either. This may be true for devices attached to Hydra. In the case of the printer, it should be the responsibility of the OS to talk to the attached device in the fastest mode that it can support, but it is not necessary to reconfigure to chip since the programming interface supports various modes.

3.4.3 Real–Time Abstraction Services (RTAS)

RTAS is a type of low–level BIOS. It controls various functions such as indicator light control and power control. This allows platforms to use various ”hacks” to save money in hardware by, for example, using the general purpose I/Os provided in the chip set. Table 12 on page 99 of the CHRP level 1.0 specification lists required and optional RTAS calls. In general, Longtrail RTAS attempts to utilize the native capabilities of the chips without extra hardware. Longtrail is dependent on RTAS. Any OS that does not use the RTAS interface will require more modifications in the HAL layers in order to run on Longtrail.

Table 7 describes which particular RTAS calls are supported in Longtrail hardware.

Table 7. RTAS Call Supported in Longtrail Hardware

restart–rtas	Comment
nvram–fetch	supported
nvram–store	supported
get–time–of–day	supported
set–time–of–day	supported
set–time–for–power–on	supported
event–scan	supported
check–exception	supported
read–pci–config	supported
write–pci–config	supported
display–char	supported
set–indicator	supported
get–sensor–state	?
set–power–level	supported
get–power–level	supported
assume–power–management	?
relinquish–power–management	?
power–off	supported
hibernate	supported
suspend	not supported ?
system–reboot	supported
cache–control	supported
freeze–time–base	not supported
thaw–time–base	not supported
stop–self	not supported
start–cpu	not supported

//??//Author's note: More description of how support is achieved is needed.

3.5 Memory Subsystem

This section describes the memory subsystem in detail.

3.5.1 Memory Capacity

Longtrail has three 168–pin 3.3v DIMM slots. It accepts JEDEC–standard 3.3V 168–pin unbuffered DIMMs. Slots 1–3 may be populated with any combination of single or double bank FPM, EDO, or Burst EDO DIMMs in all available memory sizes. Slots 1–2 may be populated with any combination of single or double banks SDRAM DIMMs in all sizes available. SDRAM may not be mixed with any other kind of memory. Slots 1–2 are wired in preparation for the latest (4clk & 2 CE pin) JEDEC standard. The maximum memory capacity is shown in Table 8 and Table 9.

Table 8. Uncached Memory Capacity — FPM or EDO

DRAM Tech	Chips/bank	Cap with Single Bank	Cap with Double Bank
1Mb X 4	16	24 M	48 M
16Mb X 1	n/a	n/a	n/a
4Mb x 4	16	96M	192 M
2Mb x 8	8	48M	96 M
16MB x 4	16	384M	768 M
8MB x 8	8	192M	384 M

Table 9. Uncached Memory Capacity — SDRAM

DRAM Tech	Chips/bank	Cap with Single Bank	Cap with Double Bank
1Mb X 4	16	16 M	32 M
16Mb X 1	n/a	n/a	n/a
4Mb x 4	16	64 M	128 M
2Mb x 8	8	32 M	64 M
16MB x 4	16	256 M	512 M
8MB x 8	8	128 M	256 M

3.5.2 Open Firmware Memory Features

OF makes the following checks and automatic adjustments:

1. Check for more memory than can be cached. Turn caching off to prevent non-coherency.
2. Check for SDRAM mixed with other types. Do not enable memory. Signal operator to change.
3. Configure the best refresh mode for the type of memory installed.
4. Set memory timing registers for the best possible timing settings considering the number and type of DIMMs installed (see Section 3.18.7).
5. A GUI interface is provided which allow experimenting with memory and cache features.

3.5.3 Memory Performance

TBD

3.5.4 Mixing Memory DIMM Speeds and Sizes — FPM and EDP

The GGII memory controller allows assignment of memory type and timing registers on a bank by bank basis. However, there are only two timing registers, Also the bank selects (RAS#) signals are wired as follows:

- Bank 0 and Bank 1 to Memory slot 1 (closest to processor)
- Bank 2 and Bank 3 to Memory slot 2 (middle)
- Bank 4 and Bank 5 to Memory slot 3 (farthest from processor).

From a practical point of view, the Longtrail board has the following population restrictions:

1. There may be at most two different kinds (type or speed) of DIMMs installed.

2. There are no restrictions on which slots may have which DIMMs, other than slot 3, which may not have SDRAM.
3. SDRAMs may never be mixed with other DIMMs.

3.5.5 Parity Memory

TBD

3.6 L2 Cache Card

Long Trail has a 160 pin connector to support industry standard L2 cards built to the COAST specification.

3.6.1 Connector Type

The connector is the ”FX” type as defined in the COAST specification. It can physically accept any of the defined COAST types.

3.6.2 Acceptable L2 Cards

Table 10 indicates the supported cache types and their respective presence detect bits. Presence detect bits are reported in the 308 GPIO register, bits [27:29].

Table 10. Cache Support

Cache	Supported	PD(3) (GPIO 27)	PD(2) (GPIO 26)	PD(1) (GPIO 25)	PD(0) (GPIO 24)
256/async	No*	1	0	0	1
512/async	No*	0	0	0	1
256 burst	yes	1	1	1	0
256 pipe burst	yes	1	1	1	1
512 burst	yes	0	1	1	0
512 pipe burst	yes	0	1	1	1
512 2 bank pipe burst	yes	0	1	0	0

Note: *OF reports if this unsupported cache type is installed.

Caches may have 5v or 3.3v tagRAM outputs but may only have 3.3v dataRAM outputs.

Caches must support the linear burst order option when pin #114 is grounded.

3.6.3 11-Bit and 8-Bit Tag

The GGII chipset has support for both 8-bit tagRAM and 11–1bit tagRAM cache modules. See the GGII specification for the protocol required to determine tag size. The presence/absence of the 11th tag bit is reported in the 308 GPIO register, bit 1–16.

One tag line is dedicated to a DTY bit; so an 8-bit tag module only uses seven address tags, and an 11-bit module only uses 10 tag bits.

3.6.4 Cached Memory Capacity

Cached memory capacity is limited by the number of tag bits available and by the logic used in GGII to allow caching of MACROM space. It is also reduced slightly because one pattern is used by an invalid indication. See Table 11.

Table 11. Cacheable Memory

	With MACROM Cached		W/O MACROM Cached	
Size	**8-bit Card (7 tag + DTY)**	**11-bit Card (10 tag + DTY)**	**8-bit Card (7 tag + DTY)**	**11-bit Card (10 tag + DTY)**
256	*	?	*	?
512	48,640K	?	65,280K	?
1024 (future potential)	114,432K	?	130,816K	?

Note: * Not useable.

3.6.5 Cache Card Sources

The manufacturers listed in Table 12 offer cache cards that operate in Long Trail.

Table 12. Cache Card Sources

Manufacturer	Contact	Models
TBD	TBD	TBD

3.7 VRM Cards

Long Trail uses the same industry-standard, 40-pin VRM cards as specified for Pentium Pro™ systems.

OEMs may choose from a variety of cards from various manufacturers in order to satisfy current requirements of the target processors. Table 13 lists suitable VRM cards.

Table 13. VRM Card Sources

Manufacturer	Contact	Current	Models
TBD	TBD	TBD	TBD

3.8 IDE Subsection

The IDE logic is implemented in the ISA bridge.

CHRP specifies that the IDE operate in the PCI Native mode. Both the 565 and the Tollgate present the same run-time programming interface when they are configured as defined in the configuration sections that follow. IDE itself is configured as any PCI device and, therefore, details are not presented here. In order to keep a common programming interface between 565 and Tollgate, CHRP specifies that only multiword DMA-compatible drives can be used.

IDE speeds for multiword DMA transfers are as follows:

Mode 0 = 4.16M/sec.
Mode 1 = 13.33M/sec.
Mode 2 = 16.66M/sec.

3.9 Physical Slot Numbering Scheme

User visible slots are numbered beginning with slot 1 on the left as viewed from the rear of the machine (see Figure 2). Slot 5 accommodates an ISA card; slot 4 is a shared slot, and slots 1-3 accommodate full or half size PCI cards.

Designator On Motherboard	J1	J2	J3	J4,J5	J6
Utilization	PCI–1	PCI–2	PCI–3	Shared ISA–2 or PCI–4	ISA–1
Identifier On Enclosure	S1	S2	S3	S4	S5

Figure 2. Slot Diagram (Viewed from rear of enclosure)

3.10 ISA Bus I/O Address Assignments

The term ”ISA bus I/O address assignments,” as used in this section, refers to all I/O addresses (0–64K), which the host bridge generates on the PCI bus, if they are claimed by the ISA bridge — whether the cycle is seen on the physical ISA bus or not. From the CPU point of view, these addresses are memory mapped from a base that depends on the memory map type selected and whether the discontinuous I/O feature is active.

3.10.1 CHRP-Mode ISA Base Addresses

The base for memory-mapped CPU load/store addresses to use when GGII is set for CHRP memory map and has the peripheral memory alias option enabled is shown in Table 14.

Table 14. CHRP-Mode ISA Base Addresses

Space	Base	PCI Address Seen
ISA I/O	0xF800 0000	0x0000–0xFFFF (0–64K–1)
ISA Memory	0xF700 0000	0x0000–0xFFFFFF (0–16M–1)

3.10.2 Hierarchy of Claiming ISA Bus I/O Addresses

The hierarchy of claiming ISA bus I/O cycles when the host bridge generates an ISA bus I/O address is as follows:

1. Any PCI device may be programmed to claim the cycle. In this case it will not be seen by the ISA bridge or any device down stream.
2. The ISA bridge itself may claim the cycle. In this case it will not be seen by any device downstream. For example all DMA, timer, and 8259 PIC registers are intercepted by the ISA bridge. Complete listings are contained in the device data books. Configuration register settings affect which cycles are claimed.
3. The ISA bridge may claim the cycle and, depending on how it is configured, pass it to ISA, but with an expected response on the XD bus.
4. All cycles not intercepted cause ISA bus cycles to run. The National PC87308VUL chip used in Longtrail is ISA PNP compatible. Therefore all of the devices such as the serial ports contained within it may be programmed to respond to offsets from separate 16–bit base registers. It is necessary for configuration code to assign addresses to the devices in the ’308 that do not conflict with each other or with addresses of ISA plug-in cards.

3.10.3 Recommended ISA Address Assignments

The National ’308 chip allows complete flexibility, subject to the hierarchy mentioned above, in assigning I/O addresses to all of its functions. If only PNP devices were to be supported, then the boot code could assign addresses as it will; however, it is suggested that the addresses be assigned as shown in Table 15 for the following reasons:

1. Older ISA cards may do only 10 bit decodes. This means they may alias the addresses and respond in every 1k of address range.
2. The PC community is very familiar with the ”traditional” assignments for the standard I/O within the ’308. There is no need to create confusion during debug.

Table 15 shows the base that should be used to obtain the base for each of the 9 functions within the ’308 in order to preserve traditional I/O addresses.

Table 15. Recommended ISA Address Assignments for 308 Logical Devices

Function	Logical Dev#	Traditional Address(es)	Base	Comment
KBC	0	0x0060	0x0060	
MOUSE	1	0x0064	0x0064	
RTC/APC	2	0x0070	0x0070	
FDC	3	0x03F0	0x03F0	
PAR PORT	4	0x0278	0x0278[1]	
Serial 2/IRR	5	0x02F8	0x02F8	
Serial 1	6	0x03F8	0x03F8	
GPIO	7	N/A	0x0800	GPIO2 = 0x0804
Power Manage	8	N/A	0x0850	
CS0#	—	N/A	0x0840	Not used
CS1#	—	N/A	0x0830	Not used
CS2#	—	N/A	0x0820	Floppy Eject Reg.

Note:

1. This may be changed. See the hardware reference note on page 83 of the CHRP I/O Reverence, Version 1.0.

3.11 Interrupt Assignments

3.11.1 Open-PIC

The open–PIC controller is located within the Hydra chip. It is strapped to be active and it operates as the interrupt master. This means that it is configured such that ISA (8259) interrupts cascade to channel 0 of the Open–PIC controller. The code need only interrogate the Open PIC controller to determine the interrupt source on channels 1–19. If an interrupt is found on channel 0, the code must also run an interrupt acknowledge cycle on the PCI bus to interrogate the 8259–PIC.

Open PIC is programmed as a PCI device within Hydra. Since Longtrail is a uniprocessor system, all interrupts must be directed toward CPU 0 (pin 112). The PCI interrupts are defined by Table 16.

Table 16. PCI Interrupts

Level	Pin#	Name	Assignment	Comment
0	113	Slotint	Cascade from 8259 PIC	Not useable for I/O
1	N/A	SCSI DMA		Fixed in Hydra[1]
2	N/A	SCC TxA DMA		Fixed in Hydra[1]
3	N/A	SCC RxA DMA		Fixed in Hydra[1]
4	N/A	SCC TxB DMA		Fixed in Hydra[1]
5	N/A	SCC RxB DMA		Fixed in Hydra[1]
6	N/A	SCSI Device		Fixed in Hydra[1]
7	N/A	SCC A Device		Fixed in Hydra[1]
8	N/A	SCC B Device		Fixed in Hydra[1]
9	N/A	VIA		Fixed in Hydra[1]
10	N/A	ADB		Fixed in Hydra[1]
11	N/A	ADB_NMI		Fixed in Hydra[1]
12	115	Extint1	PCI Slot w[2,3]	
13	117	Extint2	PCI Slot x[2,3]	
14	119	Extint3	PCI Slot y[2,3]	
15	120	Extint4	PCI Slot z[2,3]	
16	121	Extint5	IDE Primary/ Secondary[4,5]	
17	122	Extint6	IDE Secondary[4,5]	
18	123	Extint7	Power off req.	
19	—	Spare	—	

Notes:

1. Hydra does not conform to the PCI standard for interrupt assignments. Special interrupt manager code will be required in the OSs.
2. User visible slots are numbered beginning with slot 1 on the left as viewed from the rear of the machine. Slot 5 accommodates an ISA card; slot 4 is a shared slot, and slots 3–1 accommodate PCI cards.
3. The PCI slot interrupts are wired as recommended in PCI, level 2.1 as shown in Table 17. This assignment allows more efficient processing when only single-function adaptors are present, since each IRQ is assigned to a different open PIC level
4. Both IDE interrupt signals are converted to negative level–sensitive and connected to IRQ16. This corresponds to the current CHRP definition of IDE as a single native–PCI device. IRQ17 should be disabled. The OF may easily be modified to configure the primary IDE interrupt to IRQ16 and the secondary to IRQ17 if CHRP redefines this aspect. In this case, IRQ17 should be enabled.
5. The ISA bridge must be configured to present the IDE interrupts to the Open–PIC controller and by–pass the 8259 PICs. The IDE interrupts are physically wired to the ISA bridge chip because they are required for the IDE function. They emerge from the bridge chip on pins 18 and 19, and connect to the Open-PIC controller.

Table 17. PCI Slot Interrupt Wiring

Open PIC Level	Name	Connectors
12	Slot w	Slot 1 – IRQA, Slot 2 – IRQD Slot 3 – IRQC, Slot 4 – IRQB
13	Slot x	Slot 1 – IRQB, Slot 2 – IRQA Slot 3 – IRQD, Slot 4 – IRQC
14	Slot y	Slot 1 – IRQC, Slot 2 – IRQB Slot 3 – IRQA, Slot 4 – IRQD
15	Slot z	Slot 1 – IRQD, Slot 2 – IRQC Slot 3 – IRQB, Slot 4 – IRQA

3.11.2 ISA Interrupt Assignments

The National PC87308VUL chip used in Longtrail is PNP compliant; therefore, all devices within it that need interrupts may be configured to any interrupt level except IRQs 0 & 2. It is recommended that ”traditional” interrupt levels be used wherever possible because the PC community is familiar with these. The dual–8259 PIC is located in the ISA bridge and it is programmed in ISA I/O space.

Table 18 defines the Longtrail ISA interrupt system.

Table 18. Longtrail ISA Interrupt Assignments

IRQ Level	Assignment	Type[2]	ISA Pin #	Comment
0	Timer 0	Low Level	None	Internal Conn
1	KB[1]	Edge	None	
2	Cascade	Edge	None	Internal Conn
3	Serial 2[1]	Edge	B25	
4	Serial 1[1]	Edge	B24	
5	Audio-Base[3]	Edge	B23	
6	Floppy[1]	Edge	B22	
7	Parallel[1]	Edge	B21	
8	RTC[1]	Low Level	None	
9	Audio-MIDI[3]	Edge	B04	
10	ISA Slot	Edge	D03	
11	ISA Slot	Edge	D04	
12	Mouse[1]	Edge	D05	
13	S/G Complete	Edge	None	
14	ISA Slot		D07	see Table 16
15	ISA Slot		D06	see Table 16

Notes:

1. These devices may be configured to any IRQ 2–15 or IRQ 1 in the National PC8708VUL chip. This capability may be used to resolve conflicts if an ISA card cannot be configured otherwise.
2. This column shows the configuration setting required for the ISA bridge and within the 308.
3. The audio chip may be configured to use IRQ 5, 7, 9, 11, 12, or 14.

3.11.3 Architectural Note Relating to Interrupts

As far as the author is aware there is no architectural tie–in between the interrupt signaling and the buffers within ISA bridge chips. It may be possible that a device can signal end–of–transfer via an interrupt and data could still be posted in buffers within the ISA bridge or possibly the PCI bridge. This is not unique to Longtrail or CHRP, but it is mentioned here as a caution.

3.12 ISA DMA Assignments

The DMA assignments for Longtrail are defined in Table 19.

Table 19. Longtrail ISA DMA Assignments

Level	Assignment	Size	ISA Slot	Notes	Comments
0	Audio-Base and Soundblaster	8 bit	Yes	1,3,6	
1	Par Port-ECP	8 bit	Yes	1,2	
2	Floppy	8 bit	Yes	1,5	
3	Audio-Base and Soundblaster	8 bit	Yes	1,3,6	
4	Cascade	N/A	No	2	Not Usable
5		16 bit	Yes	4	
6		16 bit	Yes	4	
7		16 bit	Yes		

Notes:

1. The only DMA wiring on the motherboard is 1:1 wiring between the ISA slots, the audio chip, the ’308, and the ISA bridge. The National ’308 chip may be configured for DMA on floppy, ECP, and serial port 2 using PNP registers. The PNP configuration registers support configuration of this device to any DMA channel, but these devices are 8-bit only.
2. The Extended Capabilities Parallel port may be configured to DMA channels 1, 2, 3. The PNP configuration registers support 0:7 but only 1, 2, or 3 will function. Channel 1 was chosen at random as a recommendation.

   Boot code should configure the ECP to use a DMA channel even if the ECP mode is not initially used in order to reserve the resource.
3. It appears from the ’308 specification that serial port 2 is capable of using one or two DMA channels. No channels are available.
4. It is suggested that the audio card be configured to use these channels.
5. This is the traditional floppy DMA assignment.
6. Audio is wired to DMA channels 0, 1, and 3. It is an 8-bit device.

3.12.1 ISA DMA Programming Considerations

Scatter–gather DMA operations are supported on both the SL82C565 and on VLSI’s Tollgate only for the 16–bit channels.

Boot code should determine the best capabilities of any attached devices and configure the DMA channels as appropriate.

3.13 ISA Master and ISA Memory Card Support

Both ISA bridge chips have registers which may be programmed to locate both ISA DMA and ISA master–generated memory cycles on ISA or the PCI bus. All ISA DMA or ISA master memory cycles are forwarded to main memory via the PCI when the configuration settings are as shown in the ISA bridge configuration sections. OF will probe the ISA bus or use other methods to determine the presence of ISA memory cards and/or ISA master cards. If such cards are present, then OF will change the ISA–to–PCI mapping registers in the 565 or Tollgate as appropriate for the card(s).

The Longtrail board has the following characteristics relative to ISA memory cards and ISA Masters:

1. ISA memory located anywhere from 1M to 15M may be accessed by the CPU via PCI.
2. The ISA bridges may be configured so that ISA DMA or ISA masters can access either the ISA memory cards or main memory via PCI at these addresses. They may also access main memory via PCI using address 0–1M or 15–16M. There are some restrictions. See the user's guide(s).
3. If an ISA memory card is located at 15M to 16M, damage could occur because both the ROM and ISA card would respond when ROM is read.
4. No ISA memory card should be configured below 1M because these addresses are used by NVRAM. They are not accessible by ISA DMA or ISA masters.

3.14 PCI ID Select Assignments

Type 0 PCI configuration cycles are generated by the PCI bridge chip set whenever a load or store operation is performed with an address that falls within an offset of 00800h to 07FFFh from the base of the configuration address space. The base depends on whether the CHRP or PReP map is selected. Bits 16:20 (BE notation) of the address of the load or store instruction select the device for configuration as defined in Table 20.

Table 20. Longtrail PCI ID Select Assignments

Value of Bits 16 : 20 (BE notation)	Active PCI AD Line for ID Select	Device Receiving ID Select	CHRP Map PPC Base
0	None	GGII Chip Set	0xFEC0 00XX
1	AD17	ISA Bridge	0xFEC0 08XX
2	AD18	Hydra Chip	0xFEC0 10XX
3	AD19	PCI Slot 1, Machine Slot 1	0xFEC0 18XX
4	AD20	PCI Slot 2, Machine Slot 2	0xFEC0 20XX
5	AD21	PCI Slot 3, Machine Slot 3	0xFEC0 28XX
6	AD22	PCI Slot 4, Machine Slot 4	0xFEC0 30XX
7...15	AD23...31	None	—
8...31	None	N/A	—

3.14.1 PCI Arbitration

Both the Hydra chip and the ISA bridge chip contain PCI arbiters. Longtrail uses the arbiter in the ISA bridge. OF must never enable the Hydra arbiter.

Boot code should configure the arbiter in the ISA bridge to operate in whatever is determined to be the best performance mode for desktop applications.

3.15 Presence Detect for DIMM

The DIMM specifications dictate the use of a 2–wire I2C interface to provide information about the type of DIMM installed in each socket. A National Semiconductor NS24C02L Serial EEPROM is installed on each DIMM. This device provides 256 bytes (max) of serial information. Up to eight of the 256–byte devices may be supported on one I2C interface.

The Hydra chip contains a 2–wire interface controller. Software controls the state of the two wires by writing to a register within Hydra (which must be configured using PCI protocol first). The bit rate is determined by how fast the software changes the register. The board is wired such that the data wire is common to all DIMMs, and the clock wire is common to all DIMMs. The controller is called a cache indicator and is described beginning on page 25 of the Macintosh Technology in CHRP book. Hydra pins 136, 137, 138, and 140 are pulled high on the board so that the 2–wire interface can function. Pin 136 is the I2C clock pin and pin 137 is the I2C data pin.

Table 21. I2C control register in Hydra — Offset 000030h

Bit Number (Notation?)	7	6	5	4	3	2	1	0
Comment	0	0	data output enable	clk output enable	X	X	data pin 137	clk pin 136

An EEPROM is selected when the broadcast address matches the 3–bit static code coded via pullup or pulldowns on the pins of the DIMM connector (see Table 22). These pins connect to address pins on the EEPROM. If a device does not respond to its broadcast address it may be assumed to be absent.

Table 22. EEPROM Codes

Code	Use
0	Reserved
1	DIMM SLOT 1
2	DIMM SLOT 2
3	DIMM SLOT 3
4	DIMM SLOT 4 (Not used in LT)
5	DIMM SLOT 5 (Not used in LT)
6	DIMM SLOT 6 (Not used in LT)
7	Reserved

3.15.1 Protocol for Serial EEPROMs

The protocol which must be implemented by software is defined in the National Semiconductor Data Sheets for part NM24C02L.

Note: If software elects to write the EEPROMS, the write protocol must be one that is common to all vendors. The write protocol described for the NM24C02L is not supported by all vendors.

3.15.2 EEPROM Coding for DIMMs (Set by DIMM standards)

This information is defined in documents titled *8-Byte Unbuffered DIMM Product Overview* and *168 Pin Unbuffered SDRAM DIMM Overview* from the IBM Microelectronics memory products department in Burlington, Vermont or from JEDEC. **Caution:** This standard may be volatile. Consult with the memory department or JEDEC for the latest data. Also, the timing information in the EEPROM may not be used directly because it is necessary to consider the timings of chip and board when programming the memory controller. See Sections 3.18.7 and 3.18.8 for information on programming the memory controller. We will consider having a table of adders which may be applied directly to the timing information from the EEPROM.

3.16 NVRAM

Longtrail provides 32K of NVRAM reducible to 8K. It does not use the conventional PC port 74/75/77 protocol; instead, the NVRAM is mapped in ISA memory space.

NVRAM may be accessed using 60x load and store instructions just like any ISA memory. Loads and stores of 1, 2, or 4 bytes may be used, and the ISA bridge will assemble or disassemble, as necessary, to access the 8-bit, battery-backed, SRAM device.

If accesses greater than 1 byte are made, software must compensate for endian-mode, byte-lane switches made in the PCI bridge.

3.16.1 NVRAM Decoding (CHRP-Mode Address 0xF70E0000 to 0xF70E7FFF)

NVRAM accesses are partially decoded by the ROMCS signal generated by the ISA bridge. The details are slightly different for the 565 and Tollgate, but the principle is the same. ROMCS is generated for addresses that occur when BOOT ROM or NVRAM is accessed via the PCI. BOOT ROM accesses alias to 15-16M in ISA space. Accesses to NVRAM space produce ISA bus addresses of 0xE0000 to 0xE7FFF. External logic differentiates the target. The NVRAM is actually mapped into a traditional X86 BIOS location.

The differences in the 565 and Tollgate implementations are in the way the chips are configured by OF to enable ROMCS# for this region. This is explained in the relevant chip configuration section.

3.16.2 NVRAM Lockout in RTAS

NVRAM should only be accessed through RTAS. In order to prevent errant code from modifying NVRAM, OF must disable the ROMSC decode for the NVRAM areas. The RTAS enables it only during RTAS use. This can be accomplished as shown in Table 23.

Table 23. NVRAM Access Protection Method

ISA Bridge	Method
565	Set chip select control register (PCI configuration, index 0x4D bit 5):[1] 1 = NVRAM access open 0 = NVRAM access disabled.
Tollgate	Reset Pulse control register (PCI configuration, index 0x62 bit 7): 1 = NVRAM access open 0 = NVRAM access disabled.

Note:

1. The current specification has these bits incorrectly reversed.

NVRAM is accessed using load or store instructions. Addresses are calculated using the following formula:

NVRAM_ADDR = PCI_MEMORY_BASE + OFFSET_ISA +NVRAM_DISPL

= 0xF70E 0000 + NVRAM_DISPL (for CHRP)

Where:

- PCI_MEMORY_BASE is the base of the region that the GGII decodes for PCI memory. The base depends on the map type selected in GGII.
  CHRP → 0xF700 0000 PREP → 0x8000 0000.
- OFFSET_ISA is the base of the region that the ISA bridge decodes for ROWCS (OxE0000).
- NNRAM_DISPL is the target address in NVRAM.

3.17 Timer, Tone Generation (Speaker), and ISA Refresh

The ISA bridge contains a 3–channel timer. It is programmed in the manner conventionally used in PC systems. Longtrail makes no particular requirements on the programming. The 14.31818 MHz signal on the OSC pin of the ISA bridge is internally divided by 12 to produce a 1.193 Mhz clock to drive the counter logic. The following are noted for reference.

3.17.1 Speaker Tone — Timer 2

The speaker tone and on/off state are controlled by timer 2 and by ISA port 0061h. The SPKR output of the ISA bridge is controlled by these ports. Longtrail drives the speaker pins via this signal.

3.17.2 ISA Refresh — Timer 1

Setting up the ISA bridge to support the ISA_REFRESH# signal which is sourced from the ISA bridge chip is required. Some ISA memory cards require a periodic refresh signal. The ISA bridge utilizes a timer channel and an ISA bus arbiter to provide refresh when the ISA bus is free and timer 1 has requested. ISA bandwidth and response time could be improved if the refresh were programmed not to occur, but some ISA memory cards and some other ISA plug in cards may not function. Having an ISA memory card on any desktop CHRP box is unlikely, but not precluded in the architecture.

Timer channel 1 should be programmed to provide a request for refresh approximately every 15 microseconds.

3.17.3 IRQ 0 — Timer 0

Timer 0 is internally connected to IRQ 0. PC systems conventionally use this interrupt for time-keeping and time-out functions. The SL82C565 chip provides a capability to configure IRQ 0 on the internal 8259 PIC to be driven from timer 0 or from an external pin labelled ”IRQ0”. The function is available when the ’565 is used in Longtrail. See index register 4Eh; however, Longtrail does not wire any interrupt to the ”IRQ0” pin on the ISA bridge. Software should configure timer 0 to IRQ0.

3.18 Golden Gate II (GG II) Programming Considerations

3.18.1 GGII Power–on Strappings

The GGII chip set power–on behavior is determined by pullup and pulldown resistors attached to the chip–to–chip bus pins (see Table 24). These are wired as in the table that follows: Also, refer to table 52 in the GGII specification.

Table 24. GGII Power–on Default Controls

Pin	Pulled Up/Down	Register Bit Value	Default
GGD 10	up	1	Enables the PPC bus arbiter on GGA to function
GGD 9	up	PCI_SYNPPC = 1	PCI clock is synchronous to CPU clock
GGD 8	down	ADDR_BDGNO = 0	Host bridge is HB number 0
GGD 5	down	ROM_EN1=1	Enables access to boot ROM via PCI on power-on (Disables ROM on CPU bus)

3.18.2 HID Register Set–up Requirements to Operate with GGII

In order to operate properly with GGII, certain bits in the HID registers must be programmed to operate in a certain way. Table 25 and Table 26 define the requirements that GGII puts on each processor:

Table 25. Longtrail Processor HID0 Resister Requirements

HID0 bit	603e	604	604e Sirocco	604e Helmwind	Function Required
0		1 **Table TBD**			Enable MCP pin should be set after GGII error register and remainder of system is configured
2		0			Disable address bus parity check
3		0			Disable data bus parity check
7		0			Enable restore on ARTRY# and SHD#[2]

Notes:

1. It is not clear how to disable TEA#. If you figure it out , do it. GGII does not drive TEA#. It is pulled up on the board.
2. GGII needs to restore these signals when it drives them.

Table 26. Longtrail Processor HID1 Resister Requirements

HID1 bit	603e	604	604e Sirocco	604e Helmwind	Function Required
X					
X			Table TBD		
X					
X					

3.18.3 Configuration Settings Required for GGII

There are a large number of registers in GGII that must be initialized before operation can commence. Refer to the GGII specification for a full description of each. When the system first comes on it runs from ROM with default (slowest) timings. Hardware strappings configure the ROM to the PCI (actually ISA) bus.

This section summarizes only those things the programmer needs to know about the unique Longtrail hardware in order to set the GGII into an efficient running mode. These are summarized in Table 27.

The GGII registers are well documented. Only register bits requiring change from default or special mention are shown in Table 27.

Table 27. GGII Registers Requiring Change from Default or Special Mention

Offset	Length	Bit Num[1]	Field Name	Default	Set to	Comment
0x0004	16	8	SERREN	0	1	Enable SERR#
0x0004	16	6	PERREN	0	1	Enable PERR#
0x0004	16	1	MERMEN	0	1	Enable PCI Mem space
0x000D	8	7:3	LATENCY	0	X	Experiment to find best value – OF GUI
0x000D	8	2:0	LATENCY	0	X	Experiment to find best value – OF GUI
0x0042	8	7:0	DISCON TMR	0x00	0x00?	Leave disconnect disabled
0x0050	32	28	PPC_ACKDLY	1	0	Never use a 603X in less than 2:1 mode
0x0050	32	27	PPC_SNTYP	0	X	X=0 for 603x X=1 for 604X
0x0050	32	25:17	PPC_TIMEOUT	511d	0?	Disable timeout
0x0050	32	16	PPC_LE	0	0	0 while OF runs Set to 1 or 0 before loading the OS
0x0050	32	0	PPC_ARBEN	1	n/a	Set by strap
0x005C	32	28:1	ADDR_TEM	XXX	XXX	Set according to requirement of OS being loaded
0x005C	32	16	ADDR_PCEMUL	0	X	Set according to requirement of OS being loaded
0x005C	32	5	ADDR_DISCISA	0	X	Set according to requirement of OS being loaded
0x005C	32	4	ADDR_MALIAS	0	1	Must be a 1 for ISA bridge
0x005C	32	3	ADDR_PRO-HOLE	0	X	Set according to requirement of OS being loaded
0x005C	32	2	ADDR_IOHOLE	0	X	Set according to requirement of OS being loaded
0x005C	32	1	ADDR_BDGNO	0	0	Set by strap HB=0
0x005C	32	0	ADDR_PREP	0	X	Set according to requirement of OS being loaded 0=CHRP 1=PREP

Table 27. GGII Registers Requiring Change from Default or Special Mention (Continued)

Offset	Length	Bit Num[1]	Field Name	Default	Set to	Comment
0x0060	32	31	PCI_SYNCPPC	1	1	Set by strap Synchronous PCI clk
0x0060	32	29:28	PCI_FBSIZE	XX	XX	This is don't care FB feature not abstracted for CHRP use
0x0060	32	27:18	PCI_FBBASE	XX	XX	This is don't care FB feature not abstracted for CHRP use
0x0060	32	17	PCI_MRGEN	0	0	FB feature not abstracted for CHRP use
0x0060	32	16	PCI_CMBEN	0	0	FB feature not abstracted for CHRP use
0x0060	32	13	PCI_SN	1	1	Never change this
0x0060	32	12	PCI_PARDDRF	0	0?	FB feature not abstracted for CHRP use
0x0060	32	11	PCI_MRDPRFF	0	1?	Enable memory prefetch Experiment with this using GUI in OF
0x0060	32	10	PCI_MWRPOST	1	1?	Enable memory write post from PCI Experiment with this using GUI in OF
0x0060s	32	9	PCI_LE	1	0?	PCI and Mem LE bits should always be same 0 while OF runs Set to 1 or 0 before loading the OS
0x0060	32	4:3	PCI_RTRYNO	2	255d	?
0x0064	32	29:16	PCI_ECGBASE	XXXX	XXXX	Configure this if the Graphics cable is present See GPIO register
0x0064	32	0	PCI_ECGSHDW	1	X	Set this to 1 if the Graphics cable is present.
0x0070	32	32:24	ROM_SHDWSZ	0xXX	0xXX	?????
0x0070	32	12:11	ROM_WDTH1	0b10	0b10	Set with strap to 64 bits
0x0070	32	10	ROM_WE1	0	1?	Meaningful when ROM on PCI ??
0x0070	32	9:8	ROM_MODE1	0b00	0b00	Set with strap ROM on PCI bus
0x0070	32	4:3	ROM_WDTH0	0bXX	0b10	Set for 64 bit MAC ROM
0x0070	32	2	ROM_WE0	0	0	Set during write to MAC ROM
0x0070	32	1:0	ROM_WE0	0b00	0b01	Set to enable MAC ROM

Note: 1. Endian notation, indicated by MSb on left; varies by register

3.18.4 Programming the ROM_TIME Resister – Offset 0x0074

Longtrail is hardware–configured to use BOOT ROM on the ISA bus, accessed via the PCI bus. Therefore the ROM1 timing bits on the ROM_TIME register are not meaningful. The timings for accessing this ROM are discussed in the sections on ISA bus configuration settings. The timings for the MAC ROM are controlled by the ROM0 fields in the ROM_TIME register.

There are two possible speed versions for the MAC ROM. There is no presence detect to determine which, if any, MAC ROM is attached. Its presence may be detected by looking for meaningful patterns at the assigned addresses. OF will provide versions for each ROM speed. Speeds are:

1. Apple 3.3v FLASH ROM design using AMD 29LV800-120SC components. This version may be used during the development phase when pass2 GGII chips are available. The access time is 120ns.
2. Apple–specified burst ROM production boards. The access time is 120ns on beat 0 and 60ns on beats 1–3.

In order to achieve best possible performance, the values for ROM_TIME must be calculated using a formula that considers the cpu bus clock rate, the ROM timing parameters and the GGII AC timing parameters. OF will optimize these values. The formulas are given in Table 28, and a summary is given in Table 29. Values are tentative until GGII timings are finalized. The symbol ”RU” stands for a round–up calculation (i.e., round up to nearest integer).

Table 28. Formulas for Calculating ROM Timing Values

Value	Formula
ROM_T2ND0	RU [(AT + GG_OUT_A + PPC_SU + 10) / (CPU_BUS)]
ROM_TACC0	RU [(AS + GG_OUT_CS + PPC_SU + 5) / (CPU_BUS)]
ROM_TOFF0	RU [(TZ + GG_OUT_CS + 5) / (CPU_BUS)]

Notes:

1. AT is the device address access time in ns
2. AS is the device chip select address time in ns
3. GG_OUT_A is the GGII clock–to–ROM address (pin 164,165) out AC timing in ns
4. GG_OUT_CS is the GGII clock to ROMCS# AC timing in ns
5. PPC_SU is the PPC data setup time in ns
6. 10 is a factor in ns to allow for signal propagation and buffer delay
7. 5 is a factor in ns to allow for signal propagation delay
8. CPU_BUS is the cpu bus clock period in ns (20,16.6, or 15)
9. TZ is the CS to High Z specification of the device
10. RU is a round up function.

Results of tentative calculations are summarized in Table 29 for three device types and three CPU bus rates.

Table 29. ROM_TIME Register (0X0074) Values in Clocks – Convert to Bit Format

Parameter	Apple Flash Pass 2	Production Rom
ROM_T2ND0	50 60 66	50 60 66
ROM_TACCO	? ? ?	5 5 6
ROM_TOFF0	? ? ?	1 2 2

3.18.5 GGII Endian Mode Controls

There are three bits which control the endian–mode behavior of Longtrail. One is the MSR(31) LE mode bit of the processor. Two bits are located in GGII configuration space. The major reason for having two bits is to allow a mixed endian mode. For example with one setting a program in BE mode could have the byte–swap performed in hardware when it reads a LE hardware register rather than use byte–swap instructions. If the same mode setting is in effect when it begins transfer of data to a hard file (more than 1 byte at a time) the bytes will be swapped out of the desired BE order.

Also this function is not supported in the OF descriptors at present. It will be necessary to get this capability into the OF tree if the OSs wish to take advantage.

When the endian mode switch is performed both endian bits in GGII should be switched to the corresponding state. They are in different registers (0050 and 0060) so precautions against accidental mixed mode operation will be necessary.

3.18.6 Mixed Endian Mode At Reset

Caution: GGII resets to a state with PPC_LE indicating BE mode and PCI_LE indicating LE mode. The 60x processor resets to BE mode.

It is suggested that the OF set the PPC_LE bit in GGII to indicate BE mode before any other operations are started. This can be accomplished as follows:

1. Do a one-byte read to address 0xFEC00052 to get the default value.
2. Turn off the low-order bit (PPC_LE).
3. Write the result back to 0xFEC00052.

Other changes to this register may be required, but this will put the system in a consistent BE state. When the system is in BE mode, any fixed multi-byte register must be accessed using load/store with byte reverse instructions.

3.18.7 Programming the GGII Memory Controller

This section defines how to program the memory controller and memory timing registers for various DIMMs, taking into account DIMM specifications, loadings, and GGII chip timings.

RTAS Note: Longtrail is designed to operate at the maximum possible speed with a lightly loaded system. Certain combinations of DIMMs (e.g., three double bank DIMMs) may not operate reliably with faster memory timings. It is a requirement on RTAS to adjust memory timing for the fastest reliable operation, considering the number and type of DIMMs installed.

Guidelines are included in this section. TBD

3.18.8 SDRAM Programming

This section contains instructions for programming SDRAMs.

TBD

3.18.9 8/11-Bit Tag Determination

The algorithms for initializing the cache controller are in the GGII specification. GGII can support 7, 8, 9, or 10-bit cache tags; however, the COAST specification supports only 8 and 11-bit cache tags. The COAST presence detect bits do not identify the number of tag bits. GGII has defined a method where it writes a 0 to tag(10) and then holds the tag output enable active. Tag(10) is isolated and wired to GPIO bit 1-6. The OF must interrogate GPIO 1-6 while the cache is in this setup mode. A 0 indicates that tag(10) is implemented; otherwise, an 8-bit tag is indicated.

3.19 Programming Requirements for the Symphony Labs SLC 82C565

3.19.1 Power–on Strappings for the Symphony Labs SL82C565

Table 30 defines how the Symphony Labs part is strapped for power–on configuration and the resulting defaults:

Table 30. Power–on Strappings for the Symphony Labs SL82C565

Pin Number	Pin Name	Pulled	Default Condition
16	ARBDIS#	hi 27k	Enables the arbiter in the 565.
13	PCI5TH#	hi 27k	Enables the FLUSHREQ/MEMACK pins and disables the optional arbitration request/grant pair function associated with these pins.
8	POWERPC/ X86	hi 27k	Configures for PowerPC mode. Pin 119 becomes ROMCS PCI addresses FFF0 0000 to 4 G activate ROMSC in addition to X86 Boot Addresses (not used in CHRP. Pin 118 becomes chip select for ports 0800-08FF. Pin 3 becomes IRQ 0 Pin 4 becomes HRESET# (host reset). Pin 5 becomes ISARST. Pin 22 becomes PCIRST#. Pin 116 is read into port 92 at power-on. Registers behave as described for PowerPC, mode.
86	NAT/LEG#	hi 27K	The IDE bus master controller comes up in native PCI mode.

3.19.2 Configuration Settings Required for the Symphony Labs SL82C565

This section describes how configuration registers must be set in order to operate with the board as used in Longtrail. Refer to the user’s guide for a complete description of registers and bits. This section only describes settings required by Longtrail.

3.19.2.1 Setting the PCI Configuration Space Registers – 565 ISA Bridge (Function 0)

These registers should be initialized as indicated in the Table 31.

Table 31. Setting the PCI Configuration Registers—565 ISA Bridge

Name	Size	Index	Default	Set to	Comment
Vendor ID	16	0x01–00	0x10AD	n/a[1]	R/O
Device ID	16	0x03–02	0x0565	n/a	R/O
Command	16	0x05–04	0x0207	0x0047	Set PCI parity error PERR# check Other bits R/O
Status	16	0x07–06	0x0200	n/a	—
Rev ID	8	0x08	0x00	n/a	R/O
Class Code	24	0x09–0B	0x060100	n/a	R/O
HDR Type	8	0x0E	0x80	n/a	R/O
PCI Cntl	8	0x40	0x20	0x27	Enable posted writes Enable retries Enable NMI on PCI error Experiment using GUI n OF to find best performance
S/G Base Hi	8	0x41	0x04	n/c[2]?	S/G base at 0x0410 Author is not clear on how S/G relocation works.
Line Bfr Cntl	8	0x42	0x00	0x22	Ping–pong packing Experiment using GUI in OF to find best performance.
IDE Int Route	8	0x43	0xEF	n/c	IDE interrupts routed to Open PIC, don't cares here
PCI Int Route	16	0x44–45	0x0000	n/c	PCI interrupts routed to Open PIC, disabled here
BIOS Timer Base	16	0x47–46	0x0078	n/c	Not used; make sure address does not conflict
ISA To PCI Cntl	8	0x48	0x01	0xFF	Forward all ISA Master cycles to PCI
ISA ROM Deal	8	0x49	0x00	0xFF	Forward all ISA Master cycles to PCI
ISA2PCI Hole	8	0x4A	0x00	n/c	Forward all ISA Master cycles to PCI
ISA2PCI Hole Sz	8	0x4B	0x00	n/c	Forward all ISA Master cycles to PCI
Clock Divisor	8	0x4C	0x00	0x0X	X=1 if CPU Bus=50 Mhz X=0 otherwise
Chip Sel Cntl	8	0x4D	0x33	0x40	Enable NVRAM CS decode 0XE0000 Write protect NVRAM Disable others

Table 31. Setting the PCI Configuration Registers—565 ISA Bridge (Continued)

AT System Cntl1	8	0x4E	0x04	0x64	Enable port 92 IRQ0 = Timer 0 disabled ISA Refresh enabled
AT System Cntl2	8	0x4F	0x00	n/c	Normal ISA timing
IRQ Break Evnt0	8	0x60	0x00	n/c	Not available in PPC Allocate as reserved
IRQ Break Evnt1	8	0x61	0x00	n/c	Not available in PPC Allocate as reserved
Add Break Evnt	8	0x62	0x00	n/c	Not available in PPC Allocate as reserved
DMA Break	8	0x63	0x00	n/c	Not available in PPC Allocate as reserved
PCI Arb Cntl0	8	0x80	0xE0	n/c	Experiment for best perf. using GUI in OF
PCI Arb Ext	8	0x81	0x01	n/c	Experiment for best perf. using GUI in OF
PCI Arb Enh	8	0x82	0x02	n/c	Experiment for best perf. using GUI in OF
PCI Arb Cntl1	8	0x83	0x80	0x83	Experiment for best perf. using GUI in OF
PCI Min Gnt 1	8	0x84	0x00	n/c	Experiment for best perf. using GUI in OF
PCI Min Gnt 2	8	0x85	0x00	n/c	Experiment for best perf. using GUI in OF

Notes:
1. n/a = not applicable.
2. n/c = no change required.

3.19.2.2 Configuring the DMA Controller I/O Space Registers

See applicable CHRP documentation. These registers are standardized in the CHRP I/O Reference.

3.19.2.3 Configuring the PIC Controller I/O Space Registers

See applicable CHRP documentation. These registers are standardized in the CHRP I/O Reference.

The edge/level registers must be set consistently with the settings in the National 308 and with other interrupt sources (see Table 32).

Table 32. Interrupt Edge/Level Control Registers – Tollgate ISA Bridge

Name	Size	Address	Default	Set to	Comment
PIC 1 E/L	8	0x04D0	0x00	0x??	I cant tell what the spec means
PIC 2 E/L	8	0x04D1	0x00	0x??	I cant tell what the spec means

These registers should set all interrupts to high edge sensitive, except IRQ 0,8 are low level sensitive.

3.19.2.4 Configuring the Counter/Timer Registers in I/O Space

CHRP does not specify the use of the counter/timer. However the device must be configured so that ISA refresh will function as it normally functions in X86 machines.

3.19.2.5 Configuring Miscellaneous 565 ISA Bridge I/O Space Registers

The following registers should be initialized as shown in Table 33.

Table 33. Configuring Miscellaneous 565 ISA Bridge I/O Space Registers

Name	Size	Address	Default	Set to	Comment
Port B	8	0x0061	0x00	0x03	Enable IOCHK error Enable SERR error
70 Shadow	8	0x0070	0xxx xxxx	1xxx xxxx	Enable NMI out
Port 92	8	0x0092	0x24	n/c[1]	Not needed on Longtrail Allocate as reserved
Coprocessor	8	0x00F0	0x??	n/c	Not used Longtrail Allocate as reserved
RTC Protk1	8	0x0810	0xXX	n/a[2]	Not used Longtrail Allocate as reserved Note 3
RTC Protk2	8	0x0812	0xXX	n/a	Not used Longtrail Allocate as reserved Note 3

Notes:

1. n/c = no change required
2. n/a = not applicable
3. If the RTC is configured at port 70, these ports will function as described in the user's guide when the 565 is used; however, the ports do not exist in Tollgate. OF should not use these ports. It is suggested that OF use extra NVRAM in the RTC to catalog protected locations if necessary. OF should not use these port addresses for another function.

3.19.2.6 Setting the 565 PCI Configuration Space Registers – IDE (Function 1)

Refer to the 565 user's guide page 109 for the IDE bus master configuration registers. Important things to remember are:

1. Only the IDE bus master (PCI native) mode may be used. The legacy mode cannot be used for operating systems. Pin 86 is pulled low during reset in order to select PCI native mode.
2. Only multi–word DMA mode drives may be used. Do not use base address 5 (offset 0x24–27).
3. Configuration registers are not visible to the OSs; therefore, OF interrogates the attached drive(s) to determine their speed capability and it sets configuration timing parameters in an optimal way for the drives that it finds. The OF in Longtrail does not use the most common denominator(lowest speed) approach.
4. Longtrail hardware does nothing special to limit or change the IDE capabilities of the chip.
5. Certain parameters must be set as shown in Table 34.

Table 34. Setting the IDE Function 1 Control Registers – 565 ISA Bridge

Name	Size	Index	Default	Set to	Comment
Vendor ID	16	0x00–01	0x10AD	n/a[1]	R/O
Device ID	16	0x02–03	0x0105	n/a	R/O
Command	16	0x04–05	0x0000	0x0125	Bit 0 strapped to Native mode Enable Bus Mastering Enable PERR & SERR check
Status	16	0x06–0	0x0280	n/c[2]	—
Rev ID	8	0X08	0x05?	n/a	R/O Revision varies
Prog Intf	8	0x09	0x8?	0x8F	Select Native for primary Note 2 Select Native for secondary
PCI Base	8	0x0A	0x01	n/a	R/O
PCI Subclass	8	0x0B	0x01	n/a	R/O
Cache Line	8	0x0C	0x08	n/c	32 Byte
Latency Tmr	8	0x0D	0x08	n/c	Note 5
Hdr Type	8	0x0E	0x80	n/c	R/O
Reserved	8	0x0F	0x80	0x??[3]	n/a
Pri Base 0	32	0x10–13	0x000001F1	0xXXXX XXXX[4]	Set to locate drive in PCI space
Pri Base 1	32	0x14–17	0x000003F5	0xXXXX XXXX	Set to locate drive in PCI space
Sec Base 0	32	0x18–1B	0x00000171	0xXXXX XXXX	Set to locate drive in PCI space
Sec Base 1	32	0x1C–1F	0x00000375	0xXXXX XXXX	Set to locate drive in PCI space
Base Add 4	32	0x20–23	0x00000001	0xXXXX XXXX	Set to locate in PCI space for multiword drives
Base Add 5	32	0x24–27	0x00000001	0xXXXX XXXX	Do not use this register. Using it would not yield CHRP–compatible program model.
Reserved	32	0x28–3B	0x00000000	n/a	n/a
Int Line	8	0x3C	0x0E	n/c?	IRQ14 is not used. How to override?
Int Pin	8	0x3D	0x01	n/c?	RQ14 is not used. How to override?
Min Gnt	8	0x3E	0x02	n/a	R/O
Max Latency	8	0x3F	0x28	n/a	R/O
Contl/Status	32	0x40–43	Bits 26:16	0xXXXX XXXX	Note 5
			Bit 11 = 0	1	Route Int to Open PIC via INTC# pin. Note 6
			Bit 5 = 0	1	Note 7
			Bit 1 = 0	1	Note 7

Table 34. Setting the IDE Function 1 Control Registers – 565 ISA Bridge (Continued)

Name	Size	Index	Default	Set to	Comment
Port0/Drv0	32	0x44–47	0x???? ????	0xXXXX XXXX	Note 8
Port0/Drv1	32	0x48–4B	0x???? ????	—— XXXX	Note 8
Port1/Drv0	32	0x4C–4F	0x???? ????	—— XXXX	Note 8
Port1/Drv1	32	0x50–53	0x???? ????	—— XXXX	Note 8

Notes:

1. n/a = not applicable
2. n/c = no change required
3. ? = data not found or author uncertain
4. X = varies with conditions
5. Experiment with this value to determine best performance. It is controllable in the OF GUI.
6. Bit P1N/L# should be set to 1 to route both PCI interrupts to Open PIC via the IRQC# pin. P1N/L# is in index 0x09.
7. It may be necessary to have this bit set to 0 while the drives are interrogated for capability. Drives should be set for the best performance of the slowest drive found.
8. Set according to the capabilities of the device. Experiment with the read–ahead and posted write enables (via GUI in OF) to determine best performance.

3.19.3 Programming Requirements for Tollgate (Alternate chip to ’565)

Tollgate is the VLSI code name for the ISA bridge chip that complements the GGII chip set. It is pin–compatible with the 565 described above. It is configured differently and has slightly different characteristics. The major differences are:

1. Tollgate does not implement an X86 mode and it is not necessary to strap it into the PPC mode.
2. Tollgate subtractively decodes all 4G of both PCI memory and PCI I/O addresses whereas the 565 only claims the first 16M of PCI memory and the first 64K of PCI I/O. This makes no difference under normal operations, but Tollgate is less robust when the code produces incorrect addresses.
3. The method of dealing with PIO IDE drives is different. CHRP deals with this by disallowing PIO drives.
4. Configuration code is different for the two chips.
5. Tollgate supports fast back–to–back cycles. The 565 does not.
6. Tollgate has made changes to be compatible with the 565 in these areas:
   - DMA programming model
   - PIC edge–level control
   - IDE Interrupts brought out to INTC#, D#
   - Reset logic.

Refer to the user’s guide for a complete description of registers and bits. This section only describes settings required by Longtrail.

3.19.3.1 Setting the PCI Configuration Space Registers – Tollgate ISA Bridge (Function 0)

These registers should be initialized as indicated in Table 35.

Table 35. Setting the PCI Configuration Registers – Tollgate ISA Bridge

Name	Size	Index	Default	Set to	Comment
Vendor ID	16	0x01–00	0x1004	n/a[1]	R/O
Device ID	16	0x03–02	0x0703	n/a	R/O
Command	16	0x05–04	0x000F	0x0147	Set PCI parity error Set PERR# check Disable special cycle Other bits R/O
Status	16	0x07–06	0x0280	n/a	—
Rev ID	8	0x08	0x00?	n/a	R/O
Class Code	24	0x09–0B	0x060100	n/a	R/O
Reserved	16	0x0C–0D	0x0000	n/a	n/a
HDR Type	8	0x0E	0x00	n/a	R/O
BIST	8	0x0F	0x00	n/a	R/O
Misc Cntl	8	0x50	0x00	n/c[2]?	Spec may be changed here. IRQs are changed in the PIC I/O space.
Clk Cntl	8	0x51	0x1B	n/c?	Some optimization is possible by using the fast ISA clk feature but just don't do it. Note 3
Misc A	8	0x52	0x00	0x63	Enable PERR to NMI Enable SERR to NMI Enable I/O write posting Enable mem write posting Will need to experiment with posting enables and some other bits. Not sure what to do with bit 0.
DMA Cntl	8	0x53	0x04	n/c?	This register may be removed. All DMA timing should be controlled by I/O space DMA registers. I have no idea about bit 0.
PMRA1	8	0x54	0x00	n/c?	Forward all ISA master cycles to PCI. Subtractively decode ISA Setting bit 6 might violate PCI specification??
PRME1	8	0x55	0x00	n/c?	0x55 looks like 0x54 to me.
PRMA2	8	0x56	0x00	n/c?	Looks like a don't care if positive decoding is not enabled.
PRME2	8	0x57	0x00	n/c?	0x57 looks like 0x56 to me.
Bus Cntl	8	0x58	0x00	n/c	Default timing is ok. OF should allow changing this register in the GUI.
Fast Bus Region	8	0x59	0x00	n/c	Function not enabled
ROM Cntl	8	0x5A	0x00	0x40	Speed up ROM access
Reserved	8	0x5B	n/a	n/a	n/a

Table 35. Setting the PCI Configuration Registers – Tollgate ISA Bridge (Continued)

Name	Size	Index	Default	Set to	Comment
Int Assert	8	0x5C	0x00	n/c?	Spec may be changed here. IRQs are changed in the PIC I/O space.
Misc B	8	0x5D	0x01	n/c?	Function of this register is not clear to me, especially bit 3.
Reserved	16	0x5E–5F	0x0000	n/a	n/a
Arb Cntl PAC	8	0x60	0x00	n/c?	Some experimentation may be necessary to determine best performance mode for arbiter.
				0x04?	Bit 2 may need to be set.
				0x05	Bit 0 may need to be set.
Arb Cntl PAPC	8	0x61	0x00	n/c?	Some experimentation may be necessary to determine best performance mode for arbiter.
Rst Pulse	8	0x62	0x00 0x40?	n/c?	This register may be redefined in pass 2. Bit 6 to default to 1. Note that Bit 7 is a Flash write enable.
Top Address	8	0x63	0x00	n/c?	What does this do?
Reserved	—	0x64–77	0x00–00	n/a	n/a
Reserved	—	0x78–79	0x??	n/a	n/a
S/G Base	8	0x7A	0x04	n/c?	What does this do? If it breaks the programming model it must be changed.?
S/G Cntl	8	0x7B	0x00	0x07?	Experiment for best performance. Pretty sure we need GAT. Does this only affect buffers in S/G mode?

Notes:

1. n/a = not applicable
2. n/c = no change required
3. Bits 1:0 should be set as follows:

CPU BUS CLK	= 50	=> PCI = 25	=> Divisor of 3 => 8.33 MHz
	= 60	=> PCI = 30	=> Divisor of 4 => 7.50 MHz
	= 66.6	=> PCI = 33.3	=> Divisor of 4 => 8.33 MHz

Divisor 3 is not listed in the specification.

Refer to the user's guide for a complete description of registers and bits. This section only describes settings required by Longtrail.

3.19.3.2 Configuring the DMA Controller Registers in I/O Space

See applicable CHRP documentation. These registers are standardized in the CHRP I/O Reference.

3.19.3.3 Configuring the PIC Controller I/O Space Registers

See applicable CHRP documentation. These registers are standardized in the CHRP I/O Reference.

The edge/level registers must be set consistently with the settings in the National 308 and with other interrupt sources (see Table 36).

Table 36. Interrupt Edge/Level Control Registers — Tollgate ISA Bridge

Name	Size	Index	Default	Set to	Comment
PIC 1 E/L	8	0x04D0	0x00	0x??	This register being added
PIC 2 E/L	8	0x04D1	0x00	0x??	This register being added

These registers must set all interrupts to high edge sensitive, except IRQ 0 and 8, which are low level sensitive.

3.19.3.4 Configuring Miscellaneous Tollgate ISA Bridge I/O Space Registers

The following registers should be initialized as shown in Table 37.

Table 37. Configuring Miscellaneous Tollgate ISA Bridge I/O Space Registers

Name	Size	Index	Default	Set to	Comment
Port B	8	0x0061	0x00	n/c	Enable IOCHK error Enable PCI error check
70 Shadow	8	0x0070	0x0X	0x80	Enable NMI out
Port B	8	0x0061	0x00	0x0D	Enable IOCHCK to NMI Enable PERR/SERR to NMI Enable timer 2
Port 92(A)	8	0x0092	0x??	n/c?	Not needed on Longtrail Allocate as reserved I cant find this in Tollgate

3.19.3.5 Setting the Tollgate PCI Configuration Space Registers – IDE (Function 1)

Refer to the Tollgate user’s guide page 109 for the IDE bus master configuration registers. Important things to remember are:

1. Only the IDE bus master (PCI native) mode may be used. The legacy mode cannot be used. Tollgate selects PCI native mode at reset.
2. Only multi–word DMA mode drives may be used. Do not use the soft–DMA function unless it is assured that this function is 100% software transparent to the OSs.
3. Configuration registers are not visible to the OSs; therefore, OF interrogates the attached drive(s) to determine their speed capability and it sets configuration timing parameters in an optimal way for the drives that it finds. The OF in Longtrail does not use the most common denominator (e.g. lowest speed) approach.
4. Longtrail hardware does nothing special to limit or change the IDE capabilities of the chip.
5. Certain parameters must be set as shown in Table 38.

Table 38. Setting the IDE (Function 1) Control Registers – Tollgate ISA Bridge

Name	Size	Index	Default	Set to	Comment
Vendor ID	16	0x01–00	0x1004	n/a[1]	R/O
Device ID	16	0x03–02	0x0703	n/a	R/O
Command	16	0x05–04	0x0000? x000F?	0x0147	Set PCI parity error. Set PERR# check Disable special cycle. Other bits R/O
Status	16	0x07–06	0x0280? x0000?	n/a	—
Rev ID	8	0x08	0x00?	n/a	R/O
Prog Intf	8	0x09	0x8F	n/c[2]	Select Native for primary. Select Native for secondary
Sub–class	8	0x0A	0x01	n/a	R/O
Class code	8	0x0B	0x01	n/a	R/O
Cache Line	8	0x0C	0x00?[3]	n/a	R/O
Latency Tmr	8	0x0D	0x00?	n/a	Experiment for best performance
Hdr Type	8	0x0E	0x00	n/a	R/O
BIST	8	0x0F	0x00	n/a	R/O
Pri Dev 0 (A0)	32	0x10–13	0x????	0xXXXX[4]	Set to config in PCI map
Pri Dev 1 (A1)	32	0x14–1	0x????	0xXXXX	Set to config in PCI map
Sec Dev 0 (A2)	32	0x18–1B	0x????	0xXXXX	Set to config in PCI map
Sec Dev 1 (A3)	32	0x1C–1F	0x????	0xXXXX	Set to config in PCI map
Bus Master(A4)	32	0x20–23	0x????	0xXXXX	Set to config in PCI map
Reserved	32	0x24–2B	n/a	n/a	n/a
IDE Config Pri	8	0x40	0x??	0xX1	This register may be changing. IDE nts to be outputs. Enable IDE ints and DMA for Primary Disable soft IDE
IDE Config Sec	8	0x44	0x??	0xX1	This register may be changing. IDE nts to be outputs. Enable IDE ints and DMA for Primary Disable soft IDE
IDE System	8	0x41	0x??	0xX3	Experiment with settings best performance Enable IDE if primary drive found
IDE System	8	0x45	0x??	0xX3	Experiment with settings best performance Enable IDE if primary drive found
IDE Timing Pri	8	0x42	0x??	0xXX	Set for best performance for slowest drive found at Pri. Only multiword drives are supported.
IDE Timing Sec	8	0x46	0x??	0xXX	Set for best performance for slowest drive found at Pri. Only multiword drives are supported.
Pri Read Ahead	8	0x4	0x??	0xXX	Experiment with setting best performance using GUI in OF.
Sec Read Ahead	8	0x47	0x??	0xXX	Experiment with setting best performance using GUI in OF.

Notes:

1. n/a = not applicable
2. n/c = no change required
3. ? = data not found or author is not sure
4. X = varies according to conditions

3.20 Programming Requirements for the National PC87308VUL

3.20.1 Power–on Strappings for the National PC87308VUL Chip

The board has pull–up/pulldown resistors which configure the chip as indicated in Table 39. Note that, after power–on, the only registers open are the index and data pair located at 015Ch. Software uses this pair to configure all other registers. It is not necessary to do the full PnP isolation procedure to awaken this chip because it comes up in motherboard mode.

Table 39. PC87308 Power–On Strapping

Pin#	Signal Name	Pulled	Resulting Default
138	CONFIG0	lo (internal)	FDC, KBC, RTC wake up inactive No XBUS defined on '308 Clock source is 24 MHz External
144	CONFIG1	lo (internal)	
146	CONFIG2	lo (internal)	
148	CONFIG3	lo (internal)	
134	BADDR0	lo (internal)	PnP motherboard mode selected with Base address = 015Ch
136	BADDR1	hi	
77	SELCS	hi (internal)	CS0 routed to pin 68

These registers are used to access all other configuration registers. It is not necessary to run the full ISA PNP isolation protocol (see Table 40).

Table 40. Index/Data Registers at Hardware Reset

Index	Data
0x15C	0x15D

3.20.2 Use of the GPIO Registers and Signals in the PC87308VUL

The '308 has two general purpose I/O ports which Longtrail uses for various purposes summarized in Table 41. The configuration, reading, and writing of these registers is rather specialized. See the PC87308VUL data book for details.

The two GPIO registers share a common base address. The base address should be set so that GPIO 1[7:0] are accessed at port 0800h (This address is not critical as long as it does not conflict with any other fixed address in the ISA space). All functions in these registers are controlled by Open Firmware or RTAS and are not required to be at compatible addresses.

Table 41. Assignments of GPIO Registers and Signals

Port	Name	Pin #	In/out	Function	Notes
1	GPIO10	149	in	BURST_CAPABLE	1
1	GPIO11	150	in	VAUX_Power Supply	2
1	GPIO12	151	out	S/W Controlled Power off	3
1	GPIO13	152	out	Reset Failsafe Defeat	4
1	GPIO14	153	out	Ser Failsafe Defeat	5
1	GPIO15	154	out	STANDBY_MODE	6
1	GPIO16	155	in	11-Bit TAG Present	7
1	GPIO17	156	in	Password Override	8
2	GPIO20	157		Reserved for Infrared	9
2	GPIO21	158		Reserved for Infrared	9
2	GPIO22	159		Power off Request	9
2	GPIO23	160		Reserved for Ring	9
2	GPIO24	73	in	L2 Presence Detect (0)	8
2	GPIO25	74	in	L2 Presence Detect (1)	9
2	GPIO26	75	in	L2 Presence Detect (2)	10
2	GPIO27	76	in	L2 Presence Detect (3)	11

Notes:

1. The installed MAC ROM supports 120-60-60-60 if this bit bit=0.
2. PM_SUPPLY_PRESENT
   1 = R/O bit means that the system is equipped with a supply that can be switched on/off under logic control and that maintains an auxiliary 5V when off.
   0 = A non power–managed supply is present.
3. Software controlled power-off
   1 = default after power-up. A button press at the Apple keyboard power key or J32 causes a Power-off interrupt request, and the power may or may not go off within 0-21 seconds, depending on whether the failsafe defeat latch is set and on how the 308 power supply controller is programmed.
   0 = Either button press has no effect if power is already on. If power is off, this bit is meaningless.
4. Active output pulse puts the system in a non–failsafe power–down mode.
   1 = default after system or I/O reset
   0 = reset failsafe mode.
5. Active output pulse puts the system in a failsafe power–down mode.
   1 = default after system or I/O reset
   0 = set failsafe mode.
6. Active output causes audio and L2 to enter low–power standby mode
   1 = default after system or I/O reset: standby mode
   0 = run mode.
7. The installed L2 supports 11-bit tag if this bit=0 when needed during a special test routine.
8. This input reflects the position of a jumper on the board which may be parked in either of two positions. The usual use is to compare the current state at boot time to the last state (saved in NVRAM) and interpret a change as a request to override the power–on password.
9. This bit is not configured to be part of the GPIO.
10. Presence detect bits for L2 as defined in Section 3.6.

3.20.3 Configuration and Use of the CS Signals on the PC87308VUL

The chip has three general purpose chip select pins which must be configured. Configuration registers in the '308 control the addresses and other factors that activate these pins. Also, some are multifunction and must be configured for CS usage. The hardware uses these pins and some external logic gates for control of the system as outlined in Table 42.

Table 42. PC87308 Chip Select (CS) Pin Utilization

Pin	Active Level	Set-to Activate	Address[2]	Ignore Bits	Function
CS0#	Low	Read AEN=0	0840	None	Unused[1]
CS1#	Low	Read/Write AEN=0	0830	None	Unused[2]
CS2#	Low	Write AEN=0	0820	None	EJECT_FLOPPY_CS#[3]

Notes:

1. Longtrail OF will set this for a convenient check point address. A pulse on this pin may be used as a convenient trigger.
2. Longtrail OF will set this for a second check point address. A pulse on this pin may be used as a convenient trigger.
3. See Section 3.21 for a discussion of floppy drive considerations.

3.20.4 Extra NVRAM in the RTC

It is noted that the RTC in the '308 has three banks of NVRAM. Extra NVRAM storage may be useful to RTAS or OF.

3.20.5 RTC NVRAM Lock in '308

The NVRAM in the 308 may be locked using programming methods described in the 308 users guide. This lock has nothing to do with the 8-32K system NVRAM.

3.20.6 Configuration Register Settings Required for the National PC87308VUL Chip

The '308 part must be configured before much of the Longtrail I/O will function. The table below outlines specific configuration settings that are necessary to match the hardware connections.

This chapter does not attempt to replicate the complete configuration protocol for the 308. It is too long and the author doesn't understand it all anyway. Important points to remember are:

- The chip is configured to wake up in motherboard mode.
- The base address from which all other configuration registers may be accessed is 0x15C/Dh. These are the addresses of an Index/Data register pair.
- The Longtrail board itself makes few requirements on configuration except for the GPIOs, the programmable chip selects, and a few instances where 308 pin functions must be configured to match the rest of the motherboard. For the most part, assignments of DMAs, IRQs, IRQ types and levels, etc. are software issues. As long as the ISA bridge and the 308 are programmed consistently, the hardware should

work. Many of the address and resource assignments suggested below are only a ”stake in the ground” to provide a common understanding between hardware and OF/RTAS developers.

- The GPIOs require specific set–up and some bits require a pulse to be formed in order to initialize external logic.
- OF developers should provide a table or list of all configured address assignments for inclusion in this document.

3.20.6.1 Standard PNP Register Definitions

Table 43 defines the standard PNP registers. For more information see the National 308 users guide or the ISA PNP specification.

Table 43. PNP Standard Control Registers

Index	Name	Definition/Comment
0x00	Set RD_DATA Port	No change required ?
0x01	Serial Isolation	Do not write to this
0x02	Configuration Control	Do not write to this; may be used to reset configuration
0x03	Wake CSN	Do not write this
0x04	Resource Data	Not needed
0x05	Status	Not needed
0x06	CSN	Do not write
0x07	Logical Device Number	Write the logical device number (0–8) of the component that you wish to configure here.
0x20	Vendor defined	Serial I/O ID Register – Default 0xA0
0x21–24	Vendor Defined	Card control registers – see below
0x30	Activate	Set bit 0 to one for each logical device. This bit makes each logical device active on the ISA bus.
0x31	I/O Range Check	Use as defined in the user’s guide
0x60	I/O Port Base High	0x60/61 set the base of the I/O for each logical device
0x61	I/O Port Base Low	0x60/61 set the base of the I/O for each logical device
0x70	Int Req Level Select	Sets the IRQ level for the logical device number in 0x07
0x71	Int Req Type	Sets the level and type of IRQ for the device number in 0x07. Bit 0, 1=level sensitive, 0=edge sensitive Bit 1, 1=high level, 0= low level (There may be a typo in the user’s guide; this appears to conflict with the default values)
0x74	DMA Channel Select 0	Sets the DMA level for the logical device number in 0x07
0x75	DMA Channel Select 1	Sets the DMA level for the logical device number in 0x07
0xF0–FE	Vendor Defined	See Table 44, Table 47, Table 49 through Table 51, Table 57 through Table 61, Table 71, and Table 74.

3.20.6.2 Logical Device Control Registers

This section defines the values to place in each of the logical device configuration registers (see Table 44 through Table 52). In most cases the default values are retained.

Table 44. Logical Device 0 — KBC Configuration Registers – KBD

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c	I/O range check
0x60	R/W	0x00	0x00	n/c	I/O Base = 0x00 MSB
0x61	R/W	0x60	0x00	n/c	I/O Base = 0x60 LSB
0x62	R/W	0x00	0x00	n/c	Cmd Base = 0x00 MSB
0x63	R/W	0x64	0x00	n/c	Cmd Base = 0x64 LSB
0x70	R/W	0x01	0x01	n/c	KBD Interrupt = IRQ1
0x71	R/W	0x00	0x00	0x02	KBD Int = high, edge sensitive (may be p308 errata here)
0x74	R	0x04	0x04	n/c	No DMA assigned for 8 bit channels
0x75	R	0x04	0x04	n/c	No DMA assigned for 16 bit channels
0xF0	R/W	0x40	n/e	n/c	KB Clk = 12 Mhz

Notes:

1. n/e= no effect
2. n/c= no change required

Table 45. Logical Device 1 — KBC Configuration Registers – Mouse

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x70	R/W	0x0C	0x0C	n/c	MSE Interrupt = IRQ12
0x71	R/W	0x00	0x00	0x02	MSE int = high, edge sensitive (may be p308 errata here)
0x74	R	0x04	0x04	n/c	No DMA assigned for 8 bit channels
0x75	R	0x04	0x04	n/c	No DMA assigned for 16 bit channels

Note: n/c= no change required

Table 46. Logical Device 2 — RTC & APC Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate (APC always active)
0x31	R/W	0x00	0x00	n/c	I/O range check
0x60	R/W	0x00	0x00	n/c	I/O Base = 0x00 MSB
0x61	R/W	0x70	0x70	n/c	I/O Base = 0x70 LSB
0x70	R/W	0x01	0x01	n/c	RTC Interrupt = IRQ8
0x71	R/W	0x00	0x00	0x01	RTC Int = low, level sensitive (may be 308 errata here)
0x74	R	0x04	0x04	n/c	0x74 R 0x04 0x04 n/c No DMA assigned for 8 bit channels
0x75	R	0x04	0x04	n/c	No DMA assigned for 16 bit channels

Note: n/c= no change required

Table 47. Logical Device 3 — FDC Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[1]	I/O range check
0x60	R/W	0x03	0x03	0x03	I/O Base = 0x03 MSB
0x61	R/W	0xF0	0xF0	n/c	I/O Base = 0xF0 LSB
0x70	R/W	0x01	0x01	n/c	FDC Interrupt = IRQ6
0x71	R/W	0x02	0x02	n/c	FDC Int = high, edge sensitive
0x74	R	0x02	0x02	n/c	FDC DMA assigned to Ch 2
0x75	R	0x04	0x04	n/c	No DMA assigned on 16 bit channels
0xF0	R/W	0x00	n/e[2]	0x40	Two drive mode, Enhanced TDR, Densel active hi (experiment with bit 5)
0xF1	R/W	0x00	n/e	n/c?	I'm clueless. Probably only meaningful when 4 drives are used.

Notes:

1. n/e= no effect
2. n/c= no change required

Table 48. Logical Device 4 — Parallel Port Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[1]	I/O range check
0x60	R/W	0x02	0x02	n/c	I/O Base = 0x02 MSB
0x61	R/W	0x78	0x78	n/c	I/O Base = 0x78 LSB
0x70	R/W	0x07	0x07	n/c	PAR Interrupt = IRQ7
0x71	R/W	0x00	0x00	0x02	PAR Int = high, edge sensitive (may be p308 errata here) also see the user's guide
0x74	R	0x02	0x04	0x01	DMA assigned to channel – Note 2
0x75	R	0x04	0x04	n/c	No DMA assigned

Notes:

1. n/c= no change required
2. The correct initialization for the PP is somewhat unclear at this time. The issue is whether one initialization meets all run time requirements for all possible modes of operation. The configuration registers are not visible to the OSs.

Table 49. Logical Device 5 — UART2 and Infrared Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[1]	I/O range check
0x60	R/W	0x02	0x02	n/c	I/O Base = 0x02 MSB
0x61	R/W	0xF8	0xF8	n/c	I/O Base = 0xF8 LSB
0x70	R/W	0x03	0x03	n/c	UART2 interrupt = IRQ3
0x71	R/W	0x03	0x03	0x02	PAR Int = high, edge sensitive (may be p308 errata here). Also see the user's guide
0x74	R	0x02	0x04	n/c?	No DMA assigned
0x75	R	0x04	0x04	n/c?	No DMA assigned
0xF0	R/W	0x02	n/e[2]	0x0A	Tri state off, Normal power, Ring detect=RI, Bank switching? It may be necessary to assign DMA channels to the UART2 port if the Infrared capability is configured.

Notes:
1. n/c= no change required
2. n/e= no effect

Table 50. Logical Device 6 — UART1 Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[1]	I/O range check
0x60	R/W	0x03	0x03	n/c	I/O Base = 0x03 MSB
0x61	R/W	0xF8	0xF8	n/c	I/O Base = 0xF8 LSB
0x70	R/W	0x04	0x04	n/c	UART1 interrupt = IRQ4
0x71	R/W	0x03	0x03	0x02	UART1 Int = high, edge sensitive (may be p308 errata here) also see the user's guide
0x74	R	0x02	0x04	n/c	No DMA assigned
0x75	R	0x04	0x04	n/c	No DMA assigned
0xF0	R/W	0x04	n/e[2]	n/c	See user's guide

Notes:
1. n/c= no change required
2. n/e= no effect

Table 51. Logical Device 7 — GPIO Ports Configuration Registers[1]

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[2]	I/O range check
0x60	R/W	0x00	0x00	0x08	I/O Base = 0x08 MSB
0x61	R/W	0xF8	0xF8	0x00	I/O Base = 0x00 LSB
0x74	R	0x02	0x04	n/c	No DMA assigned for 8 bit channels
0x75	R	0x04	0x04	n/c	No DMA assigned for 16 bit channels

Notes:

1. Additional configuration required – See Section 3.20.6.10.
2. n/c= no change required. No interrupt assigned

Table 52. Logical Device 8 — Power Management Configuration Registers

Index	R/W	Hard Reset	Soft Reset	Set to	Comment
0x30	R/W	0x00	0x00	0x01	Activate
0x31	R/W	0x00	0x00	n/c[1]	I/O range check
0x60	R/W	0x00	0x00	0x08	I/O Base = 0x08 MSB
0x61	R/W	0x00	0x00	0x50	I/O Base = 0x50 LSB
0x74	R	0x02	0x04	n/c	No DMA assigned
0x75	R	0x04	0x04	n/c	No DMA assigned

Notes:

1. n/c= no change required. No interrupt assigned

3.20.6.3 Card Control Registers

See Table 53 through Table 56.

Table 53. SIO Configuration 1 Register – Index 021 – R/W

Bit	7	6	5	4	3	2	1	0	Hex
Default	0	0	0	0	0	1	1	0	0x06 1
Set to:	0	0	0	0	0	0	1	1	0x03
Comments: Try bit 0 =1 (Zero ISA wait states) for better performance. Select PS2 mode for the FDC									

Table 54. SIO Configuration 2 Register – Index 022 R/W

Bit	7	6	5	4	3	2	1	0	Hex
Default	0	0	0	0	0	0	1	0	0x02
Set to:	0	0	1	1	0	1	1	0	0x36
Comments: bit 2 configures power off request pin (IRQ10). Bits 3–5 reserve pins for IRDA functions									

Table 55. Programmable Chip Select Index Configuration Register – Index 023 R/W

Bit	7	6	5	4	3	2	1	0	Hex
Default	0	0	0	0	0	0	0	0	0x00
Set to:	0	0	1	1	0	1	1	0	0-3
Comments: This register is used in connection with logical device 7 configuration register. It points to CS0, CS1, or CS2 for configuration. See Section 3.20.6.9 for additional CS configuration information.									

Table 56. Programmable Chip Select Configuration Data Register – Index 024 R/W

Bit	7	6	5	4	3	2	1	0	Hex
Default	X	X	X	X	X	X	X	X	0xXX
Set to:	Data								
Comments: This register is used in connection with logical device 7 configuration register. It to conveys data for CS0, CS1, or CS2 for configuration. See below at TAG XYZ for additional CS configuration information.									

3.20.6.4 KBC Configuration Register

TBD

3.20.6.5 FDC Configuration Registers

See Table 57 through Table 58.

Table 57. SIO FDC Configuration Register – Index 0XF0 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	1	0	0	0	0	0	0	
Comment: Bit 6 enables reading for media type at the TDR									

Table 58. SIO Drive ID Register – Index 0XF1 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	0	0	0	0	0	0	
Comments: No idea									

3.20.6.6 SIO Parallel Port Configuration Register — Index OXF0 — R/W

Table 59. SIO Parallel Port Configuration Register — Index OXF0 — R/W

Bit	7	6	5	4	3	2	1	0	
Default	1	1	1	1	0	0	1	0	
Set to:	?	?	?	?	?	0	1	1	
Comments: Configure bits 3–7 as required to be S/W compatible with CHRP. The correct initialization for the PP is somewhat unclear at this time. The issue is whether one initialization meets all run time requirements for all possible modes of operation. The configuration registers are not visible to the OSs.									

3.20.6.7 UART2 and Infrared Configuration Registers – Index 0XF0 – R/W

Table 60. UART2 and Infrared Configuration Registers – Index 0XF0 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	1	0	1
Set to:	0	0	0	0	0	0	1	0	
Comments: Bit 3 enables the RING pin for future use.									

3.20.6.8 UART1 Configuration Register – Index 0XF0 – R/W

Table 61. UART1 Configuration Register – Index 0XF0 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	1	0	1
Set to:	0	0	0	0	0	0	1	0	
Comments:									

3.20.6.9 Programmable Chip Select Configuration Registers

See Table 62 through Table 70.

Table 62. CS0# Base Address MSB Register – Index 0X00 – W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	0	0	1	0	0	0	
Comments: Configure at 0x0840									

Table 63. CS0# Base Address LSB Register – Index 0X01 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	1	0	0	0	0	0	0	
Comments: Configure at 0x0840									

Table 64. CS0# Configuration Register – Index 0X02 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	1	0	0	0	0	0	0	
Comments: R/W of 0x0840 gives a trigger point on CS0# pin. Set for read or write									

Table 65. CS1# Base Address MSB Register – Index 0X04 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	0	0	1	0	0	0	
Comments: Configure at 0x0830									

Table 66. CS1# Base Address LSB Register – Index 0X05 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	1	1	0	0	0	0	
Comments: Configure at 0x0830									

Table 67. CS1# Configuration Register – Index 0X06 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	1	0	0	0	0	0	0	
Comments: R/W of 0x0830 gives a trigger on CS1# pin for read or write									

Table 68. CS2# Base Address MSB Register – Index 0X08 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	0	0	1	0	0	0	
Comments: Configure at 0x0820. This is the floppy eject register. Bit 0 of 0x0830 is the FE bit.									

Table 69. CS2# Base Address LSB Register – Index 0X09 – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	1	0	0	0	0	0	
Comments: Configure at 0x0820. This is the floppy eject register. Bit 0 of 0x0830 is the FE bit.									

Table 70. CS2# Configuration Register – Index 0X0A – R/W

Bit	7	6	5	4	3	2	1	0	
Default	0	0	0	0	0	0	0	0	1
Set to:	0	0	0	1	0	0	0	0	
Comments: Decodes floppy eject register. Set for write only. Bit 0 of 0x0830 is the FE bit.									

3.20.6.10 GPIO Configuration – In I/O Space

After the GPIO base address and decode qualifiers are set, the configuration must be completed by writing to associated registers according to Table 71.

Table 71. GPIO Configuration – In I/O Space

GPIO Register	Offset	Type	Hard Reset Value	Set to	Comment
Port 1 Data (0x0800)	0	R/W	0XFF	n/c	Data Port GPIO(7:0)
Port 1 Direction (0x0801)	1	R/W	0x00	0x7F	See Table 41. GPIO(7:0) Note 2
Port 1 Output (0x0802)	2	R/W	0x00	n/c	See Table 41. GPIO(7:0)
Port 1 Pullup (0x0803)	3	R/W	0xFF	n/c	See Table 41. GPIO(7:0)
Port 2 Data (0x0804)	4	R/W	0XFF	n/c	Data Port. GPIO(15:8)
Port 2 Direction (0x0805)	5	R/W	0x00	n/c	See Table 41. GPIO(15:8)
Port 2 Output (0x0806)	6	R/W	0x00	n/c	See Table 41. GPIO(15:8)
Port 2 Pullup (0x0807)	7	R/W	0xFF	n/c	See Table 41. GPIO(15:8)

Notes:

1. n/c= no change required.
2. The OF must initialize the external failsafe defeat latch by writing a 0 to GPIO bit 13 (Port 1, bit 3) and then writing this bit back to a 1. This must be done after the GPIO is completely initialized. The latch comes up in an indeterminate state. See Table 41 and the discussion of power on–off control in Section 3.27. Writing GPIO13 resets the defeat latch so that the system may respond to a power–off button press during the boot process. Just before giving control to the OS, the OF should pulse GPIO14 by writing a 0 and then a 1. This will set the external failsafe defeat latch, so that the system power can only be turned off by explicit software commands.

3.20.6.11 Advanced PS Control (APC) Configuration – Part of Logical Device 2

The programming of these registers is subject to change during the development process. They are addressed using a procedure that addresses bank2 of RTC memory. They are reset to 0x00 only when battery power is applied and they retain values during normal power–off. Initialize the registers to the values suggested in Table 72.

Table 72. APC Register Configuration

Name	Bank2-Index	Type	Set to	Comment
APCR1	0x40	mixed	0x10	5sec off, POR=edge, mask auto–on from fail
APCR2	0x41	R/W	0x15	Enable timer match, ring=XDS pin, ring=falling edge, ring enabled, RI1 enabled, RI2 disabled, switch off after 0 delay.
APSR	0x42	R to clr	n/a[1]	Status input register
RLR	0X47	R/W	n/a	Locks access to RAM; cleared only by hard reset

Notes:

1. n/a= not applicable

3.20.6.12 Configuring the Power Management Device – Logical Device 8

The five registers of the Power Management controller are accessed via an index/data register pair located as shown in Table 73.

Table 73. Power Management Index Registers

Address	Type	Function
Base (0x0850)	R/W	Index to point to remainder of the power management resisters (Index = 0–4)
Base + 1 (0x0851)	R/W	Data register for the five power management registers

The power management registers must be configured as shown in Table 74.

Table 74. Power Management Registers

Name	Index	Type	Hard Reset	Set to	Comment
FER1	0x00	R/W	0xFF	n/c[1]	All functions enabled
FER2	0X01	R/W	0xFF	n/c	CS pins enabled, GPIO enabled
PMC1	0x02	R/W	0x00	n/c	FDC, PP, UARTs, not tristated
PMC2	0x03	R/W	0x00	n/c	Clock is 24 Mhz external
PMC3	0x04	R/W	0x0E	n/c	PP, UARTs clock enabled

Notes:

1. n/c= no change required

3.20.7 Configuration Register Settings Required for the CS 4236 Audio Chip

This section describes all the settings required to configure the CS4236 to operate compatibly with the code designed for the CHRP audio subsystem.

TBD

3.21 Floppy Drive Considerations

CHRP places two unique requirements on floppy drives. It specifies that auto-eject floppies be used and that the media sense function detects whether a floppy is present without stepping or spinning the media. Apple operating systems frequently check for disk presence. Note that CHRP also requires that the floppy disk controller be programmed in the PS2 mode of operation.

3.21.1 Auto Eject

Longtrail provides for the use of either standard or auto-eject floppies; however, users who do not provide auto-eject floppies may have unknown problems with Apple operating systems. The ’308 does not directly support the auto-eject function, and additional glue logic is added for this.

Longtrail provides a means of driving a signal wire in the floppy drive cable for the eject function. The address is configurable, and it is reported in the OF device tree. Software in the floppy driver code must control the eject signal timing by writing to bit 0 of the eject–floppy register. Longtrail utilizes the CS2# output of the ’308 chip to decode this register and implements a 1–bit register which is configurable anywhere in ISA I/O space. CHRP does not specify timing parameters for this signal, so ad–hoc standards will apply. This function is not abstracted by RTAS. The hardware and software interfaces are defined by Table 75 and Table 76.

Table 75. Floppy Eject Address

Address	Type	Bit Number							
0x0820	R/O	7	6	5	4	3	2	1	0
		x	x	x	x	x	x	x	FE
		FE=0 Eject signal inactive							
		FE=1 Eject signal active							

Table 76. Floppy Eject Information

Requirement	Value
Cable pin number for FE# signal	1
Signal levels	TTL
Active level	low
Conditioned by	Drive signal active
Timing requirements	Similar to Sony MPF 520–7

3.21.2 Media Presence Sense

The CHRP specification requires that a floppy drive be used which provides media–presence sense information. OEMs who supply drives that do not conform will have unknown problems with MAC OS and will not be CHRP compatible.

Floppy drives are required to provide media–presence sense information on the pin traditionally labelled ”DISK CHANGE”. The signal must be valid any time that the drive is selected with out spinning or stepping the drive. This is a physical change required in the floppy drive itself in order to meet this requirement. The state of this signal is reported on bit 7 of the DIR register of the floppy disk controller implemented in the National ’308. No change is made to the board logic or the National superIO part. This is a standard register interface. The conditions for correct interpretation of this register are not changed, only the meaning of the input signal. Table 77 summarizes this paragraph.

Table 77. Floppy Media Presence Register

ISA Address	Bit						
FDCbase + 07h (03F7h if configured in standard manner)	MP	x	x	x	x	x	x	x
	MP=0 No media present in selected drive MP=1 Media is present in selected drive (AKA DSKCHG bit)							

3.21.3 Media–Type Sense

CHRP does not require a mechanism to sense the type of media in the drive. This is traditionally handled by cut–and–try methods. However the National ’308 and Longtrail support two media–type signals which are reported in the TDR register of the floppy disk controller. The relevant portion of the TDR is summarized in Table 78.

Table 78. Media-Type Portion of TDR

Address	FDC Name	Type	7	6	5	4	3	2	1	0
FDC base + 03h (03F3 if configured in standard manner)	TDR	R/W	ED 2	HD 3	1	1	1	1	1	1

Notes:
1. See National ’308 specification for other bits.
2. R/O bit. Corresponds to MS1# pin. See Table 79 for meanings.
3. R/O bit. Corresponds to MS0# pin. See Table 79 for meanings.

OEMs are cautioned that many drives do not support media–type signals or that they support only one or the other.

The individual bit meanings are:

- HD=1 means high–density (1.44MB) media is present if it is also known that some media is actually present. The state of this bit is the same with media in the drive or not, because a hole in the case is sensed with an optical sensor.
- HD=0 means that some media is in the drive, but not a HD media.
- ED=1 means Extra–density (2.88MB) media is present if it is also known that some media is actually present. The state of this bit is the same with media in the drive or not, because a hole in the case is sensed with an optical sensor.
- ED=0 means that some media is in the drive, but not a ED media.

For drives that support both MS bits, the meanings may be summarized in Table 79.

Table 79. Media-Type Bit Meanings for Some Drives

Signal at Floppy Drive Cable		Corresponding TDR bit		Interpretation
MS0#	MS1#	HD	ED	
0	0	1	1	No media or 5.25” drive used
0	1	1	0	1.44 MB (HD) media in selected drive
1	0	0	1	2.88 MB (ED) media in selected drive
1	1	0	0	720 K media in selected drive

3.22 Configuration Requirements for Hydra

Required configuration settings
TBD

3.23 PCI Card Presence

Longtrail does not report the presence or absence of the PCI cards except via the configuration mechanism. If a card does not respond to configuration cycles it will appear to be absent and a visual check will be necessary for diagnosis.

3.24 Reset Conditions

3.24.1 Soft Reset

Soft reset is accomplished in Longtrail by writing to the processor initialization register, offset 0x41090, in Hydra. The processor soft reset pin is connected to the RESET_CPU0# pin of Hydra (pin 133). Note that this register bit is ”sticky.” There must be code in the reset vector path to turn it off before the exception interrupt is re-enabled.

3.24.2 Power-On Reset

The processor and all system components are reset when the power supply is first turned on.

3.24.3 System Reset/System Reboot

Longtrail supports the ”system–reboot” RTAS call by providing an I/O port that RTAS may write to in order to cause a system–wide reset, which results in an automatic reboot. All motherboard logic, the CPU, and all bus–attached devices are put into their power-on default conditions. Memory contents are corrupted. Any write-once registers, such as password protect, are reset. The OF must completely reinitialize the whole system, even though it will distinguish the reboot from a power-on boot with information stored in NVRAM. This function is implemented by an ADB reset command to Hydra.

The ADB reset function is not correctly described in the Hydra literature. It may be accessed with the following procedure:

1. Set the reset enable bit in the ADB interrupt source enable register by writing 0x10 to PCI base address for Hydra + 0x110A0.
2. Reset the system by writing 0x10 to the test mode register at PCI base for Hydra + 0x111100.

3.24.4 I/O Reset

Longtrail supports the CHRP requirement for an I/O reset capability by providing a port that RTAS may write to in order to reset I/O devices. All motherboard I/O devices including all native PCI and ISA and all bus–attached PCI and ISA devices are reset to their power–on conditions.

The CPU and the GGII chip set are not reset. The ISA bridge is not reset. Any write-once registers in the ISA bridge, such as password protect, are preserved. Memory operation is unaffected. Note that RTAS will have to reconfigure the entire I/O subsystem including the 308, audio, PNP devices, and etc. after writing this port before returning control to the OS. This port is described in Table 80.

Table 80. IO Reset Port

	565 Implementation	Tollgate Implementation
Address	PCI config 004Ch	?
Port name	ISA clock divisor reg	?
Bit number	3	?
Type	W/O (this bit)	W/O
Sticky	no	no

3.24.5 ADB Reset

ADB_RESET# is a feature of the Hydra chip that is supported in Longtrail. It is not defined as a CHRP requirement. When the ADB cell in Hydra detects certain key combinations involving the power key on the Apple keyboard, it activates this pin. The result is the same as defined above for a system reset. This is a hardware function not controlled by firmware or the OS.

3.25 Clock Design

3.25.1 Main Clock

The main system clock is the W49C65–04 clock chip from IC works. It synthesizes all output frequencies from a 14.318 MHz crystal and it may be set for five different output frequencies.

The system clock is configured when the jumpers are set or the key card is inserted. Control signals are pulled high or low according to Table 81.

Table 81. Clock Controls

Clock Select Input			Frequency Out	
Sel 2	Sel 1	Sel 0	CPU	PCI
1	0	0	50	25
1	1	1	55	27.5
1	0	1	60	30
1	1	0	66.6	33.3
1	1	1	75[1]	37.5[1]
1				

Note:
1. Not supported.

3.25.1.1 Other Frequency Sources

Other crystals and oscillators are summarized in Table 82.

Table 82. Crystals and Oscillators on Longtrail Card

Frequency	Crystal	Oscillator	Use
14.318 MHz	yes	no	W49C65 main clock synthesizer
32.768 KHz	no		PC87308VUL clock synthesizer & RTC
31.3344 MHz	no	yes	Hydra ADB
50.0000 MHz	no	yes	Hydra MESH SCSI
24.576 MHz	no	no	Audio Frequency Synthesizer
???	no	no	Audio Frequency Synthesizer

3.26 Power Management

There is no dedicated power management hardware on Longtrail other than the ability to support hibernate mode with software controlled power–off and a standby control for the L2 and audio. Firmware or RTAS may interrogate GPIO bit 10 to determine if a software controllable supply is being used.

GPIO 10 = 1 means a software controllable supply is present
GPIO 10 = 0 means the supply is not software controllable

All power management in Longtrail is controlled by RTAS using the native capabilities of the chips and devices. See the various chip specifications for power management capabilities. It is possible to power manage portions of the National 308, Hydra, the audio chips, and the L2. GGII and the ISA bridge do not have dedicated PM functions, but they will revert to lower than normal power consumption when activity ceases or slows significantly. Various processors have various power management capabilities. There are no reduced frequency clocks or power islands in Longtrail.

The power management states supported are shown in Table 83.

Table 83. Power Management States

State	Description/State	Power Consumption	Possible Wake-up Events
Full On	Normal state All functions fully operational	maximum	n/a
Suspend	Pwr Supply on Processor in low-power mode but responsive to interrupts Memory—low power refresh or memory off SCSI – off ADB off unless ADB wake up is required SCC—off Open PIC—on Audio—off—standby L2—off—standby ISA bridge—on ’308 Any portion not required for wake–up may be off Hard disk—spin down ISA Plug–in—depends on card PCI Plug-in—depends on card	intermediate (May be possible to reach energy star)	ADB KB ADB Mouse KB Mouse External modem Timed wake–up (in 308’s APC)
Hibernate	Power–supply off (trickle supply on)	< 30watts incl Pwr supply excl CRT	Timed wakeup External modem

3.27 Power-On/Off Control

This section describes how the board implements power-on/off when a power-managed supply is attached. The description includes both Apple and non-Apple keyboards.

Longtrail has two two–pin headers where OEMs may connect momentary push buttons for on–off control. OEMs may choose to support neither, either or both of the on/off switches. These are outlined in Table 84.

Table 84. Power-On/Off Connectors

Connector	Function
J-30	Turns power on if it is off. Unconditionally turns power off if it is on. This overrides any software. It may be used if the OS does not support the power–off RTAS call or for an emergency power–off in case the OS is unresponsive.
J-32 (Apple power button)	Turns power on if it is off. Button presses are ignored if power is on. The Apple keyboard power switch is wired in parallel with this button input and has the same effect. Some Power Mac models treat this button as an On button and a software-controlled power down. A GPIO bit (GPIO12) may be configured to alter this function. In that case, a key press when the system is on causes an power-off interrupt request. The OS/RTAS will shut down the system.

The board includes the following provisions:

- Battery back up for RTC, APC, and NVRAM
- Trickle power back up for battery
- ONCNTL is wired to the power control of the power supply
- The SWITCH input on the APC is wired to the Apple keyboard power switch and to a 3-pin header, which may connect to a momentary switch. These two are wired in parallel. The circuit is arranged so that a press of either button activates the input if the power is off. The power may always be turned on with either of these buttons. GPIO12 is used to control operation when power is already on as follows:

  GPIO12 output high = Either button press is propagated and the 308 will signal power-off request (power-off IRQ10). The APC will try to shut down power after the programmed delay. Power may or may not go off, depending on the state of the external failsafe defeat latch described in the next bullet.

  GPIO output low = Either button press is blocked. The system takes no notice and power stays on.
- An external latch on board defeats the failsafe nature of the 308 power supply controller. If the power is on and a button press is propagated to the SWITCH input pin, the 308 resets ONCNTL in order to turn the power off. But the failsafe defeat latch will hold power on as long as it is set. Both the 308 and the failsafe defeat latch must agree in order to remove power. The latch comes up in an undefined state. OF must either reset the latch by writing a 0 to GPIO13, or else it must set the latch by writing a 0 to GPIO14. In either case, GPIO 13 or 14 must be returned to 1.
- Power-off request interrupt output is wired to IRQ10.

In order for the APC to function as described, there are a number of configuration bits which must be set by OF.

3.27.1 Power-On Events

The automatic power supply control (APC) is the National ’308. When power is off (trickle power or battery power is on), the APC can detect a power-on event as follows:

1. Activation of the Apple keyboard ON/OFF button or activation of one the external switches.
2. A match on time and date if the APC is programmed to turn on at a predetermined time.

3. A ring indicator activation from an external modem connected to serial port 1 (if enabled).
4. OEMs who wish to extend the automatic power-up function may connect a falling-edge signal to the ring pin at the 308. For example, a network card that is always powered might connect at this point.

When a power-on event occurs, the APC automatically activates the ONCNTL signal, which then activates the system power supply. A normal boot results. Software may poll the APC status register, 0x42, to determine the cause of the power-on event.

The system may turn on as soon as AC power is restored following a power failure if bit 4 of APC register 1, 0x40, is set to zero. Configuration code should set this bit to 1 to prevent surprise activation. A configuration option is supplied in the OF GUI, which allows users to change this option for special applications.

3.27.2 Configuring for Power-Off During Boot

Longtrail uses the APC feature of the National '308 chip to control both power-on and power-off; however, Longtrail adds a feature to defeat the failsafe (FS) nature of the APC. This is because CHRP requires a non-FS power-off when software controlled power-off hardware is present. OF will maintain the system in a FS state as long as possible.

When power is first applied, OF programs the APC for 0–seconds turn off delay. OF sets GPIO12 to a 1 (default condition) so that button presses at the Apple keyboard power switch or J32 are propagated. OF also resets the failsafe defeat latch by writing a 0 and then a 1 to GPIO13. These bits are defined in Table 85, Table 86, Table 87, and Table 88. OF will maintain this state as long as possible so that pressing any of the on/off keys will give an immediate power-off.

Table 85. Software Controlled Power-Off Bit

Name	SW_CONT_PO
Address	GPIO Base + 0 (ISA I/O 0800h)
Bit	2 — GPIO12 1 = Default, Button presses at Apple keyboard power button or J32 are propagated to the SWITCH input on the 308 so that the buttons may invoke a software controlled power-off 0 = Blocks the button presses. These buttons will not invoke a hardware or software power-off.
Type	R/W specialized

Table 86. Set Failsafe Defeat Bit

Name	SET FS Defeat
Address	GPIO base + 0 (ISA I/O 0800h)
Bit	4 — GPIO14 1 = Default, no active set to external defeat logic. 0 = Sets the external defeat logic. Firmware must form a pulse by writing a ”0” and then writing a ”1.” See National data book for specialized procedure to write the GPIOs.
Type	R/W specialized

Table 87. Reset Failsafe Defeat Bit

Name	RESET FS Defeat
Address	GPIO base + 0 (ISA I/O 0800h)
Bit	3 — GPIO13 1 = Default, no active reset to external defeat logic 0 = Resets the external defeat logic
Type	R/W specialized

Table 88. Software Off Command

Name	APCR1
Address	APC base + 0040h
Bit	5 — Software off command 0 = ignored 1 = immediately shut off power (if external defeat logic is reset)
Type	R/W Read returns 0

3.27.3 Configuring for Run-Time in the Normal Way

Just before giving control to the OS, the OF writes the following:

- GPIO12 = 0 (blocks the button presses at Apple keyboard power switch
- GPIO14 = 0, then 1 (sets the FS defeat latch. Setting the FS defeat is redundant, but it makes the RTAS common for the methods described herein).

The other conditions are left as follows:

- Power-off delay set in APC = 0 (APCR2 bit 6 = 0)
- All APC control registers are left as initialized.

At this time, the power-off comes under the control of the operating system. At some later time, the OS may initiate a shutdown sequence as the result of an operator action or command. In either case the OS will make the ”power-off” RTAS call when it is ready. RTAS responds to this call by writing to two ports. First it resets the external FS defeat logic by writing a 0 to bit 3 of GPIO 1. Then it writes a software-off command to the APC in the ’308. These bits are described in Table 87.

If the system is locked up, still booting, or otherwise unable to respond to the power-off request IRQ, the power will remain on until AC is removed or until button J30, if present, is pressed.

3.27.4 Configuring for Run-Time When Software Controlled Button Response is Desired

Some Apple models treat a press of the power key (or J32) as a request for a power-off. If this response is desired, the OF must be modified to respond as follows:

- Configure as described for boot time.
- Just before transferring control the the OS, perform the following:
  - Set the power-off delay in the APC to five seconds by setting bit 6 of ACPR 2 to 1.

- Leave GPIO12 in the 1-state (do not block button presses)
- Set failsafe defeat by writing a 0 then a 1 to GPIO14.

In this case, a press of J32 or the Apple keyboard power button propagates to the SWITCH input pin of the 308, and the 308 immediately generates an IRQ10. If there is no software intervention, the 308 shuts off ONCNTL after five seconds, but the failsafe defeat latch will maintain power. When the OS calls RTAS to shut off power, RTAS must issue a shutdown power command to the 308 and write a 0 to GPIO13 to reset the failsafe defeat latch.

Note that the Apple power key switch engages when the key is used in any key combination, but not all of these combinations result in power-off.

3.27.5 Operation with Non-Power Managed Supplies

If the OEM does not wish to supply a power supply that may be turned on and off with logic controls, the motherboard may be modified by populating R894 with a 0-ohm resister and by removing R95. This connects VAUX to VCC. When power is on, the circuitry operates as described in Section 3.27.1 through Section 3.27.4, but the RTAS call to shut down power has no effect. OF may determine the way the board is built by reading GPIO 25. There is no architected use for this bit. One possibility is for RTAS to clear part or all of the screen and prompt the operator for a manual power-off whenever the OS makes the power-off call.

3.28 Processor Configuration Hardware

The Long Trail board is designed to accept a variety of speeds and types of processors. PGA processors do not have presence detect pins to indicate the speed or type of processor. The schematics include two methods for configuring the processor being installed. These are listed as follows:

1. Jumpers —

   1–x4 Block to set VRM input (see Table 89 and Table 90)

   1–x9 Block to set (see Table 91 and Table 97):

   - Three signals for CPU bus speed (see Table 92 and Table 93)
   - Two signals to set bus mode as required by the CPU (see Table 94 and Table 95)
   - Four signals to set CPU PLL ratio (see Table 96, Table 97, and Table 98).
   - Also refer to Table 99 as a quick reference for one optimum bus frequency, processor mode, and CPU PLL setting for each processor type.
2. Key Card Connector — A small card may be inserted to set all the configurations listed in item 1. The OEM needs to supply the key in the upgrade kit if this option is implemented. In that case, the jumpers may be omitted. A different key is required for each processor.

3.28.1 VRM Jumpers, J20

The VRM is controlled by a set of jumpers diagrammed in Table 89. Table 90 shows the possible settings. Except for the 604, all processors have nominal settings of 2.5v. The setting for the 604 is 3.3v. Contact IBM Microelectronics for special cases.

Table 89. J20

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o
4	o	o	o

Table 90. VRM Jumpers (J20) Voltage Identification Code

Row 1	Row 2	Row 3	Row 4	Vccp	
AB	BC	BC	BC	2.1	
BC	AB	BC	BC	2.2	
AB	AB	BC	BC	2.3	
BC	BC	AB	BC	2.4	
AB	**BC**	**AB**	**BC**	**2.5**	← **604ev 603ev**
BC	AB	AB	BC	2.6	
AB	AB	AB	BC	2.7	
BC	BC	BC	AB	2.8	
AB	BC	BC	AB	2.9	
BC	AB	BC	AB	3.0	
AB	AB	BC	AB	3.1	
BC	BC	AB	AB	3.2	
AB	**BC**	**AB**	**AB**	**3.3**	← **604 603e**
BC	AB	AB	AB	3.4	
AB	AB	AB	AB	3.5	

3.28.2 Processor Configuration Jumper Block, J23

The J23 jumper block is labeled on the board with nine rows (1-9) and three columns (A-C). Three major configuration functions are set using the J23 jumper block as shown in Table 91.

Table 91. J23 Jumpers

Row	A B C (columns)
1	Bus Speed (see Table 92 and Table 93)
2	
3	
4	Processor Mode (see Table 94 and Table 95)
5	
6	Processor PLL/VCO (see Table 96, Table 97, Table 98)
7	
8	
9	

3.28.2.1 Bus Frequency

Rows 1, 2, and 3 of the J23 jumper block set the CPU bus frequency (see Table 92). The PCI bus is automatically set to 1/2 the selected CPU bus frequency. Long Trail is designed to run at a maximum CPU bus speed of 66.6 MHz (see Table 93).

Table 92. J23 (Bus Frequency Select)

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o
4	Processor		
5	Mode		
6	CPU		
7	PLL/VCO		
8	Ratio		
9			

Bus Frequency (rows 1–3)

Table 93. J23 Bus Frequency Selection

Row 1	Row 2	Row 3	CPU Bus	PCI Bus
AB	AB	BC	50	25
BC	BC	BC	55	27.5
BC	AB	BC	60	30
AB	BC	BC	66.6	33.3
AB	AB	AB	75[1]	37.5[1]
BC	BC	AB	83.3[1]	41.65[1]

Note:

1. Not supported on the Long Trail design.

3.28.2.2 Processor Mode

Rows 4 and 5 of the J23 jumper block set the processor mode (see Table 94 and Table 95). These settings control the state of bus signal DRTRY# during and after RESET. The obtained settings are as follows:

- 604 — NORMAL mode
- 604ev/603e/603ev — No-DRTRY# mode.

Table 94. J23 (Processor Mode)

	A	B	C
1		Bus	
2		Frequency	
3		Select	
4	o	o	o
5	o	o	o
6		CPU	
7		PLL/VCO	
8		Ratio	
9			

Processor Bus Mode

Table 95. Processor Mode

Row 4	Row 5	Processor
BC	BC	604
AB	AB	604ev
BC	AB	603e/ev

3.28.2.3 CPU PLL/VCO Settings

Rows 6, 7, 8, and 9 of the J23 jumper block set the CPU PLL and Voltage Controlled Oscillator (VCO) (see Table 96). Table 97 shows the valid VCO frequency range for each family of processors. CPU speed settings must be limited to the ultimate VCO range indicated by processor type. After setting the processor mode and PCI bus frequency, these jumpers can be used to optimize the PLL ratio for a given processor. For example, a 150 MHz 604 processor can be optimized for CPU local bus speed at 66.6/133 MHz using a 2:1 PLL ratio or for processor core speed at 50/150 MHz using 3:1 PLL ratio. The numbers in parenthesis in Table 98 are the resulting VCO frequencies at each setting. Also refer to Table 99 as a quick reference for one optimum bus frequency, processor mode, and CPU PLL setting for each processor type.

Table 96. J23 (CPU PLL/VCO Ratio)

	A	B	C
1		Bus	
2		Frequency	
3		Select	
4		Processor	
5		Mode	
6	o	o	o
7	o	o	o
8	o	o	o
9	o	o	o

CPU PLL/VCO Ratio

Table 97. Processor VCO Range

Processor	VCO Range
604	180-360MHz
604e/ev	200-400MHz
603e	100-266MHz
603ev	250-400MHz

Table 98. Jumper Block J23 Settings

						CPU Frequency in MHz (VCO Frequency in MHz)			
Proc. Type	**J23 Row 6**	**J23 Row 7**	**J23 Row 8**	**J23 Row 9**	**PLL Ratio**	**Bus 50MHz**	**Bus 55MHz**	**Bus 60MHz**	**Bus 66.6 MHz**
604	AB	AB	AB	BC	1:1	50 (200)	55 (220)	60 (240)	66.6 (266)
	AB	BC	AB	AB	2:1	100 (200)	110 (220)	120 (240)	133 (266)
	BC	AB	AB	AB	3:1	150 (300)	165 (330)		
	BC	BC	AB	AB	1.5:1			90 (180)	100 (200)
	BC	BC	AB	BC	1.5:1	75 (300)	82.5 (330)	90 (360)	
604ev	AB	BC	AB	AB	2:1	100 (200)	110 (220)	120 (240)	133 (267)
	AB	BC	BC	AB	2.5:1	125 (250)	137.5 (275)	150 (300)	166 (333)
	BC	AB	AB	AB	3:1	150 (300)	165 (330)	180 (360)	200 (400)
	BC	AB	BC	AB	4:1	200 (400)			
	BC	BC	AB	AB	1.5:1				100 (200)
603e (PID6)	AB	AB	AB	AB	1:1			60 (120)	66.6 (133)
	AB	AB	AB	BC	1:1	50 (200)	55 (220)	60 (240)	66.6 (266)
	BC	BC	AB	AB	1.5:1	75 (150)	82.5 (165)	90 (180)	100 (200)
	AB	BC	AB	AB	2:1	100 (200)	110 (220)	120 (240)	133 (266)
	AB	BC	BC	AB	2.5:1	125 (250)			
603ev (PID7V)	AB	BC	AB	AB	2:1				133 (266)
	AB	BC	BC	AB	2.5:1	125 (250)	137.5 (275)	150 (300)	166 (333)
	BC	AB	AB	AB	3:1	150 (300)	165 (330)	180 (360)	200 (400)
	BC	BC	BC	AB	3.5:1	175 (350)			
	BC	AB	BC	AB	4:1	200 (400)			
	AB	AB	BC	BC	Bypass for all processors				

Table 99. Bus/CPU Configuration Quick Reference

Proc. Type	Max. Speed	J23 Row 1	J23 Row 2	J23 Row 3	J23 Row 4	J23 Row 5	J23 Row 6	J23 Row 7	J23 Row 8	J23 Row 9	Bus/ RPU Freq.
604	133	AB	BC	BC	BC	BC	AB	BC	AB	AB	66.6/ 133
	150	AB	AB	BC	BC	BC	BC	AB	AB	AB	50/ 150
	166	BC	BC	BC	BC	BC	BC	AB	AB	AB	55/ 165
604ev	150	BC	AB	BC	AB	AB	AB	BC	BC	AB	60/ 150
	166	AB	BC	BC	AB	AB	AB	BC	BC	AB	66.6/ 166
	180	BC	AB	BC	AB	AB	BC	AB	AB	AB	60/ 180
	200	AB	BC	BC	AB	AB	BC	AB	AB	AB	66.6/ 200
603e	100	AB	BC	BC	BC	AB	BC	BC	AB	AB	66.6/ 100
	120	BC	AB	BC	BC	AB	AB	BC	AB	AB	60/ 120
	133	AB	BC	BC	BC	AB	AB	BC	AB	AB	66.6/ 133
603ev	150	BC	AB	BC	BC	AB	AB	BC	BC	AB	60/ 150
	166	AB	BC	BC	BC	AB	AB	BC	BC	AB	66.6/ 166
	180	BC	AB	BC	BC	AB	BC	AB	AB	AB	60/ 180
	200	AB	BC	BC	BC	AB	BC	AB	AB	AB	66.6/ 200

3.29 Video/Graphics

The Longtrail board does not contain an on–board video controller.

3.30 Audio

The board contains a fully CHRP-compatible audio system, comprised of the CS4236, which contains FM synthesis function. Space is provided for Yamaha YMF2898 and YAC516E FM synthesis chips if regression to the 4232 controller is necessary.

3.30.1 Audio Subsystem Hardware Specification

3.30.1.1 Overview

The audio subsystem provides the capability to record and play back high quality audio in a PowerPC CHRP system. It consists of a Crystal Semiconductor CS4236 or CS4232 Multimedia Codec connected to the ISA bus of the system planar board. Several op–amps are used to condition the analog signals going into the Codec and coming out of it. The CS4236 contains an internal FM synthesizer. The subsystem also includes a standard joystick interface and a MIDI I/O interface. The joystick and MIDI interfaces are accessible through a DB–15 connector. Up to two joysticks can be attached to this connector. MIDI I/O requires the use of a joystick/MIDI breakout cable. Additionally provisions have been made for an optional wavetable synthesizer and an optional 3–D sound processor module.

The subsystem has essentially two parts:

1. Analog Subsystem
2. Digital Subsystem.

The analog portion consists of the analog audio I/O jacks (Microphone, Line In, Line Out and Headphone Out) along with buffer amplifiers used to condition the analog signals connected to the CS4231 Codec. It also includes the analog portion of the optional wavetable synthesizer and the optional 3–D sound processor module.

The digital portion provides the joystick interface for two PC style joysticks, the MIDI I/O, and the bus interface to a standard ISA bus.

The following features are supported by the hardware:

- Simultaneous record and playback of 8–bit or 16–bit audio
- Up to 48 KHz sampling rates for Digital Audio Tape (DAT) quality audio
- Stereo microphone input with phantom power for electrical as well as dynamic type microphones
- Stereo line level input to connect other external audio devices to the subsystem
- Stereo line level output to feed other external audio devices such as powered speakers or stereo amplifiers
- Stereo headphone output to drive headphones directly from the audio subsystem
- Stereo auxiliary input connector to hook up the audio out of a CD–ROM device internal to the system box
- MIDI interface for connecting external synthesizers
- A 1 Watt speaker amplifier to drive the system speaker
- Soundblaster Pro™ compatibility for games
- Auxiliary connector to connect a fax/modem with voice capabilities
- Connector for an optional Waveblaster™ compatible wavetable synthesis expansion board
- Connector for an optional Philips 3–D sound processor module.

3.30.2 Specifications

3.30.2.1 Input Specifications

Sampling Rate	Up to 48 KHz per channel
Channel Bandwidth	20 Hz to 20 KHz (+1/–3dB)
Dynamic Range	16–bit resolution
S/(N+D) (Line Input)	82 dB (full scale at 1 KHz, analog path)
	77 dB (full scale at 1 KHz, digital loopback)

Line Input	Input Impedance	10 KOhms (for use with 2 KOhm source impedances or lower)
	Signal Level	2 Vrms nominal
	Connector	Planar board stereo, stacked 3.5 mm 3–conductor mini phone jack with: Tip: Left Channel Ring: Right Channel Sleeve: Audio Ground
Microphone Input	Input Impedance	3.6 KOhms (for use with 50 to 1000 Ohm microphones)
	Phantom Power	Both channels 1 mA for nominal operation at 3 VDC
	Signal Level	7.75 mVrms nominal up to 200 mVrms max.
	Connector	Planar board stereo, stacked 3.5 mm 3–conductor mini phone jack with: Tip: Left Channel Ring: Right Channel Sleeve: Audio Ground
CD–ROM Audio Input	Input Impedance	10 KOhms
	Signal Level	1 Vrms nominal
	Connector	1X4 ELCO style male connector

3.30.2.2 Output Specifications

Sampling Rate	Up to 48 KHz per channel
Channel Bandwidth	20 Hz to 20 KHz (+1/–3 dB)
Dynamic Range	16–bit resolution
S/(N+D) (Line Output)	82 dB (full scale at 1 KHz, analog path) 77 dB (full scale at 1 KHz, digital loopback)

Line Output	Output Impedance	1 KOhms (for use with 10 KOhm load impedances or higher)
	Signal level	2 Vrms nominal
	Connector	Planar board stereo, stacked 3.5 mm 3–conductor mini phone jack with: Tip: Left Channel Ring: Right Channel Sleeve: Audio Ground
Headphone output	Output Impedance	12 Ohms (for use with 32 Ohm or higher headphones)
	Signal level	2 Vrms (Bridge)
	Connector	Planar board stereo, stacked 3.5 mm 3–conductor mini phone

		jack with:	
		Tip:	Left Channel
		Ring:	Right Channel
		Sleeve:	Audio Ground
System Speaker Output	Speaker Impedance	8 Ohms (typical)	
	Power Output	1 Watt max (8 Ohm load)	
	Connector	2 pin Berg type header	

3.31 Performance

TBD

3.32 Wave Table Cards

Table 100 shows a representative list of wave table cards that may be installed at J??.

Table 100. Wave Table Cards

Manufacturers	Models
TBD	

3.33 3-D Sound Enhancement

Table 101 shows a representative list of 3-D sound cards that may be installed at JXX.

Table 101. 3-D Sound Cards

Manufacturers	Models

Appendix A Changes from Pass 1 to Pass 2

Appendix A.1 Purpose and Organization

This document outlines the major changes between the Pass 1 release and the Pass 2 release of the Longtrail CHRP PowerPC Reference Design. The document does not attempt to describe every minor implementation difference. It is a bridge between the Pass 1 specification and the Pass 2 specification.

Appendix A.2 Major Changes

The major changes are listed with a paragraph or two of rationale and explanation. Subordinate changes which were driven by the major change are listed in indented format under each major change. All changes are driven by the desire to make the board less expensive and one that OEMs can very quickly bring to market.

Appendix A.2.1 Processor Card Replaced With PGA Processor in ZIF Socket

Major customers indicated a strong preference for this mode of processor attachment in order to better fit their business model. IBM has announced availability of all 60x PowerPC processors in PGA. A common pinout has been designed so that the 603 family or 604 family processors may be interchanged in a common socket. The socket chosen is a 17x17 fully populated array similar to socket 3. Low cost fan sink and or passive heat sink solutions are available.

Appendix A.2.1.1 VRM Chosen for Regulator

The 40–pin VRM module used in Pentium–Pro designs was chosen because it is expected to be a readily available commodity and it meets requirements. OEMs may be able to make certain optimizations by setting the core voltage to values other than 3.3 or 2.5 volts.

Appendix A.2.1.2 Autoconfigure PAL Replaced with Jumpers or ”KEY” card

The processor card had seven presence detect bits which were used to drive a PAL which configured the bus speed, PLL ratio, and bus mode. The PGA socket does not contain these presence bits. Accordingly, jumpers are required to set these parameters for the particular type and speed of processor installed. Longtrail is designed to accept any 60x family processor except the original 603 which is near end of life.

A socket is defined for a ”KEY” card which may be used to set all configuration variables without the use of jumpers. OEMs may choose either option or both when assembling the board. IF the ”KEY” card option is chosen, a small 20 pin card must be provided with each system to customize the board to the mated processor. The card has only wires that replace jumper connections. A different ”KEY” would have to be provided to the customer in in order to upgrade. IBM does not supply ”KEY” cards. Jumpers are required:

- 4 – to program the VRM output voltage
- 3 – to set the cpu/pci bus frequencies to 50/25, 27.5/55, 60/30, or 66/33 MHz as best optimizes the CPU speed for the inserted processor
- 4 – to set the CPU PLL ratio
- 2 – to set the bus mode according to the family of the inserted processor.

Appendix A.2.1.3 Debug Support Modified

The Pass 1 offering included a 60x bus probe card set compatible with the processor card. This is not appropriate to the PGA processor. HP offers the HP E2465A PowerPC 604 PGA Preprocessor Interface product which may be adapted to probe the 60x bus at the PGA processor. Other vendors may have similar offerings. IBM will not offer a probe device.

Appendix A.2.2 Golden Gate Bridge Chip Set Upgraded to Pass2 Silicon

Appendix A.2.2.1 COASt L2 Cache Modules Supported

The GG designers chose to provide support for commodity L2 cache modules available for X86 systems. Cache modules supporting linear burst order are required. The 182–pin standard on Pass 1 has been abandoned. The chip set contains support for both burst and flow–though cache designs. Both the 8–bit tag and 11–bit tag versions are supported. The board utilizes the FX connector and can physically accept any version of the COASt module.

Appendix A.2.2.2 SDRAM Support Added

Support for SDRAM has been implemented in the Pass 2 design. The Pass 1 board supported it, but the function was not in the first silicon.

Appendix A.2.2.3 GG Refinements

Pass 2 silicon contains additional buffers and other refinements which speed the operation but do not affect function. Firmware has minor impacts due to register changes.

Appendix A.2.3 Design changed to Four–layer

Customers indicated that the design must be on a four–layer board in order to be cost competitive. Pass 1 was a six–layer design. This decision drove a decision to substantially change the pinout of the pass 2 GG chips.

Appendix A.2.4 I/O Cable Connector Scheme Changed

The Pass 1 board used connectors in order to provide egress for both the Apple–type connectors and the IBM compatible type connectors. The Pass 2 board uses less costly connectors and allows the OEM options to assemble the board in a way that cost–optimizes for Apple–type connectors or for compatible–type connectors. The OEM may also support both sets of connectors. The keyboard connector site has a dual footprint that may be populated with either an ADB connector or a stacked KB/MSE connector. The VGA connector space has been eliminated.

Appendix A.2.5 Clock Chip Replaced

IC works announced a clock chip which combines the processor, PCI, and SDRAM clocks into one low–cost clock chip. We adopted this chip. There is virtually no penalty in the cost of the board to support SDRAM.

Appendix A.2.6 308 Errata Embedded

There are minor hardware errata outstanding against the current version of the NS ’308 chip. These have been embedded. The schematic indicates how to reverse the changes when the chip is upgraded.

Appendix A.2.7 3.3V MACROM Standard Supported

A standard for 3.3v MACROM SIMMs has been worked out with Apple Computer. There are minor pinout changes but no functional differences. Our objective is to use standard 3.3V MACROM SIMMs to be offered by Apple Computer.

Appendix A.2.8 Tollgate ISA Bridge

Tollgate has been upgraded to pass 2 silicon. It is currently being tested on pass 2 boards. The plan is to build pass 2 boards with Tollgate. OF will be modified accordingly.